10 Gbit/s Transmitter MUX with Re-timing GD16555B

Preliminary

General Description

GD16555B is a 9.95328 Gbit/s transmitter chip for use in SDH STM-64 and SONET OC-192 optical communication systems.

GD16555B integrates all the main functions of the transmitter, which is clock generation, PLL circuits and multiplexer in a single monolithic IC. Hence only an external loop filter is required.

The main functions of GD16555B are shown in the figure below. The clock generation is made on-chip by a low noise and tuneable 10 GHz VCO. The VCO centre frequency is controlled by a PLL with an external loop filter, allowing the user to control the loop characteristic.

The clock synchronisation is controlled by the Phase and Frequency Detector with a 155 MHz or 622 MHz reference clock input (package bonding option).

GD16555B multiplexes a 16 bit parallel 622 Mbit/s interface into a serial 9.9553 Gbit/s data stream.

The output of the MUX stage is retimed by the 10 GHz clock and the output driver is a *Current Mode Logic* (CML) output with internal 50 Ω termination resistors.

The 16 bit wide parallel input interface is differential CML with 50 Ω internal load termination, and with a 622 MHz clock output mastering the timing at the STM-4 interface. The phase of the output clock is selected in four phases: 0°, 90°, 180°, and 270° by two select pins.

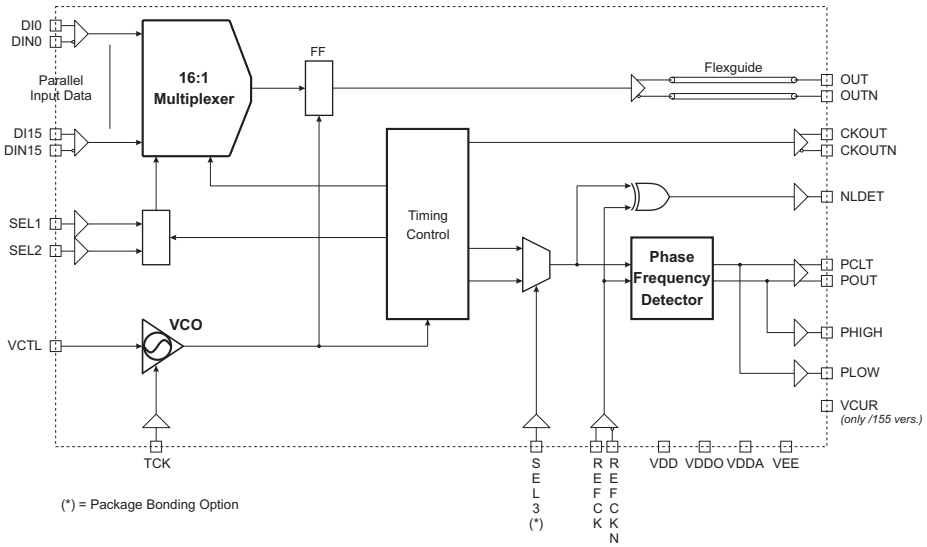
GD16555B is manufactured in a Silicon Bipolar process.

GD16555B uses a single -5.2 V supply voltage.

The power dissipation is 2 W, typical.

GD16555B is delivered in a *Multi Layer Ceramic* (MLC) package, with internal high-speed 50 Ω transmission lines.

All high-speed signals is bonded with GiGA's proprietary Flexguide® Bonding Technique.



Features

- On-chip low noise 10 GHz VCO with a wide tuning range.
- Automated capture of the VCO frequency by a true phase and frequency detector.
- Retiming of MUX stage output with 10 GHz clock.
- Clock failure detection NLDET.
- 16:1 MUX with differential 622 Mbit/s CML data input.
- CML data input with 50 Ω internal load termination.
- 622 MHz clock output for counter clocking.
- Clock output is selectable in four phases: 0°, 90°, 180°, or 270°.
- 155 MHz or 622 MHz reference clock input (package bonding option).
- Single supply operation: -5.2 V
- Low Power dissipation: 2 W (typ.).
- Silicon Bipolar process.
- 68 pin Multi Layer Ceramic (MLC) package.
- Flexguide® Bonding Technique.

Applications

- Telecommunication systems:
  - SDH STM-64
  - SONET OC-192.
- Fibre optic test equipment.
- Submarime transmission systems.

Functional Details

The main function of GD16555B is as transmitter in STM-64 and SONET OC-192 optical communication systems.

It integrates:
- *Voltage Controlled Oscillator* (VCO)
- *Phase and Frequency Detector* (PFD)
- 16:1 Multiplexer
- Re-timing of output data.

VCO

The VCO is an LC-type differential 10 GHz oscillator controlled by pin VCTL and with a tuning range of ±5 %. The VCO and the clock divider circuit generates the clock signal and load pulses needed for multiplexing. It also generates the output clock (CKOUT/ CKOUTN) and the clock used in the phase and frequency detector.

With the VCTL voltage at -3 V the VCO frequency is fixed at 9.953 GHz and by changing the voltage from 0 to –5.2 V the frequency is controlled from 9 GHz to 10.2 GHz (See VCO Measurements on page 17). The modulation bandwidth of VCTL is 90 MHz.

PFD

The PFD is made with digital set/reset cells giving it a true phase and frequency characteristic. The reference clock (REFCK/REFCKN) to the PFD is 155 or 622 MHz (package bonding option, two different product numbers).

A No Lock DETection signal (NLDET) is provided as a status signal of the PLL. It compares the VCO clock with the reference clock and is high whenever they differ. Using NLDET the situation of clock failure, i.e. loss of signal can be detected.

The reference clock input has 50 Ω internal termination resistors to pin VCMLT and should be used differential.

The PLL will synchronize the 10 GHz VCO to the external reference clock. Noise from the reference clock, within the PLL bandwidth will be multiplied and added to the 10 Gbit/s output by the divider ratio between VCO and reference clock i.e. N = 16 / 64 or in terms of noise as 20Log(16) = 24 dB or 36 dB. A low noise reference clock with high frequency stability is required in order to fulfill the ITU-T jitter requirements.

Inputs

The parallel input interface is 622 Mbit/s differential *Current Mode Logic* (CML) with 50 Ω internal resistors. The 16 bits are multiplexed starting with DI0, DI1...DI15.

All CML inputs have 50 Ω internal termination resistors to a separated power pin (VCMLT). With VCMLT connected to 0 V all inputs are configured as CML inputs (high/low equal 0/-0.4 V) or with VCMLT connected to –2 V all inputs are configured as ECL compatible inputs (high/low equal -0.8/ -1.8 V). With ECL inputs the maximum current out of VCMLT is 400 mA and proper de- coupling of VCMLT is required.

The select inputs (SEL1-2 and TCK) are low-speed inputs, that can be connected directly to the supply rails (0 / -5.2 V).

Loop Filter

The external loop filter is made using an operational amplifier connected to output pins (PHIGH and PLOW). The characteristics of the phase lock loop are controlled by the loop filter components hence the op-amp is designed as an integrator by a feedback capacitor and a resistor. The gain-bandwidth of the op-amp need to be larger than the required PLL bandwidth in order not to limit it. The recommended op-amp is Analog Devices (AD8042) with a gain-bandwidth of 160 MHz sufficient for PLL bandwidths up to 50 MHz. The op-amp is used single supplied by -5.2 V. See Figure 1 for application information.

The phase information from the PFD is high frequency pulses at output pins (PHIGH and PLOW). They are open collector outputs with an 8 mA current drive and are terminated externally by 220 Ω to 0 V. A pre-filtering of the phase pulses are applied by a parallel 10 pF capacitor.

The PCB layout of the external loop filter and the connecting lines to PHIGH, PLOW and VCTL are critical for the jitter performance of the component. The artwork for the op-amp and the passive components should be placed very close to the pins of GD16555B in order to have connecting lines as short as possible. Ideally the loop filter components are placed on the opposite side of the PCB directly underneath GD16555B. For more layout suggestions see the 10 Gbit/s evaluation board GD90244/255.

Alternatively the phase information is also available at output pins (PCTL and POUT) and they can be used with an external passive loop filter in applications with a low PLL bandwidth (< 1 MHz) instead of the above recommended active loop filter. The PCTL and POUT pins should always be terminated as shown in Figure 1 also even though they are not actively used in the PLL.

POUT is a high impendance input and will be destroyed if connected directly (low-ohmic, <25 kΩ) to -3.6 V to 0 V.

The Outputs

The 10 Gbit/s output driver is internal terminated with 50 Ω resistors to 0 V and bonded with Flexguides® from the die to the package edge. This bonding technique insures a true 50 Ω transmission line environment from the outside edge of the package through the package to the die. The output should be terminated externally with 50 Ω at the receive end and should be used differential. Both OUT and OUTN are best terminated with the same load resistor e.g. 50 Ω, an asymmetrically loading will decrease the performance of the output due to reflections. When terminated externally with 50 Ω, the output voltage is 650 mV_{PP}.

Both outputs **OUT/OUTN are not ESD protected** and extra precautions should be taken when handling the outputs (the internal 50 Ω resistor provides some ESD hardness making the input low impedance).

The clock outputs (CKOUT/N) are differential open collector outputs with a 8 mA output current. They are terminated externally with a resistor (R) to 0 V and the output voltage swing is
V = -50 × 8 mA = -400 mV with R = 50 Ω.
Increasing the resistor increases the output voltage swing and reduces the bandwidth.

Counter Clocking Timing

When the counter clocking timing is used to control the timing between GD16555B and the system ASIC, the output clock (CKOUT/CKOUTN) is feed to the system ASIC and clocks valid output data from the ASIC into GD16555B. For easy interfacing of the system ASIC, the output clock is selectable in four phases (0°, 90°, 180° or 270°) by SEL1-2. The maximum variation in the round trip delay should be less than 1.1 ns when using the counter clocking timing. This leaves 0.5 ns of valid data time for the GD16555B . The roundtrip delay is the total delay from clock in, to data out of the system ASIC and the board delay for clock and data. The setup and hold times between CKOUT and input data are specified for all four phases (see AC Characteristics on page 14). The valid time (e.g. the period of time where the in-

put data is not allowed to change) is given by adding the setup and hold times. The setup time is defined positive before the rising edge of CKOUT. The hold time is defined positive after the rising edge.

If the variation is bigger than 1.1 ns another type of different clocking timing is needed e.g. forward clocking timing.

It is recommended to use all data inputs differential for best performance.

Forward Clocking Timing

With the forward clocking timing both the data and the clock is applied to GD16555B with the clock as a reference clock input (REFCK/REFCKN). See AC Characteristics on page 15. It is important for the jitter performance that the clock is clean with no spurious frequency noise and no noise injection from data transitions. If the clock is generated from a CMOS ASIC an additional PLL is needed to clean up the clock before being applied as reference to GD16555B. When using GD16555B with forward clocking, the 622 MHz reference clock option should be ordered.

The Output Voltage Control

For the GD16555B version with a 155 MHz reference clock (GD16555B/155-XX) a control signal (VCUR) is available at pin 41.

By controlling the voltage at VCUR the DC output voltage at OUT/OUTN is adjusted in the range form 0.1 V to 0.8 V. The VCUR can be operated from 0 V to VEE.

For the GD16555B version with a 622 MHz reference clock (GD16555B/622-XX) the control signal (VCUR) is not available at pin 41.

GD16555B versus GD16255A

GD16555B is plug compatible and offers the same or even better performance compared with GD16255A. The pinouts and the configurations of I/O´s are the same except of the three differences as described below:

- No RESET pin
- SEL 1/2 do not affect the timing relation between the reference clock and the internal sampling of input data.
- The values of one resistor and capacitor in the recommended loop filter.

Package

GD16555B is packaged in a 68 pin Multi Layer Ceramic package with internal 50 Ω transmission lines. The package is a cavity-down type, which gives effective cooling using the mounted heat spreader.

The 10 Gbit/s outputs are bonded with GiGA's Flexguide® Bonding Technique. These are flexible 50 Ω transmission lines bonded from the die to the internal package pin. With the use of Flexguide® distortion free transmission is ensured throughout the package.

External Circuits

The main external circuits needed to make GD16555B work as a 10 Gbit/s transmitter IC with re-timing and multiplexer are:

- An active loop filter with op-amp
- A reference clock at 155 MHz or 622 MHz with high frequency stability
- Pull up resistors and de-coupling capacitors

Mounting and Layout of PCB

The component can be mounted on a standard FR4 epoxy printed circuit board when special attention is taken in the layout and in the mounting of the component.

It is important for the performance of the component that the leads of pin OUT and OUTN (10 Gbit/s outputs) are made very short (<1 mm) when mounted on the board. Best way to make the leads short are to cut a hole in the PCB and to mount the component inside the hole. The length of the two critical leads is reduced to less than 0.5 mm whereas the rest of the leads are kept at 2 - 4 mm in order for mechanical stability. On the back side the head spreader on the package is thermally mounted to a metal block with heat sink compound (see paragraph "Mounting of Component on PCB" on page 18).

In cases where the above mounting technical is not applicable, the component can be mounted directly on the board with bend leads accepting longer leads for the 10 Gbit/s outputs. The component is available with straight leads and with gull wing leads (see the package outline drawings on page 19).

In the layout of the PCB the 10 Gbit/s inputs are connected with 50 Ω *Micro Strip Lines* (MSL) to the high- speed connector. The MSL should be as short as possible (< 30 mm) with a plain and solid ground plan below. The layout artwork for the loop filter is placed preferable on the opposite side of the component with very short connections to the pins of GD16555B. The 100 Ω resistors and 10 pF capacitor connected from PHIGH and PLOW to 0 V should be placed very close to the package pin no. 50 and 53.

The environment around the loop filter and the 10 Gbit/s outputs is noise sensitive and no noise generating lines are allowed in this area.

The power supply to GD16555B should be separated from other noise generation components on the board and de-coupled as shown on Figure 2. DC-DC converters are only allowed on the same board if proper noise filtering is applied.

Thermal Condition

The component dissipates 2.0 W with a –5.2 V voltage supply and need forced cooling with a heat sink thermally connected to the heat spreader. The thermal connection should ensure the case temperature in the range from 0 to 70 °C with the given ambient conditions e.g. temperature and air flow.

Power Noise Rejection

In a noisy environment special attention must be taken as described above to optimize the jitter performance and to reduce the input sensitivity penalty from injected noise. The *Power Supply Rejection Ratio* (PSRR) is improved by adding a serial resistor (3.3 kΩ) and capacitor (33 nF) from the positive input of the op-amp to the power pin (VEE) as shown in Figure 1.

Application

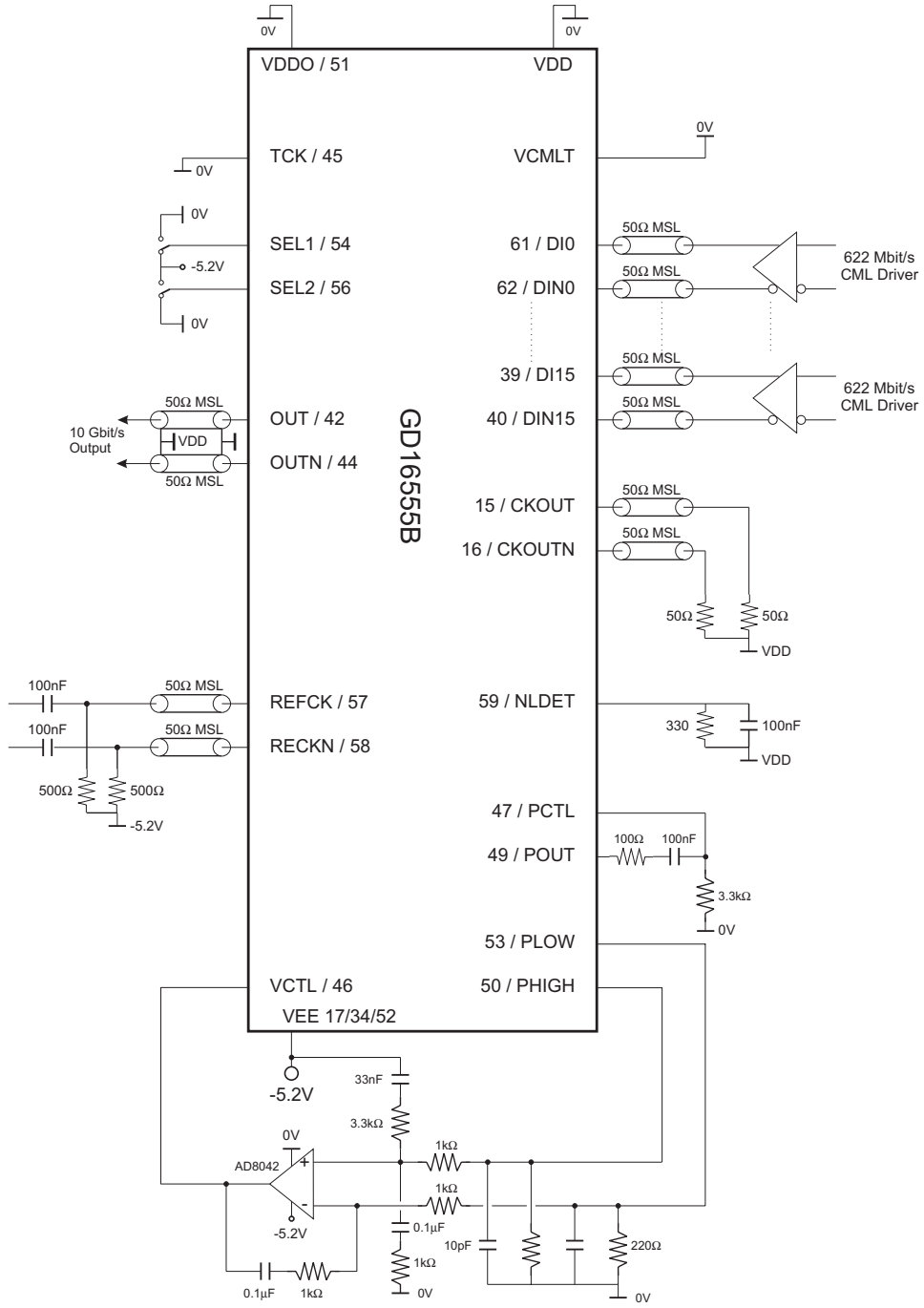


Figure 1. *Application Information*

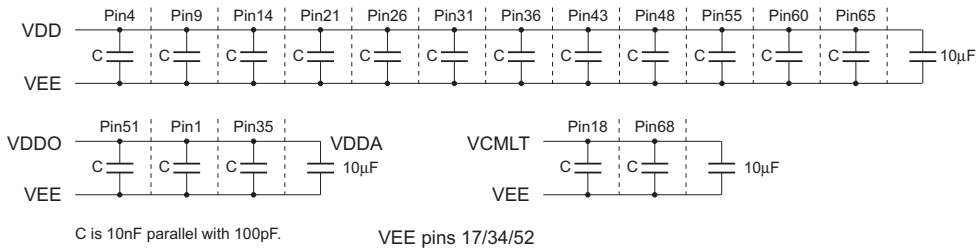


Figure 2. *De-coupling Supply*

10 Gbit/s Output Interface

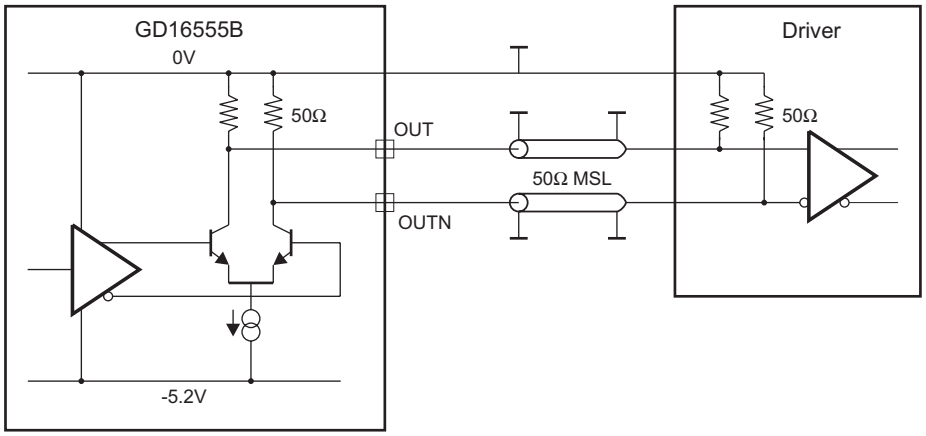


Figure 3. *10 Gbit/s Outputs (OUT/OUTN), DC Coupled*

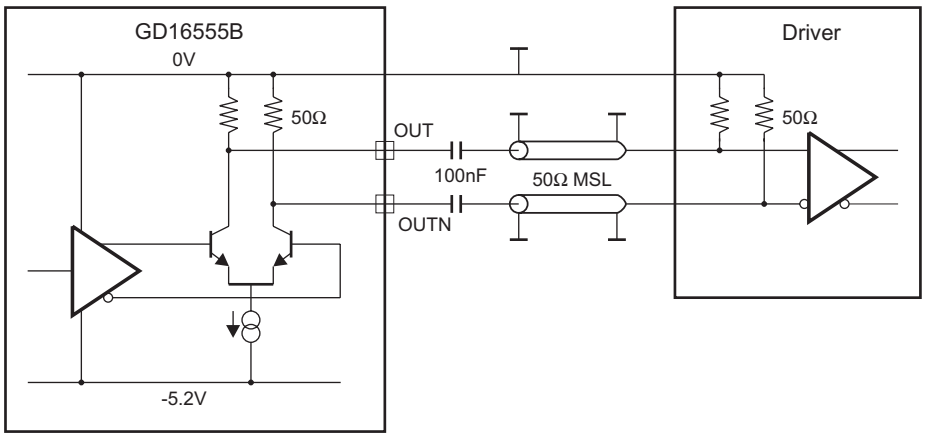


Figure 4. *10 Gbit/s Outputs (OUT/OUTN), AC Coupled*

622 Mbit/s Output Interface

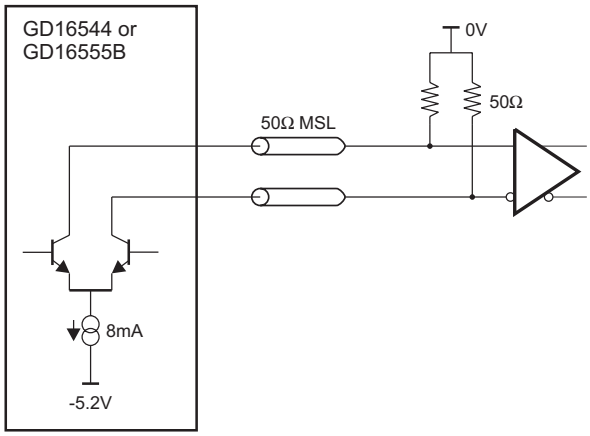


Figure 5. *Open Collector Output*

Open collector outputs should always be terminated at the receiver end, preferably 50 Ω .

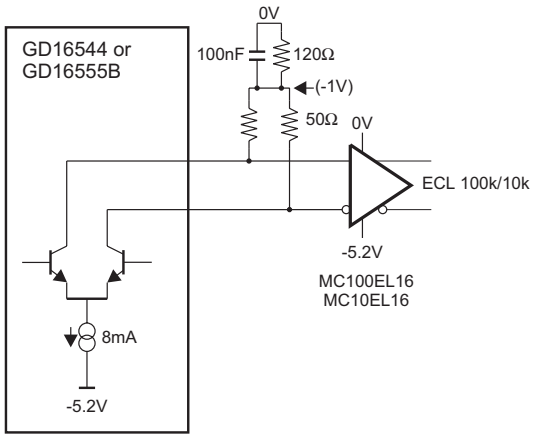


Figure 6. *ECL 100k or 10k Output.*

ECL 100k or 10k output using ECL driver MC100EL16/ MC10EL16.

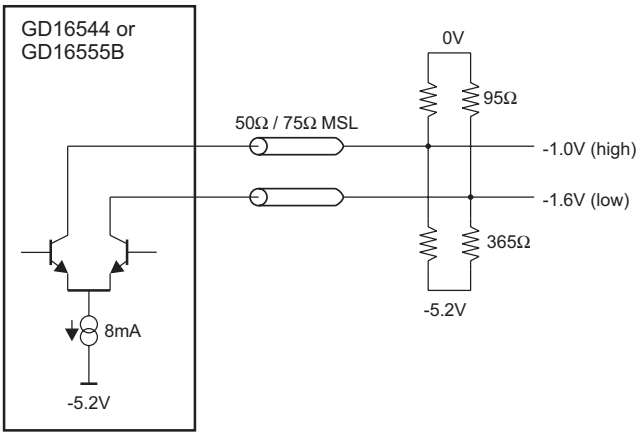


Figure 7. *ECL Compatible Output*

ECL compatible output with a voltage swing of 600 mV (single-ended) or 1200 mV (differential).

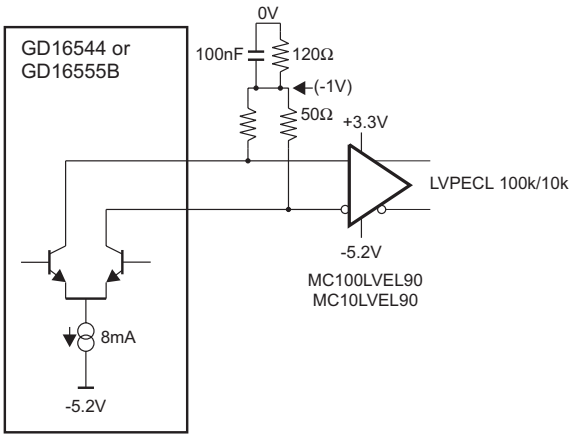


Figure 8. *Low Voltage PECL Output*

Low voltage PECL output using PECL driver MC100LVEL90/ MC10LVEL90.

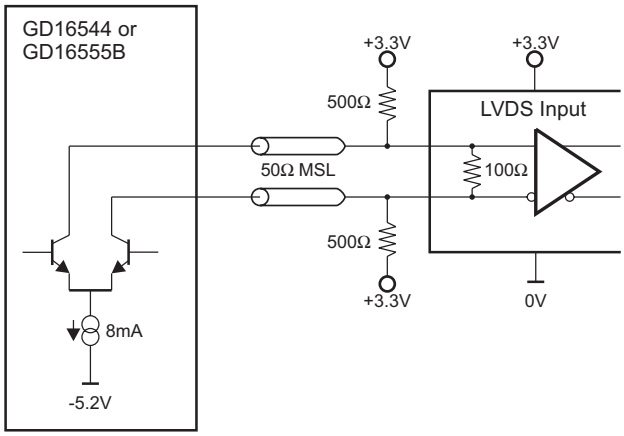


Figure 9. *LVDS Compatible Output*

Reference Clock Input

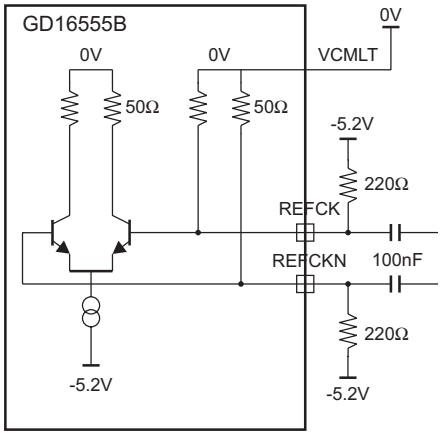


Figure 10. *Reference Clock Input (REFCK/REFCKN), Differential AC Coupled.*

622 Mbit/s Input Interface

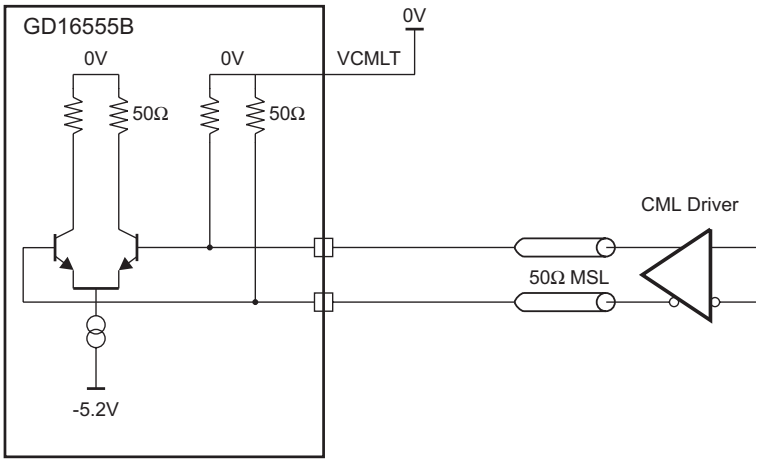


Figure 11. *CML input interface with a 0/-0.4 V input voltage swing (DC coupled) by connecting VCMLT to 0 V.*

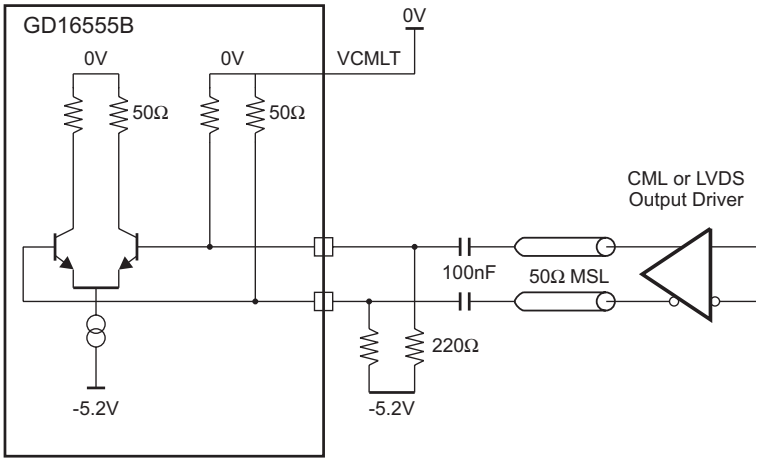


Figure 12. *CML or LVDS input interface with a 0/-0.4 V input voltage swing (AC coupled) by connecting VCMLT to 0 V.*

Pin List

Mnemonic:	Pin No.:	Pin Type:	Description:
DI0, DIN0 DI1, DIN1 DI2, DIN2 DI3, DIN3 DI4, DIN4 DI5, DIN5 DI6, DIN6 DI7, DIN7 DI8, DIN8 DI9, DIN9 DI10, DIN10 DI11, DIN11 DI12, DIN12 DI13, DIN13 DI14, DIN14 DI15, DIN15	61, 62 63, 64 66, 67 2, 3 5, 6 7, 8 10, 11 12, 13 19, 20 22, 23 24, 25 27, 28 29, 30 32, 33 36, 37 39, 40	CML In	Data input, differential 622 Mbit/s. Multiplexed to serial output starting with DI0, DI1...DI15.
REFCK, REFCKN	57, 58	CML In	Reference clock input, differential 155 MHz or 622 MHz (package bonding option).
SEL1, SEL2	54, 56	ECL In	Select the phase of CKOUT. SEL1 SEL2 0 0 T_D=0° 1 0 T_D=90° 0 1 T_D=180° 1 1 T_D=270°
OUT, OUTN	42, 44	CML Out	Data output, differential 10 Gbit/s. **No internal ESD output protection**.
CKOUT, CKOUTN	15, 16	Open Collector	Clock output, differential 622 MHz. Should always be terminated with a resistor.
PCTL, POUT	47, 49	Analogue Out/In	Phase-Frequency detector outputs.
PHIGH, PLOW	50, 53	Open Collector	Phase-Frequency detector outputs. Should always be terminated with 50 Ω to VDD.
VCTL	46	Analogue In	VCO input voltage control.
NLDET	59	Open Collector	No Lock DETect output. Should always be terminated with a resistor.
TCK	45	ECL In	Connect to VDD. Used for test purpose.
VDDO	51	PWR	VCO Ground 0 V. For test purpose connect to VEE.
VCMLT	18, 68	PWR	CML input resistor termination voltage.
VDD	4, 9, 14, 21, 26, 31, 38, 43, 48, 55, 60, 65	PWR	Digital Ground 0 V.
VDDA	1, 35	PWR	PLL Ground 0 V.
VEE	17, 34, 52	PWR	-5.2 V Digital supply voltage.
VCUR	41	Analogue In	Output voltage control in GD16555B/155-XX versions.
NC	41		Connect to VEE in GD16555B/622-XX versions.

Package Pinout

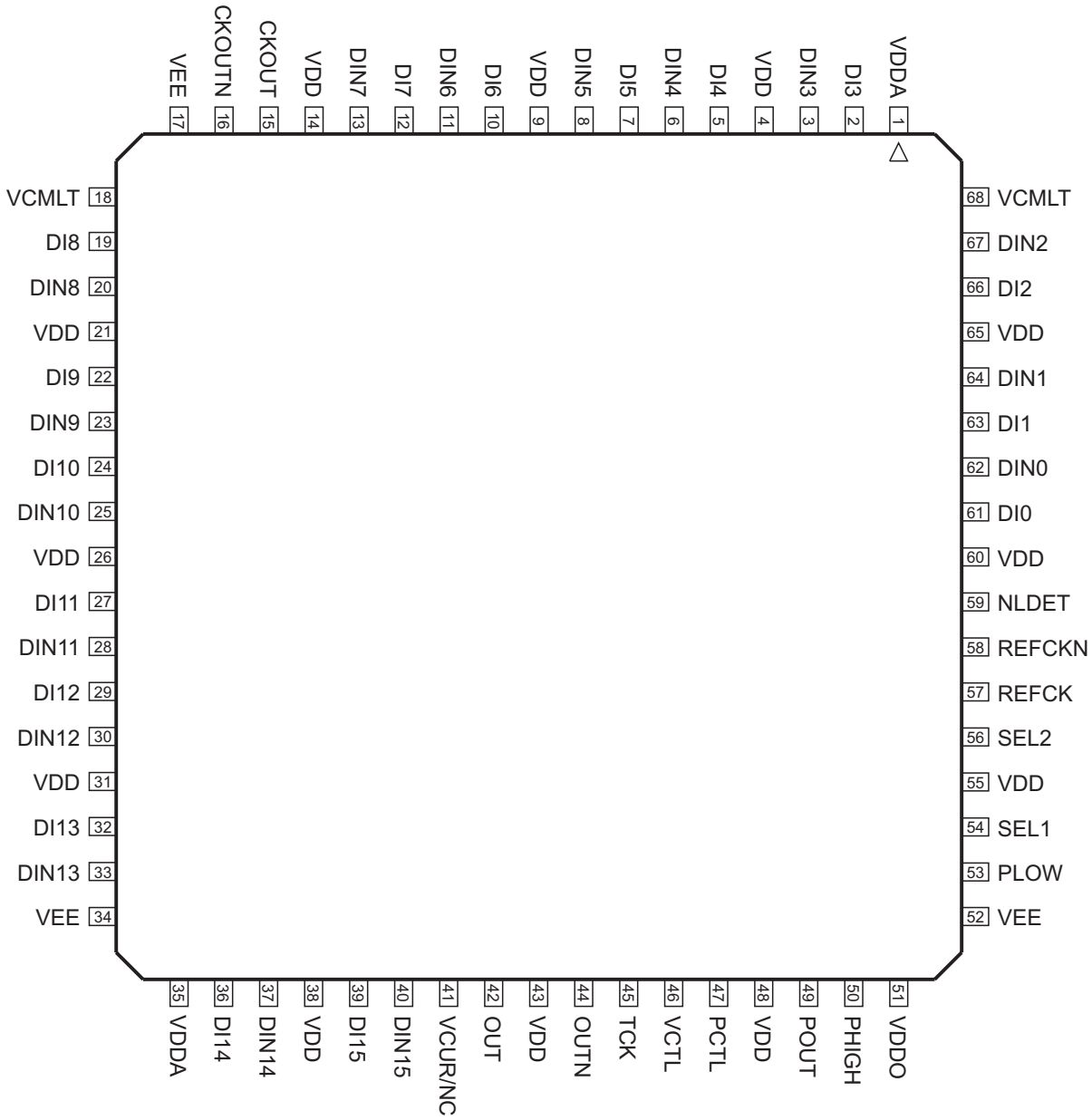


Figure 13. *Package Pinout, Top View*

Note: VDD = Cavity

Maximum Ratings

These are the limits beyond which the component may be damaged.
All voltages in table are referred to VDD/VDDA.
All currents are defined positive out of the pin.
VDD is 0 V or GND

Symbol:	Characteristic:	Conditions:	MIN.:	TYP.:	MAX.:	UNIT:
V_{EE}	Negative Supply		0		-6	V
V_{CMLT}	CML Resistor Termination Voltage		0		+0.7	V
$V_{O\ CML}$	CML Output Voltage		0		V_{EE}	V
$I_{O\ CML}$	CML Output Current	Note 1	0		-12	mA
$V_{I\ CML}$	CML Input Voltage		V_{CMLT} -1.5		0.5	V
$I_{I\ CML}$	CML Input Current	Note 1	-25		25	mA
P_{OUT}	POUT Voltage		V_{EE}		-3.6	V
T_J	Junction Temperature		-55		+125	°C
T_S	Storage Temperature		-65		+150	°C

Note 1: Nominal supply voltages.

DC Characteristics

T_{CASE} = 0 °C to 70 °C.
All voltages in table are referred to VDD.
All currents are defined positive out of pin.
VDD is 0 V or GND

Symbol:	**Characteristic:**	**Conditions**:	**MIN.:**	**TYP.:**	**MAX.:**	**UNIT:**
V_{EE}	Negative Supply Voltage		-5.0	-5.2	-5.4	V
V_{CMLT}	CML Resistor Termination Voltage	Note 4	0		-2	V
I_{EE}	Supply Current		330	400	480	mA
$V_{IH\ CML}$	CML Input Voltage High, (50 Ω Input)	V_{CMLT} = 0V, Note 3	-0.1	0	+0.1	V
$V_{IL\ CML}$	CML Input Voltage Low, (50 Ω Input)	V_{CMLT} = 0V, Note 3	-0.25	-0.4	-1.0	V
$V_{IH\ ECL}$	ECL Input Voltage High, (50 Ω Input)	V_{CMLT} = -2V, Note 3	-1.0	-0.8	-0.5	V
$V_{IL\ ECL}$	ECL Input Voltage Low, (50 Ω Input)	V_{CMLT} = -2V, Note 3	-1.6	-1.8	-2.0	V
$V_{OH\ OC}$	Open Collector Output Voltage High	Note 1, 5	-0.05	0	+0.05	V
$V_{OL\ OC}$	Open Collector Output Voltage Low	Note 1, 5	-0.3	-0.4	-0.5	V
$I_{OH\ OC}$	Open Output Current High	V_{CMLT} = 0V, 50Ω Input	-0.1	0	+0.1	mA
$I_{OL\ OC}$	Open Output Current Low	V_{CMLT} = 0V, 50Ω Input	-7	-8	-9	mA
$V_{OH\ OUT}$	OUT/OUTN Voltage High	Note 1, 10 MHz	-0.1	-0.05	+0.05	V
$V_{OL\ OUT}$	OUT/OUTN Voltage Low	Note 1, 10 MHz	-0.6	-0.7	-0.8	V
$I_{OH\ OUT}$	OUT/OUTN Current High	Note 1		0		mA
$I_{OL\ OUT}$	OUT/OUTN Current Low	Note 1		-14		mA
$V_{IH\ SEL1\text{-}2,\ TCK}$	SEL1-2 and TCK Input Voltage High	Note 2	0	V_{EE} + 2		V
$V_{IL\ SEL1\text{-}2,\ TCK}$	SEL1-2 and TCK Input Voltage Low	Note 2		V_{EE} + 0.8	V_{EE}	V
$R_{IN\ CML}$	CML Input Resistor Termination	DC	45	50	55	Ω

Note 1: Output externally terminated by 50 Ω to 0 V.
Note 2: SEL1-2 and TCK can be connected directly to VDD or VEE.
Note 3: DI0/DIN0 to DI15/DIN15 are internally terminated by 50 Ω to V_{CMLT}.
Note 4: The CML inputs can be configured as ECL compatible by connecting V_{CMLT} to -2 V, hence all data inputs and REFCK/REFCKN have to be ECL.
Note 5: All open collector outputs should be terminated with a resistor to VDD even though they are not used.

AC Characteristics, General

T_{CASE} = 0 °C to 70 °C, VEE = -5.2 V.

Symbol:	Characteristic:	Conditions:	MIN.:	TYP.:	MAX.:	UNIT:
J_{TRF}	Jitter transfer	12 kHz < F < 2 MHz Note 1			0.1	dB
J_{GEN}	Jitter generation	12 kHz < F < 80 MHz Note 1			0.1	UI_{PP}
V_{OUT}	10 Gbit/s output voltage	Note 4	600	650		mV_{PP}
$V_{I,CML}$	CML input voltage sensitivity		200	100		mV_{PP}
Γ_{OUT}	OUT/OUTN output reflection coefficient	Note 2		-10		dB
F_{REFCK}	REFCK/REFCKN frequency, stability	F_{REF} = 155 MHz, Note 3	-10		+10	ppm
$D_{CYCLE, CKOUT/N}$	CKOUT/CKOUTN duty cycle	Differential	45		55	%
$D_{CYCLE, REFCK}$	REFCK duty cycle		45		55	%
$F_{MAX, REFCK}$	Maximum REFCK frequency	622 MHz reference option			635	MHz

Note 1: Measured with the recommended loop filter in the GD90244/255 evaluation board (1 UI = 100 ps).
Note 2: From DC to 6 GHz, measured on the GD90244/255 evaluation board. Depends on lead length, board, soldering, etc. of the component.
Note 3: 622 MHz is provided as a package bonding option.
Note 4: VEE = -5.2 V. Measured on the GD90244/255 evaluation board with the compound component mounted in a high speed socket.

AC Characteristics, Counter Clocking Timing

T_{CASE} = 0 °C to 70 °C, VEE = -5.2 V.

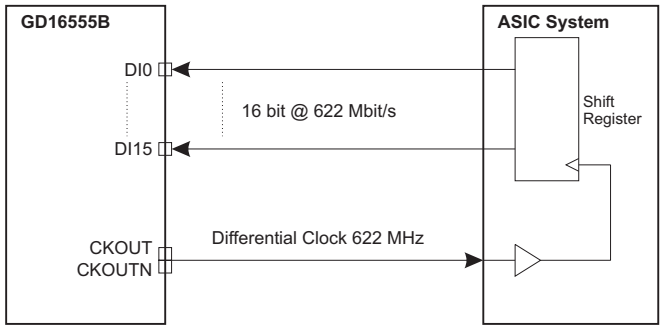


Figure 14. *Counter Clocking Timing.*

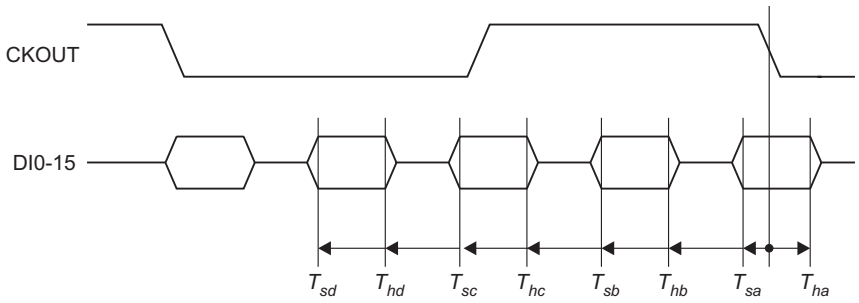


Figure 15. *Timing relation between input data and output clock.*

Symbol:	Characteristic:	Conditions:	MIN.:	TYP.:	MAX.:	UNIT:
T_{sa}	DI0-15 setup before CKOUT	SEL1,2: 0,0; Note 1	60	100	200	ps
T_{ha}	DI0-15 hold from CKOUT	SEL1,2: 0,0; Note 1	0	10	50	ps
T_{sb}	DI0-15 setup before CKOUT	SEL1,2: 1,1; Note 1	460	500	600	ps
T_{hb}	DI0-15 hold from CKOUT	SEL1,2: 1,1; Note 1	-400	-390	-350	ps
T_{sc}	DI0-15 setup before CKOUT	SEL1,2: 0,1; Note 1	860	900	1000	ps
T_{hc}	DI0-15 hold from CKOUT	SEL1,2: 0,1; Note 1	-800	-790	-750	ps
T_{sd}	DI0-15 setup before CKOUT	SEL1,2: 1,0; Note 1	1260	1300	1400	ps
T_{hd}	DI0-15 hold from CKOUT	SEL1,2: 1,0; Note 1	-1200	-1190	-1150	ps

Note 1: Setup time is defined positive before the falling edge of CKOUT and the hold time is defined positive after the falling edge of CKOUT.

AC Characteristics, Forward Clocking Timing

T_{CASE} = 0 °C to 70 °C, VEE = -5.2 V.

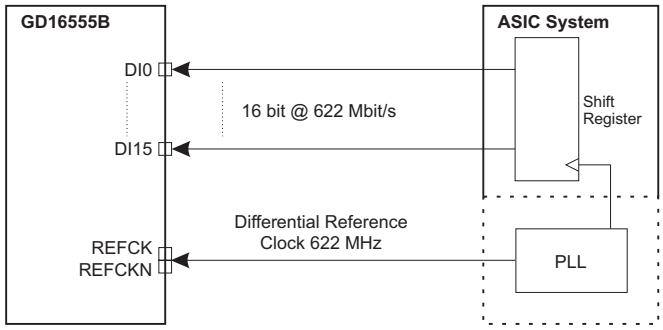


Figure 16. *Forward Clocking Timing.*

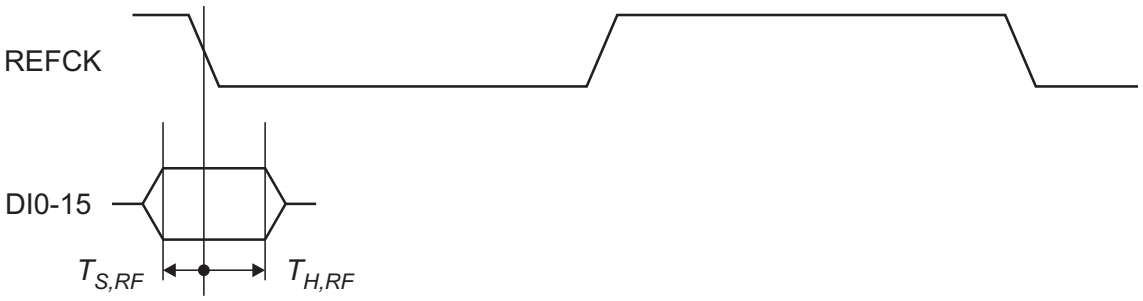


Figure 17. *Timing relation between input data and reference clock.*

Symbol:	Characteristic:	Conditions:	MIN.:	TYP.:	MAX.:	UNIT:
$T_{S,RF}$	DI0-15 setup before REFCK	VEE = -5.2V, T_C=70°, Note 1, 2	100			ps
$T_{H,RF}$	DI0-15 hold from REFCK	VEE = -5.2V, T_C=70°, Note 1, 2	250			ps

Note 1: 622 MHz reference clock option.
Note 2: Setup time is defined positive before the falling edge of CKOUT and the hold time is defined positive after the falling edge of CKOUT.

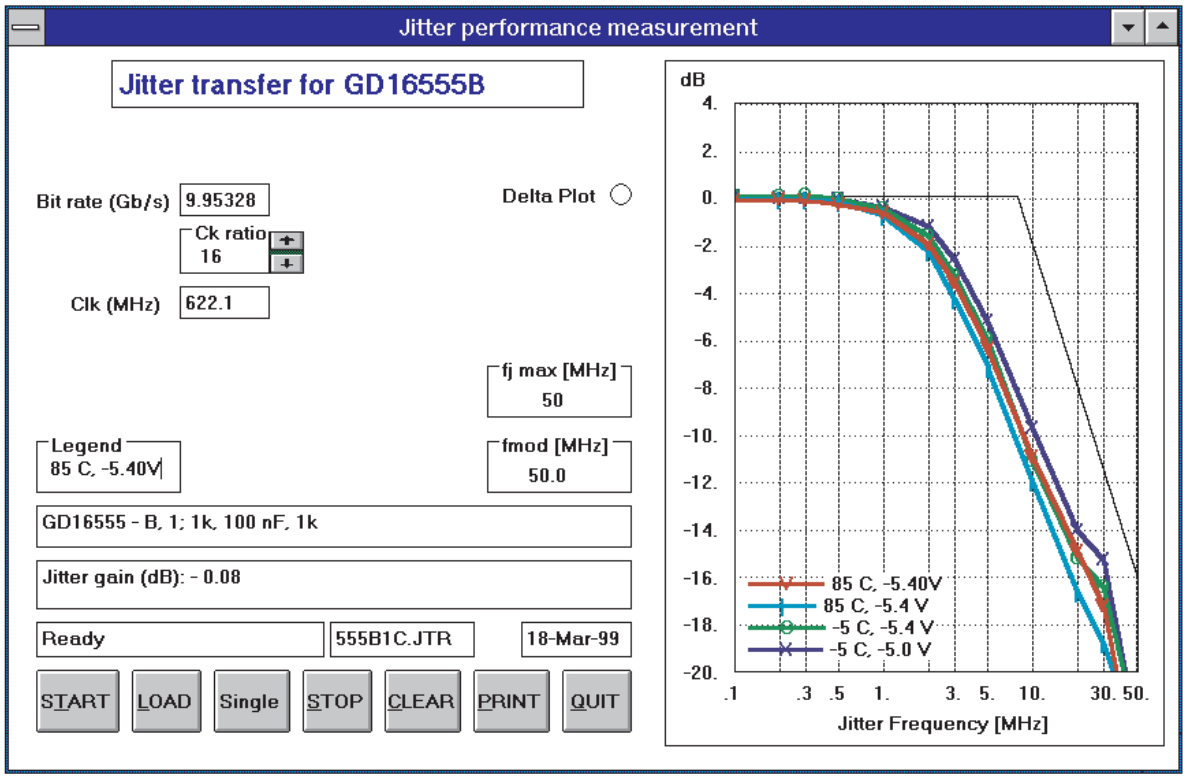


Figure 18. *Jitter transfer curve when connected with the recommended loop filter (see Figure 1) on the evaluation board GD90244/255. The case temperature -5 °C to 85 °C and power supply -5.0 V and -5.4 V.*

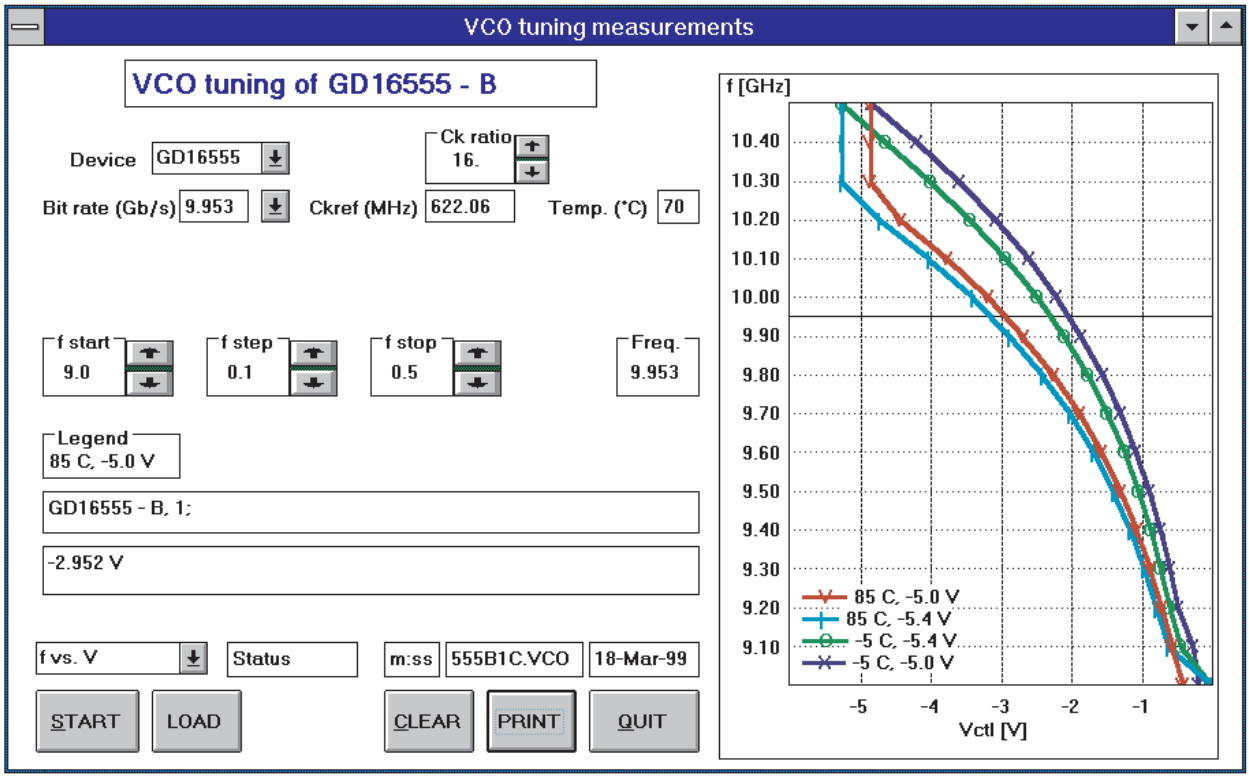


Figure 19. *VCO tuning curves.*

The tuning curves are measured at -5 °C and 85 °C and at supply voltages of -5 V and -5.4 V.

Mounting of Component on PCB

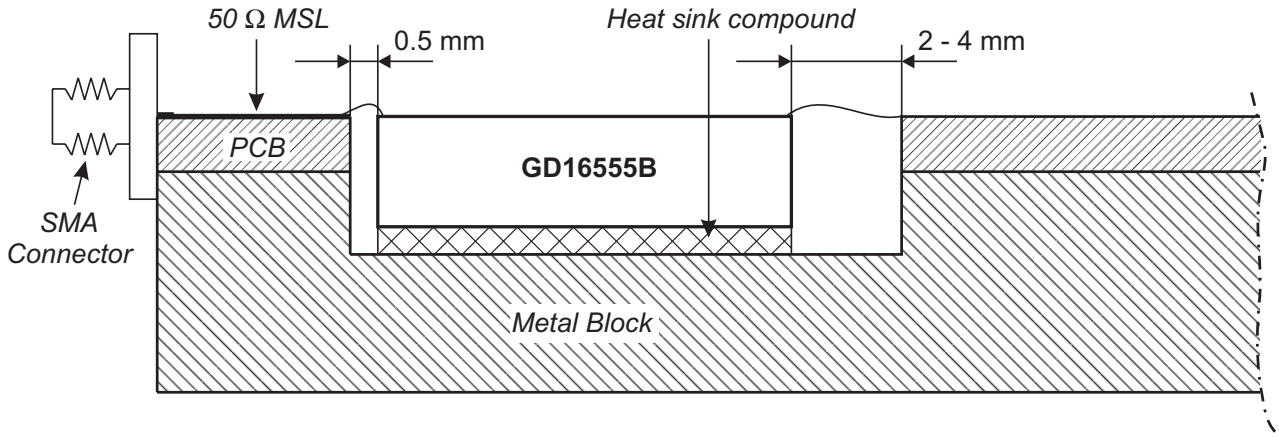


Figure 20. *Example 1.*

Mounting of the component inside a hole in the PCB with short leads for the 10 GBit/s inputs. The headspreader is down side towards the metal side for best cooling of the component.

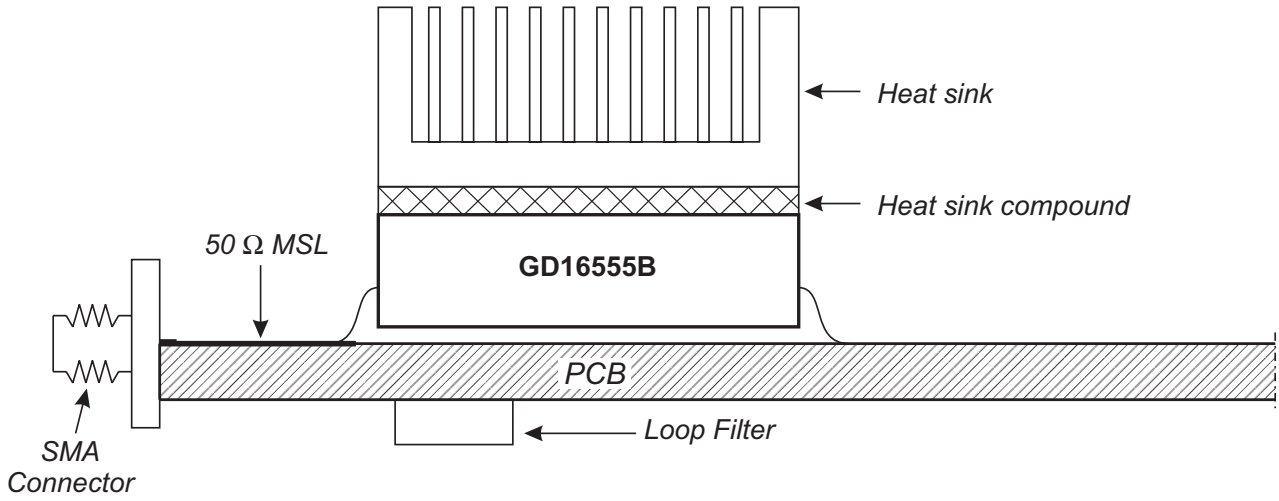


Figure 21. *Example 2.*

Mounting of the component on the PCB with bend leads (gullwings) The headspreader is thermal mounted to a heat sink.

Package Outline

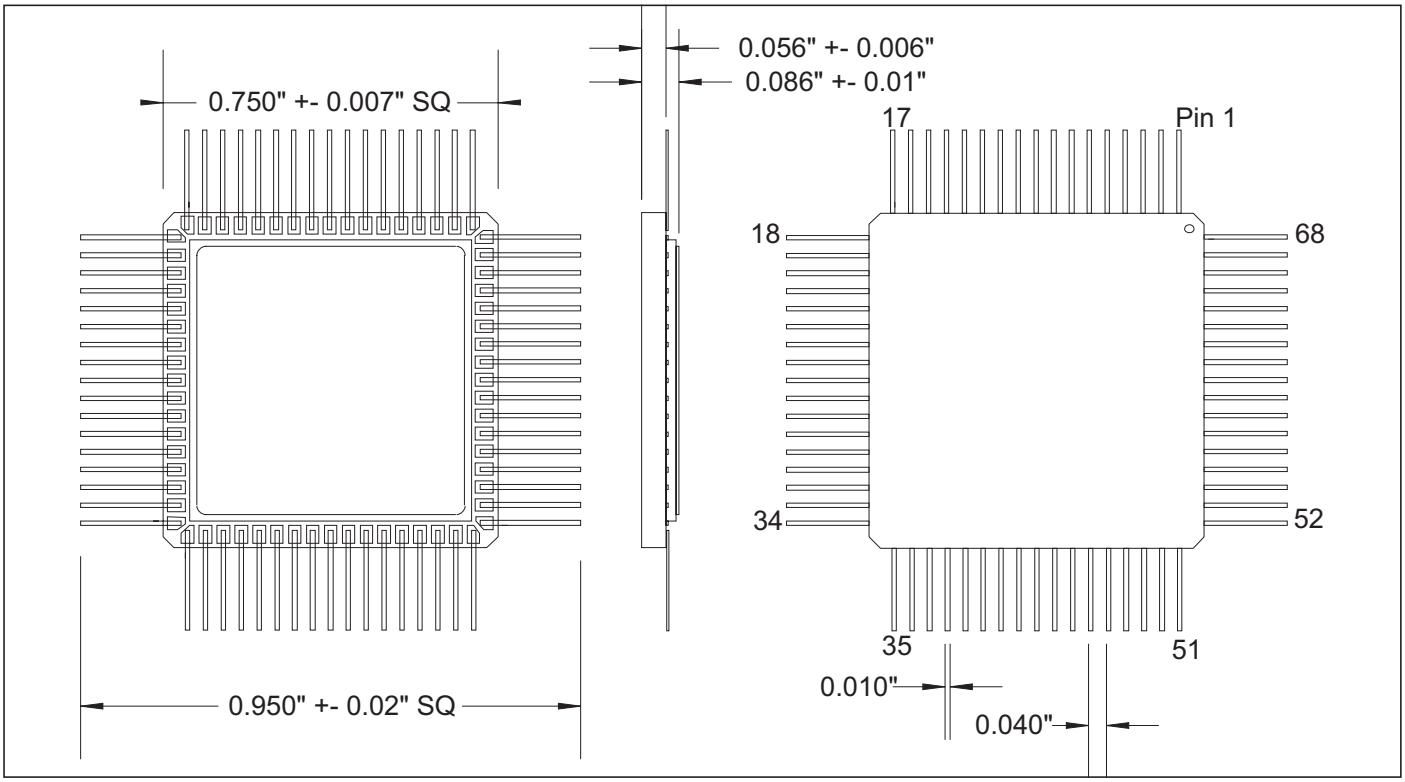


Figure 22. *Package with Straight Leads (68AB)*

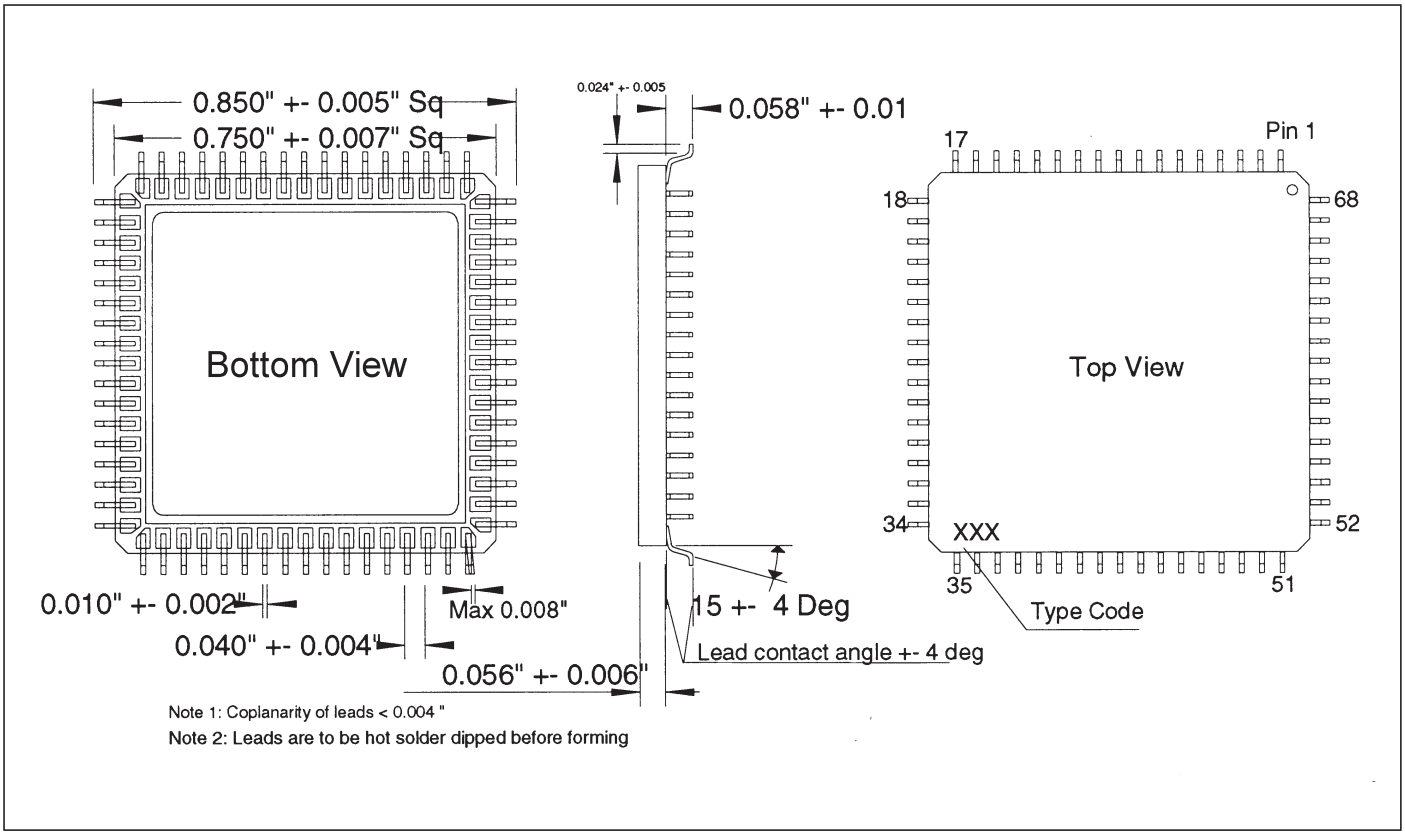


Figure 23. *Package with Gullwings Leads (68BA)*

Device Marking

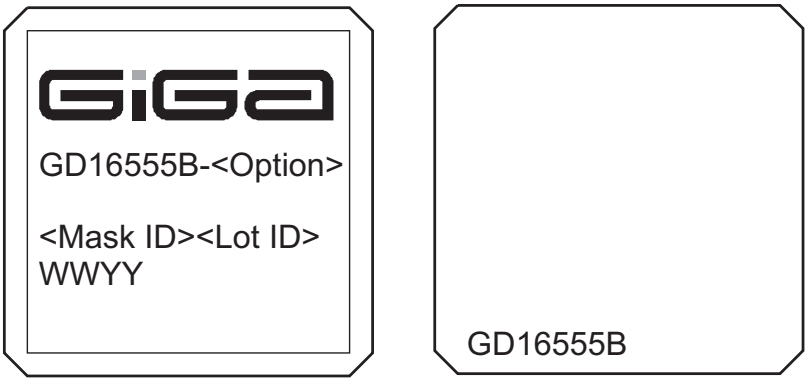


Figure 24. *Device marking, bottom and top view*

Ordering Information

To order, please specify as shown below:

Product Name:	Reference Clock:	Package Type:	Case Temperature Range:
GD16555B/155-68AB	**155 MHz**	**68 pin Straight Lead,** Multi Layer Ceramic, (MLC)	0...70°C
GD16555B/622-68AB	**622 MHz**	**68 pin Straight Lead,** Multi Layer Ceramic, (MLC)	0...70°C
GD16555B/155-68BA	**155 MHz**	**68 pin Gullwing Lead,** Multi Layer Ceramic, (MLC)	0...70°C
GD16555B/622-68BA	**622 MHz**	**68 pin Gullwing Lead,** Multi Layer Ceramic, (MLC)	0...70°C

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