

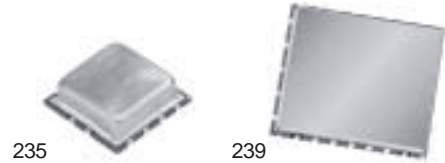
INTEGRATED FREQUENCY SYNTHESIZERS

SPLL-F, SPLH-F & OPL SERIES



FIXED FREQUENCY

Click on package to view outline drawing



FREQUENCY (MHz)	REFERENCE INPUT FREQUENCY (MHz)	DC BIAS REQUIREMENTS		Output Power (dBm/dB)	SPURIOUS REF. SIDEBAND SUPPRESSION (dBc) Typ.	HARMONIC SUPPRESSION (dBc) Min	TYPICAL PHASE NOISE dBc/Hz Offset at 10 KHz/100 KHz	PACKAGE	MODEL
		Vcc1 & 2 (Volts)	Current mA(Max)						
43.4	10	+5/+5	40	+3/±2	70	15	-97/-125	235	SPLL-43.4F
58.5	10	+5/+5	40	+3/±2	72	10	-102/-122	235	SPLL-58.5F
65.04	10	+5/+5	40	+3/±2	70	10	-95/-120	235	SPLL-65F
110.04	10	+5/+5	40	+3/±2	70	12	-95/-120	235	SPLL-110F
115	10	+5/+5	40	+3/±2	68	12	-100/-120	235	SPLL-115F
160	10	+5/+5	40	+3/±2	68	12	-100/-120	235	SPLL-160F
234	10	+5/+5	40	+3/±2	60	15	-105/-125	235	SPLL-234F
320	10	+5/+5	40	+3/±2	68	12	-100/-120	235	SPLL-320F
336	10	+5/+5	40	+3/±2	60	15	-100/-120	235	SPLL-336F
387	10	+5/+5	40	+3/±2	70	15	-97/-125	235	SPLL-387F
472.77	32.64	+5/+5	40	+3/±2	68	10	-98/-118	235	SPLL-472F
840	10	+5/+5	40	+3/±2	70	10	-98/-118	235	SPLL-840F
890	10	+5/+5	40	+3/±2	70	10	-98/-118	235	SPLL-890F
1110	10	+5/+5	40	+3/±2	70	10	-98/-118	235	SPLH-1110F
1160	10	+5/+5	40	+3/±2	70	10	-98/-118	235	SPLH-1160F
1550.4	32.64	+5/+5	40	+3/±2	65	10	-97/-117	235	SPLH-1550F
1790	10	+5/+5	40	+3/±2	65	10	-95/-115	235	SPLH-1790F
1980	10	+5/+5	40	+3/±2	65	10	-95/-115	235	SPLH-1980F
2023.17	32.64	+5/+5	40	+3/±2	65	10	-95/-115	235	SPLH-2023F
2249.8	14	+5/+5	40	+3/±2	60	10	-90/-110	235	SPLH-2249.8F
2250	14	+5/+5	40	+3/±2	60	10	-90/-110	235	SPLH-2250F
2491.75	24.9175	+5/+5	40	+3/±2	60	10	-88/-110	235	SPLH-2491F
3200	10	+5/+5	40	-12/±2.5	60	10****	-95/-116	235	SPLH-3200F
75	5	+5/+12	250	+7/±2	75	10	-110/-130	239	OPL-S-75
120	10	+5/+12	250	+7/±2	75	10	-110/-130	239	OPL-S-120
200	10	+5/+12	250	+7/±2	75	10	-110/-130	239	OPL-S-200
230	10	+5/+12	250	+10/±2	75	10	-110/-130	239	OPL-S-230
250	5	+5/+12	250	+10/±2	75	10	-106/-130	239	OPL-S-250
570	10	+5/+12	250	+7/±2	75	10	-105/-125	239	OPL-S-570
940	5	+5/+12	250	+10/±2	75	10	-95/-125	239	OPL-S-940
1456	14	+5/+8.5	250	+5/±2.5	70	10	-96/-120	239	OPL-S-1456

COMMON SPECIFICATIONS

Output Impedance: 50 ohms

Reference Input Voltage(SPLL-F series): 0.5 to 2.5 V p-p

Reference Input Voltage(OPL series): 10 dBm (±3 dB)

**** Also Applies to Sub-harmonic Rejection

Operating Temperature: -20°C to +70°C

Contact the factory for other frequencies.

PIN-OUT TABLE

RF Out	Vcc1	Vcc2	F _{ref} In	Lock Detect Output	Ground	Package Style
13	12	16	8	9	All others	235
4	6	8	22	16	All others except 2	239

For pin location and package outline drawings, see back pages.

