

Preliminary 256K x 18 & 128K x 36 Standard Write SRAM

Features

- 256K x 18 and 128K x 36 organizations
- CMOS technology
- Synchronous pipeline mode of operation with standard write
- Single Clock compatible with LVTTL levels
- +3.3V power supply. Separate output power supply and ground
- Registered addresses, write enables, synchronous select, and data ins
- Common I/O AND LVTTL I/O compatible
- Registered outputs
- Asynchronous Output Enable and Power Down inputs
- Boundary Scan using limited set of JTAG 1149.1 functions
- Byte Write capability and Global Write Enable
- 7 x 17 Bump Ball Grid Array package with SRAM JEDEC Standard Pinout and Boundary Scan order.

Description

IBM0418BSLAC and IBM0436BSLAC (Rev C part numbers) are 4Mb high performance CMOS Synchronous Static Random Access Memories which operate in Pipeline Mode. These are versatile, wide I/O SRAMs which achieve 7ns cycle times. K clock is used to initiate the read/write operation and all internal operations are self-timed. At the rising edge of the K Clock, all Addresses, Write-Enables, Sync

Select, and Data Ins are registered internally. Data Outs are updated from output registers off the next rising edge of the K Clock. Data Ins are registered in the same cycle as the write controls. These devices operate with a +3.3V power supply and have an optional +2.5V or 3.3V output power supply, and are compatible with LVTTL I/O interfaces.

x36 BGA Bump Layout (Top View)

	1	2	3	4	5	6	7
A	V _{DDQ}	SA5	SA7	NC	SA16	SA14	V _{DDQ}
B	NC	NC	SA8	NC	SA11	NC	NC
C	NC	SA6	SA9	V _{DD}	SA10	SA15	NC
D	DQc18	DQc19	V _{SS}	NC	V _{SS}	DQb10	DQb9
E	DQc20	DQc21	V _{SS}	\overline{SS}	V _{SS}	DQb12	DQb11
F	V _{DDQ}	DQc22	V _{SS}	\overline{G}	V _{SS}	DQb13	V _{DDQ}
G	DQc23	DQc24	\overline{SBWc}	NC	\overline{SBWb}	DQb15	DQb14
H	DQc25	DQc26	V _{SS}	NC	V _{SS}	DQb17	DQb16
J	V _{DDQ}	V _{DD}	NC	V _{DD}	NC	V _{DD}	V _{DDQ}
K	DQd34	DQd35	V _{SS}	K	V _{SS}	DQa8	DQa7
L	DQd32	DQd33	\overline{SBWd}	NC	\overline{SBWa}	DQa6	DQa5
M	V _{DDQ}	DQd31	V _{SS}	\overline{SW}	V _{SS}	DQa4	V _{DDQ}
N	DQd29	DQd30	V _{SS}	SA0	V _{SS}	DQa3	DQa2
P	DQd27	DQd28	V _{SS}	SA1	V _{SS}	DQa1	DQa0
R	NC	SA4	M1*	V _{DD}	M2*	SA12	NC
T	NC	NC	SA3	SA2	SA13	NC	ZZ
U	V _{DDQ}	TMS	TDI	TCK	TDO	NC	V _{DDQ}

Note: * M1 and M2 are clock mode pins. For this application, M1 and M2 need to connect to V_{SS} and V_{DD}, respectively.

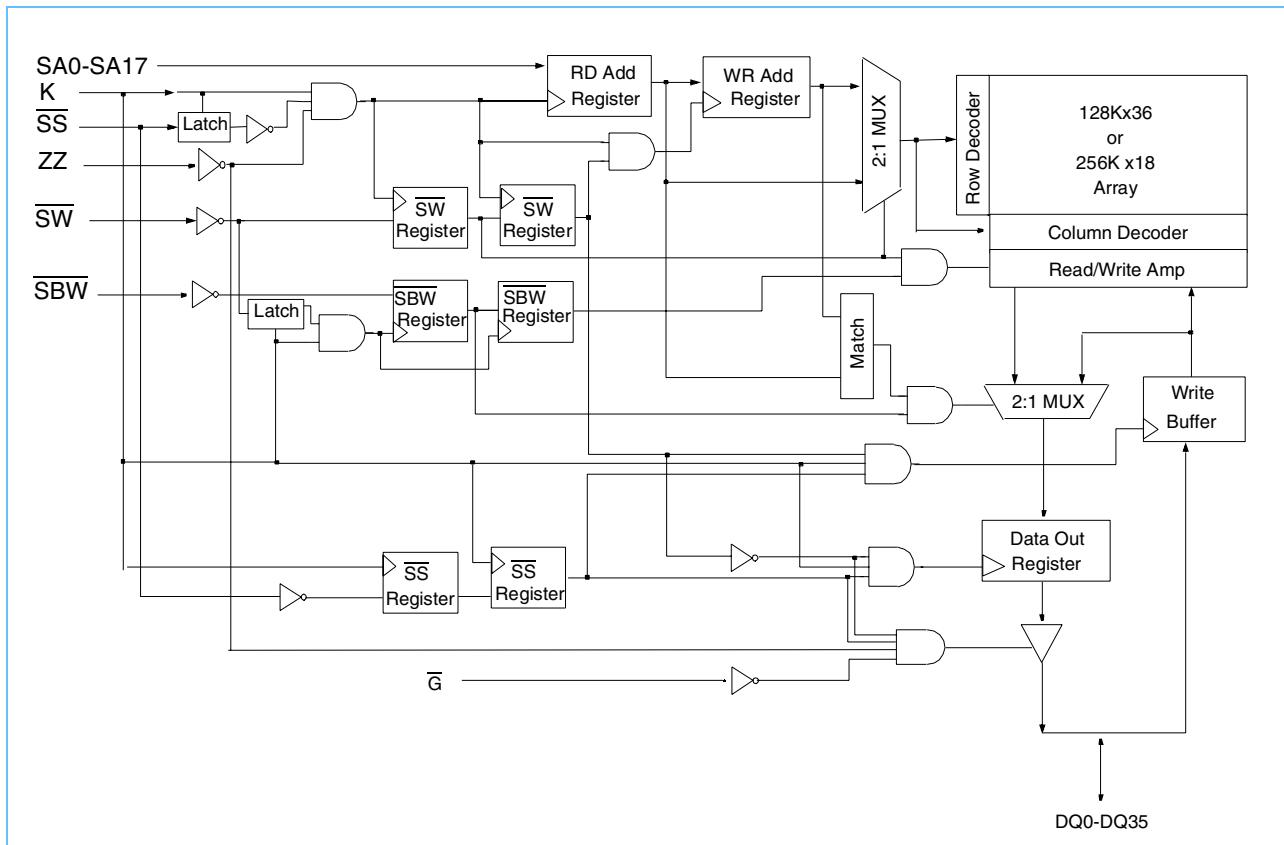
x18 BGA Bump Layout (Top View)

	1	2	3	4	5	6	7
A	V _{DDQ}	SA5	SA7	NC	SA16	SA14	V _{DDQ}
B	NC	NC	SA8	NC	SA11	NC	NC
C	NC	SA6	SA9	V _{DD}	SA10	SA15	NC
D	DQb9	NC	V _{SS}	NC	V _{SS}	DQa1	NC
E	NC	DQb12	V _{SS}	\overline{SS}	V _{SS}	NC	DQa2
F	V _{DDQ}	NC	V _{SS}	\overline{G}	V _{SS}	DQa4	V _{DDQ}
G	NC	DQb15	\overline{SBWb}	NC	V _{SS}	NC	DQa5
H	DQb16	NC	V _{SS}	NC	V _{SS}	DQa8	NC
J	V _{DDQ}	V _{DD}	NC	V _{DD}	NC	V _{DD}	V _{DDQ}
K	NC	DQb17	V _{SS}	K	V _{SS}	NC	DQa7
L	DQb14	NC	V _{SS}	NC	\overline{SBWa}	DQa6	NC
M	V _{DDQ}	DQb13	V _{SS}	\overline{SW}	V _{SS}	NC	V _{DDQ}
N	DQb11	NC	V _{SS}	SA0	V _{SS}	DQa3	NC
P	NC	DQb10	V _{SS}	SA1	V _{SS}	NC	DQa0
R	NC	SA4	M1	V _{DD}	M2	SA13	NC
T	NC	SA2	SA3	NC	SA17	SA12	ZZ
U	V _{DDQ}	TMS	TDI	TCK	TDO	NC	V _{DDQ}

Note: * M1 and M2 are clock mode pins. For this application, M1 and M2 need to connect to V_{SS} and V_{DD}, respectively.

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Pin Description

SA0-SA17	Address Input	TDO	IEEE 1149 Test Output
DQa,DQb,DQc,DQd	Data I/O (DQ0-8,DQ9-17,DQ18-26,DQ27-35)	\overline{SS}	Synchronous Select
K	Clock (LVTTTL Compatible)	M1, M2	Clock Mode Inputs
\overline{SW}	Write Enable, global	V_{DD}	Power Supply (+3.3V)
\overline{SBWa}	Write Enable, Byte a (DQ0 to DQ8)	V_{SS}	Ground
\overline{SBWb}	Write Enable, Byte b (DQ9 to DQ17)	V_{DDQ}	Output Power Supply
\overline{SBWc}	Write Enable, Byte c (DQ18 to DQ26)	\overline{G}	Asynchronous Output Enable
\overline{SBWd}	Write Enable, Byte d (DQ27 to DQ35)	ZZ	Asynchronous Sleep Mode
TMS,TDI,TCK	IEEE 1149 Test Inputs	NC	No Connect

Block Diagram

Ordering Information

Part Number	Die Revision	Organization	Speed	Leads
IBM04184BSLAC-7	C	256K x 18	3.5ns Access / 7ns Cycle	7 x 17 BGA
IBM04364BSLAC-7	C	128K x 36	3.5ns Access / 7ns Cycle	7 x 17 BGA

SRAM Features

Standard Write

In Standard Write function, write data must be registered in the same cycle as addresses and controls.

Mode Control

Mode control pins M1 and M2 are used to select four different JEDEC standard read protocols. This SRAM only supports the single clock pipeline (M1 = V_{SS} , M2 = V_{DD}) protocol. Mode control inputs must be set with power up and must not change during SRAM operation.

Power Down Mode

Power Down mode, or "Sleep mode," is accomplished by switching asynchronous signal ZZ high. When powering the SRAM down, inputs must be dropped first and V_{DDQ} must be dropped before or simultaneously with V_{DD} .

Power-Up Requirements

To guarantee the optimum internally regulated supply voltage, the SRAM requires 4 μ s of power-up time after V_{DD} reaches its operating range. V_{DD} must be powered up before or simultaneously with V_{DDQ} . Inputs must be powered up after V_{DDQ} . V_{DDQ} should not exceed V_{DD} supply by more than 0.4V during power up.

Sleep Mode Operation

Sleep mode is a low power mode initiated by bringing the asynchronous ZZ pin HIGH. During Sleep mode, all other inputs are ignored and outputs are brought to a High-Z state. Sleep mode current and output High Z are guaranteed after the specified sleep mode enable time. During Sleep mode, the array data contents are preserved. Sleep mode must not be initiated until after all pending operations have completed, as any pending operation is not guaranteed to properly complete after Sleep mode is initiated. Sense amp data is lost. Normal operation can be resumed by bringing ZZ low, but only after specified Sleep mode recovery time.



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Clock Truth Table

K	ZZ	\overline{SS}	\overline{SW}	\overline{SBWa}	\overline{SBWb}	\overline{SBWc}	\overline{SBWd}	DQ (n)	DQ (n+1)	Mode
L→H	L	L	H	X	X	X	X	X	D _{OUT} 0-35	Read Cycle All Bytes
L→H	L	L	L	L	H	H	H	X	D _{IN} 0-8	Write Cycle 1st Byte
L→H	L	L	L	H	L	H	H	X	D _{IN} 9-17	Write Cycle 2nd Byte
L→H	L	L	L	H	H	L	H	X	D _{IN} 18-26	Write Cycle 3rd Byte
L→H	L	L	L	H	H	H	L	X	D _{IN} 27-35	Write Cycle 4th Byte
L→H	L	L	L	L	L	L	L	X	D _{IN} 0-35	Write Cycle All Bytes
L→H	L	L	L	H	H	H	H	X	High-Z	Abort Write Cycle
L→H	L	H	X	X	X	X	X	X	High-Z	Deselect Cycle
X	H	X	X	X	X	X	X	High-Z	High-Z	Sleep Mode

Output Enable Truth Table

Operation	\overline{G}	DQ
Read	L	D _{OUT} 0-35
Read	H	High-Z
Sleep (ZZ=H)	X	High-Z
Write (\overline{SW} =L)	X	High-Z
Deselect (\overline{SS} =H)	X	High-Z

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units	Notes
V _{DD}	Power Supply Voltage	-0.5 to 3.9	V	1
V _{DDQ}	Output Power Supply Voltage	V _{DD}	V	1
V _{IN}	Input Voltage	-0.5 to V _{DD} +0.5	V	1
V _{OUT}	Output Voltage	-0.5 to V _{DD} +0.5	V	1
T _J	Operating Temperature	0 to +110	°C	1
T _{STG}	Storage Temperature	-55 to +125	°C	1
I _{OUT}	Short Circuit Output Current	25	mA	1

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions ($T_A = 0$ to $+85^\circ\text{C}$)

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
V_{DD}	Supply Voltage	3.135	3.3	3.47	V	1
V_{DDQ}	OCD Supply Voltage	2.375	2.5	3.47	V	1
V_{IH}	Input High Voltage	2.0	—	$V_{DD}+0.3$	V	1, 2, 4
V_{IL}	Input Low Voltage	-0.3	—	0.8	V	1, 3, 4
I_{OUT}	Output Current	—	5	8	mA	

1. All voltages referenced to V_{SS} . All V_{DD} , V_{DDQ} and V_{SS} pins must be connected.
2. $V_{IH}(\text{Max})\text{DC} = V_{DD} + 0.3 \text{ V}$, $V_{IH}(\text{Max})\text{AC} = V_{DD} + 1.5 \text{ V}$ (pulse width $\leq 4.0\text{ns}$).
3. $V_{IL}(\text{Min})\text{DC} = -0.3 \text{ V}$, $V_{IL}(\text{Min})\text{AC} = -1.5 \text{ V}$ (pulse width $\leq 4.0\text{ns}$).
4. Must be powered up after V_{DDQ} .

Capacitance ($T_A = 0$ to $+85^\circ\text{C}$, $V_{DD} = 3.3\text{V} \pm 5\%$, $f = 1\text{MHz}$)

Symbol	Parameter	Test Condition	Max.	Units
C_{IN}	Input Capacitance	$V_{IN} = 0\text{V}$	4	pF
C_{OUT}	Data I/O Capacitance (DQ0-DQ35)	$V_{OUT} = 0\text{V}$	7	pF

DC Electrical Characteristics ($T_A = 0$ to $+85^\circ\text{C}$, $V_{DD} = V_{DDQ} = 3.3\text{V} \pm 5\%$)

Symbol	Parameter	Min.	Max.	Units	Notes
I_{DD7}	Average Power Supply Operating Current - x18 ($I_{OUT} = 0$, $V_{IN} = V_{IH}$ or V_{IL} , ZZ & SS = V_{IL})	—	400	mA	1
I_{DD7}	Average Power Supply Operating Current - x36 ($I_{OUT} = 0$, $V_{IN} = V_{IH}$ or V_{IL} , ZZ & SS = V_{IL})	—	450	mA	1
I_{SBZZ}	Power Supply Standby Current (ZZ = V_{IH} , All other inputs = V_{IH} or V_{IL} , $I_{OUT} = 0$)	—	120	mA	1
I_{SBSS}	Power Supply Standby Current ($\overline{\text{SS}} = V_{IH}$, ZZ = V_{IL} , All other inputs = V_{IH} or V_{IL} , $I_{OUT} = 0$)	—	150	mA	1
I_{LI}	Input Leakage Current, any input ($V_{IN} = V_{SS}$ or V_{DD})	—	+1	μA	
I_{LO1} I_{LO2}	Output Leakage Current ($V_{OUT} = V_{SS}$ to 3.0V, DQ in High-Z) ($V_{OUT} = 3.0$ to V_{DD} , DQ in High-Z)	— -	+6 +100	μA	
V_{OH}	Output High "H" Level Voltage ($I_{OH} = -8\text{mA}$ @ 2.4V)	2.4	—	V	
V_{OL}	Output Low "L" Level Voltage ($I_{OL} = +8\text{mA}$ @ 0.4V)	—	0.4	V	
V_{OH}	Output High "H" Level Voltage ($I_{OH} = -8\text{mA}$ @ 2.4V) $V_{DDQ} = 2.5\text{V}$	1.6	—	V	
V_{OL}	Output Low "L" Level Voltage ($I_{OL} = +8\text{mA}$ @ 0.4V) $V_{DDQ} = 2.5\text{V}$	—	0.4	V	

1. I_{OUT} = Chip Output Current. I_{DD7} refers to 7ns cycle time.

PBGA Thermal Characteristics

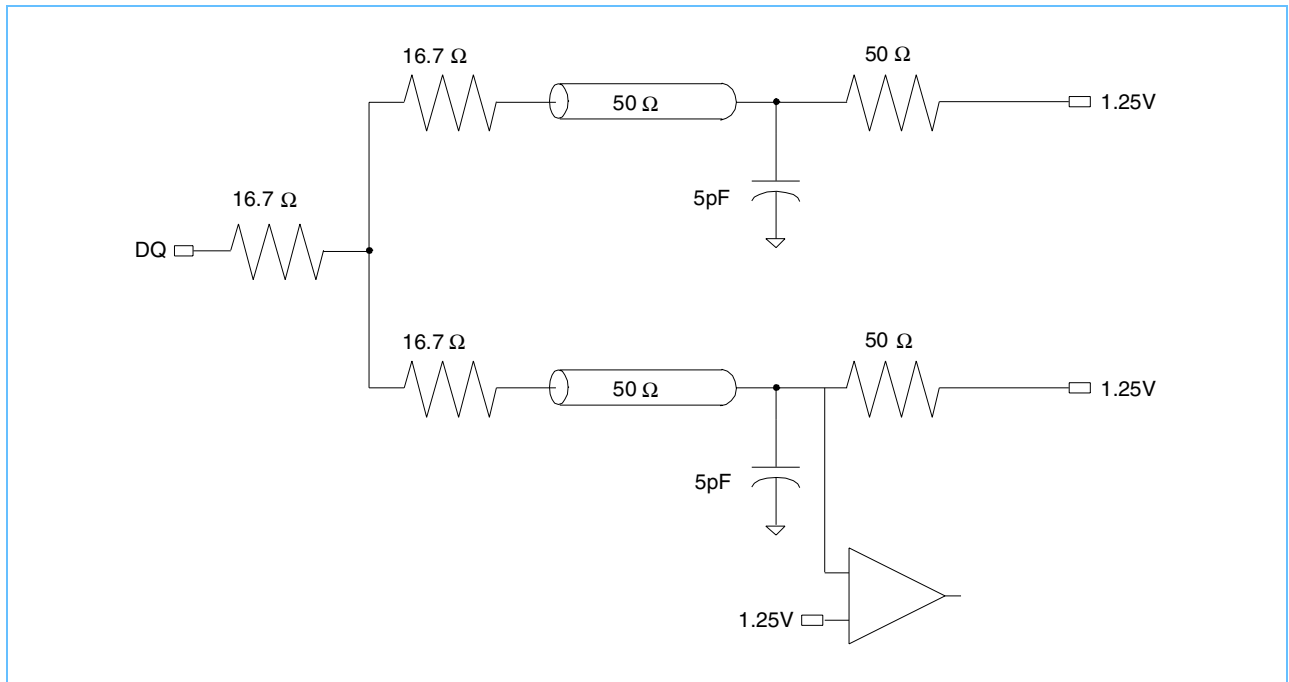
Symbol	Parameter	Rating	Units
R θ JC	Thermal Resistance Junction to Case	1	$^{\circ}$ C/W

AC Test Conditions ($T_A = 0$ to $+85^{\circ}$ C, $V_{DD} = 3.3V \pm 10/-5\%$, $V_{DDQ} = 2.5V \pm 5\%$)

Symbol	Parameter	Conditions	Units	Notes
V_{IH}	Input High Level	2.25	V	
V_{IL}	Input Low Level	0.25	V	
T_R	Input Rise Time	1.0	ns	
T_F	Input Fall Time	1.0	ns	
$T_{R-Clock}$	Clock Input Rise Time	1.0	ns	
$T_{F-Clock}$	Clock Input Fall Time	1.0	ns	
	Output Load Conditions			1
T_{REF}	Input and Output Timing Reference Level	1.25	V	

1. See AC Test Loading on page 7.

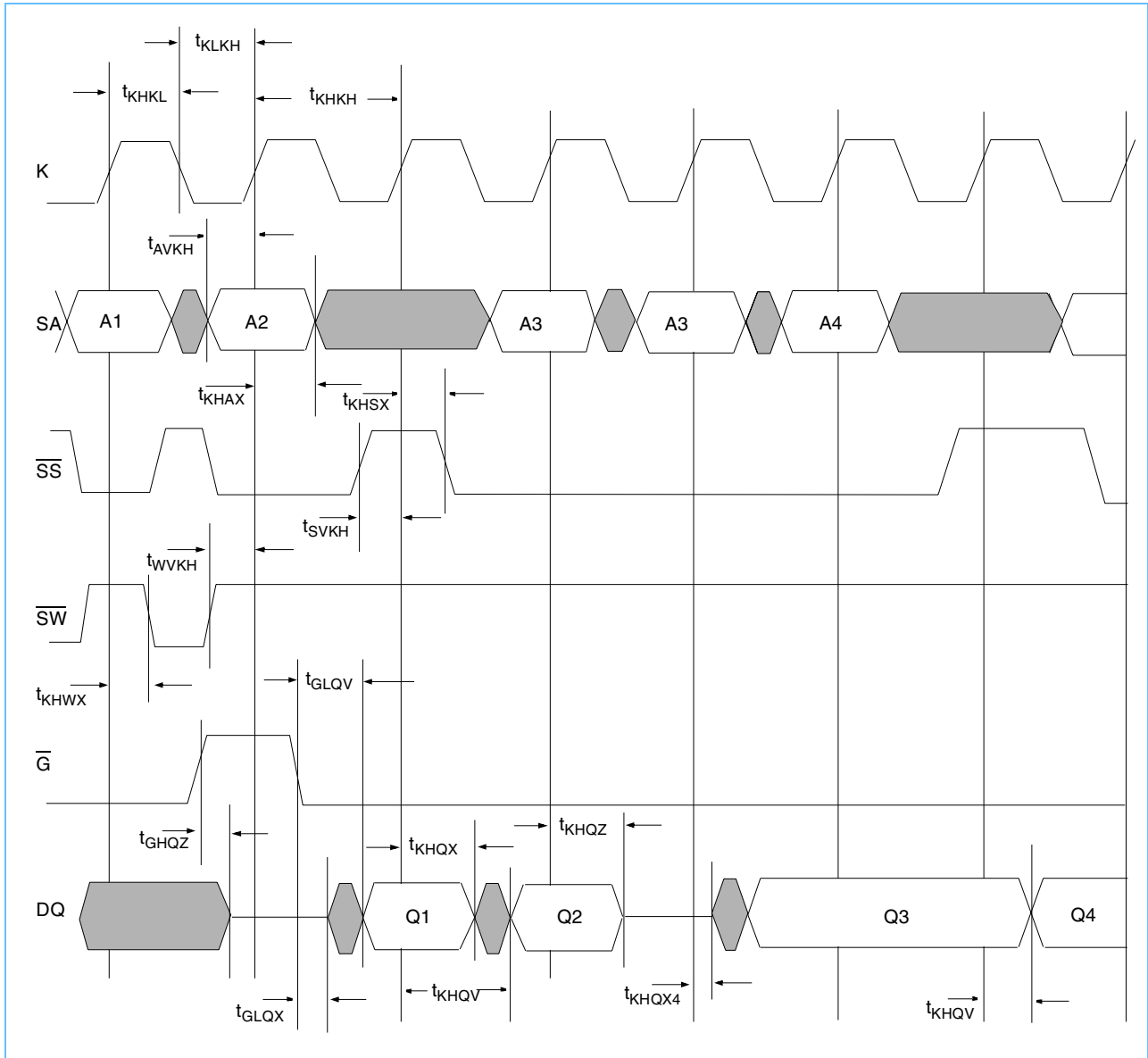
AC Test Loading



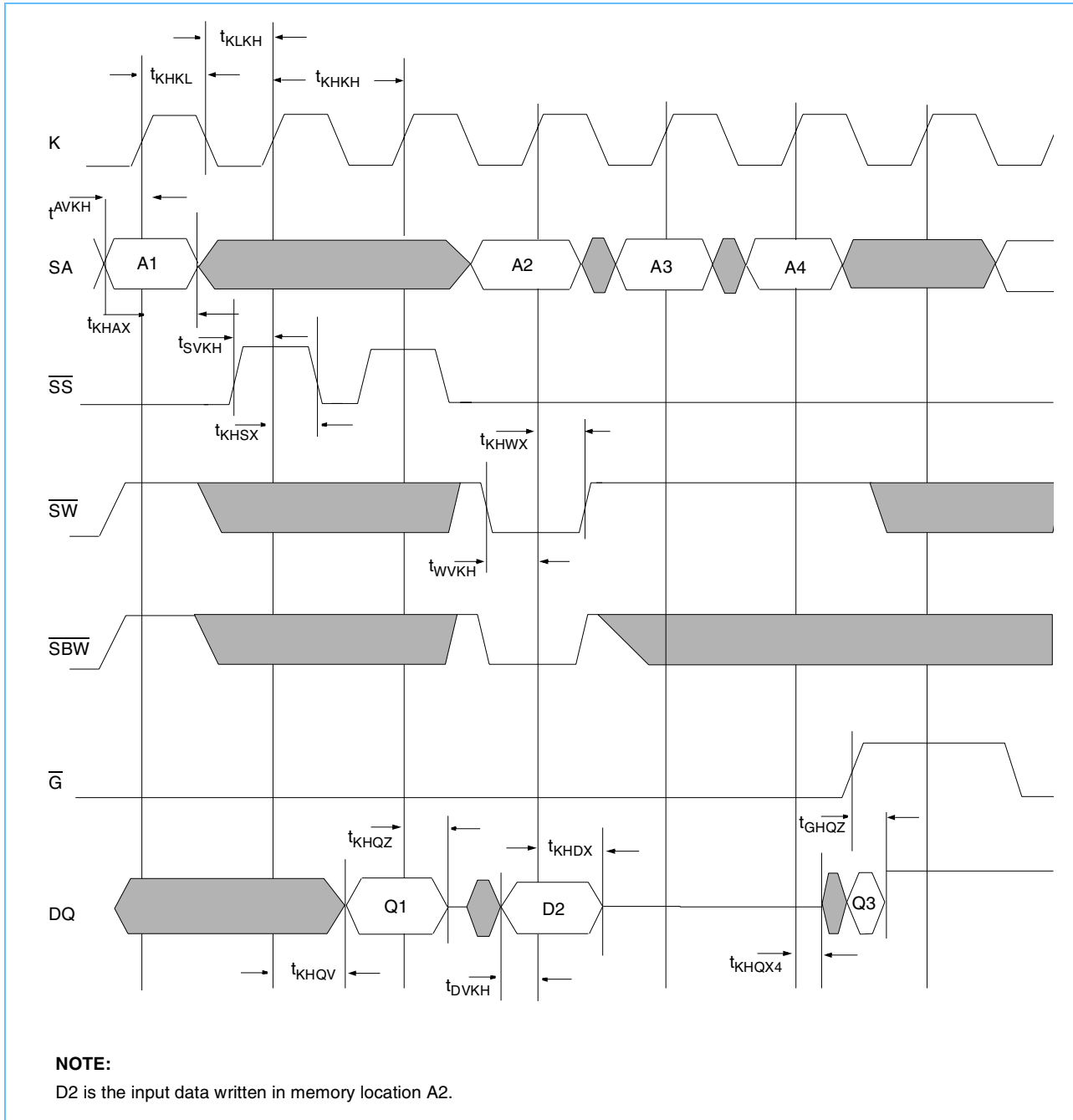
AC Characteristics ($T_A = 0$ to $+85^\circ\text{C}$, $V_{DD} = 3.3\text{V} +10/-5\%$, $V_{DDQ} = 2.5\text{V} \pm 5\%$)

Symbol	Parameter	Min.	Max.	Units	Notes
t_{KHKH}	Cycle Time	7.0	—	ns	
t_{KHKL}	Clock High Pulse Width	1.5	—	ns	
t_{KLKH}	Clock Low Pulse Width	1.5	—	ns	
t_{KHQV}	Clock to Output Valid	—	3.5	ns	1
t_{AVKH}	Address Setup Time	0.5	—	ns	
t_{KHAX}	Address Hold Time	1.0	—	ns	
t_{SVKH}	Sync Select Setup Time	0.5	—	ns	
t_{KHSX}	Sync Select Hold Time	1.0	—	ns	
t_{WVKH}	Write Enables Setup Time	0.5	—	ns	
$t_{KH WX}$	Write Enables Hold Time	1.0	—	ns	
t_{DVKH}	Data In Setup Time	0.5	—	ns	
t_{KHDX}	Data In Hold Time	1.0	—	ns	
t_{KHQX}	Data Out Hold Time	1.0	—	ns	1
t_{KHQZ}	Clock High to Output High-Z	—	3.5	ns	1, 2
t_{KHQX4}	Clock High to Output Active	0.5	—	ns	1, 2
t_{GHQZ}	Output Enable to High-Z	—	3.5	ns	1, 2
t_{GLQX}	Output Enable to Low-Z	0.5	—	ns	1, 2
t_{GLQV}	Output Enable to Output Valid	—	3.5	ns	1
t_{ZZR}	Sleep Mode Recovery Time	7	—	ns	3
t_{ZZE}	Sleep Mode Enable Time	—	7	ns	3
1. See AC Test Loading on page 7. 2. Verified by design and tested without guardband. 3. This specification is for No Data Retention. For data integrity at least 200ns of Recovery Time is recommended coupled with a 0.5ns set-up time around K clock.					

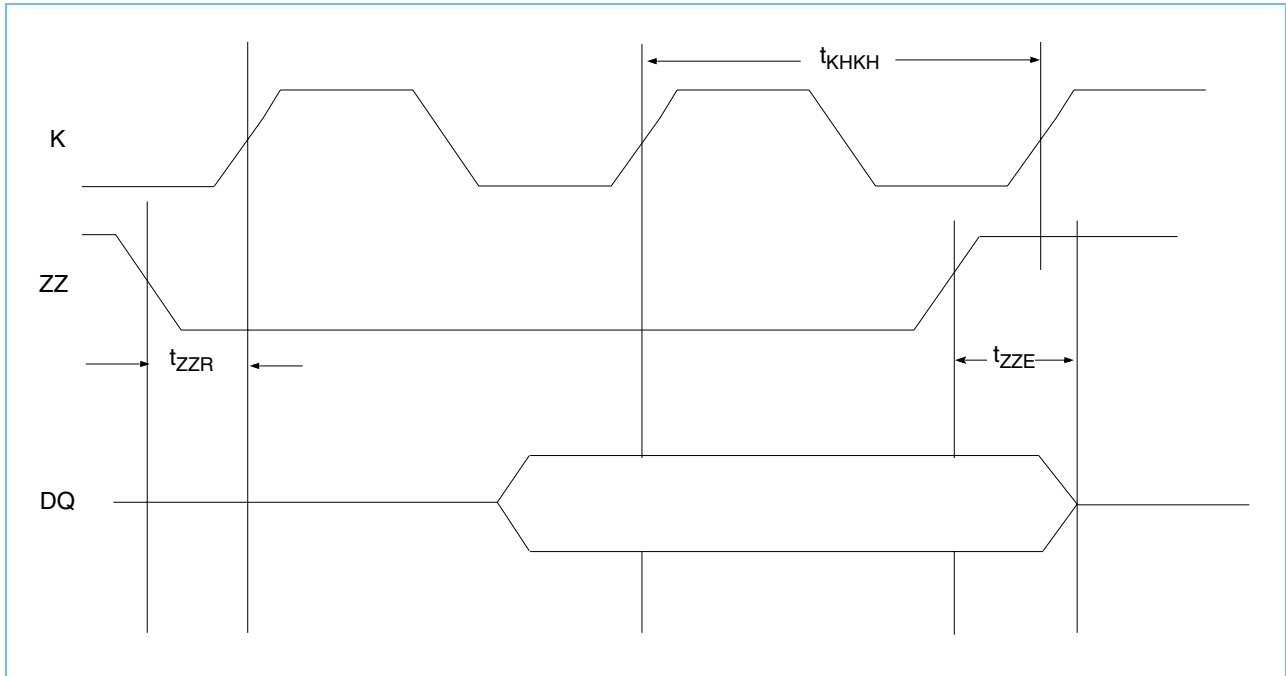
Read and Deselect Cycles



Read Write Cycles



Sleep Mode



IEEE 1149.1 TAP and Boundary Scan

The SRAM provides a limited set of JTAG functions intended to test the interconnection between SRAM I/Os and printed circuit board traces or other components. There is no multiplexer in the path from I/O pins to the RAM core.

In conformance with IEEE std. 1149.1, the SRAM contains a TAP controller, Instruction register, Boundary Scan register, Bypass register and ID register.

The TAP controller has a standard 16-state machine that resets internally upon power-up, therefore, TRST signal is not required.

Signal List

- TCK: Test Clock
- TMS: Test Mode Select
- TDI: Test Data In
- TDO: Test Data Out

Caution: TCK,TMS,TDI must be tied down, even when JTAG is not used. TCK tied off will not allow any data to be clocked in, however.

JTAG Recommended DC Operating Conditions ($T_A=0$ to 85°C)

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
V_{IH1}	JTAG Input High Voltage	2.2	—	$V_{DD}+0.3$	V	1
V_{IL1}	JTAG Input Low Voltage	-0.3	—	0.8	V	1
V_{OH1}	JTAG Output High Level	2.4	—	—	V	1, 2
V_{OL1}	JTAG Output Low Level	—	—	0.4	V	1, 3

1. All JTAG Inputs/Outputs are LVTTTL Compatible only.
2. $I_{OH1} = -8\text{mA}$ at 2.4V.
3. $I_{OL1} = +8\text{mA}$ at 0.4V.

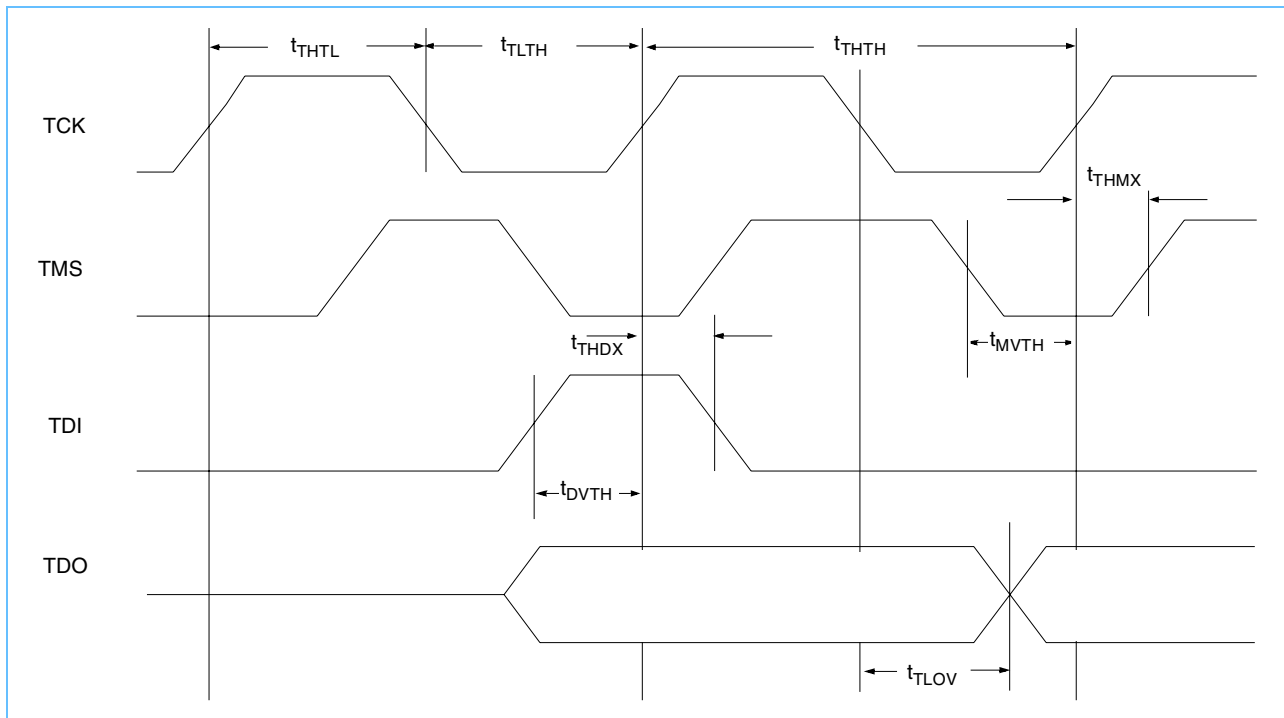
JTAG AC Test Conditions ($T_A=0$ to $+85^\circ\text{C}$, $V_{DD}= 3.3\text{V} +10/-5\%$)

Symbol	Parameter	Conditions	Units	Notes
V_{IH1}	Input Pulse High Level	3.0	V	
V_{IL1}	Input Pulse Low Level	0.0	V	
T_{R1}	Input Rise Time	2.0	ns	
T_{F1}	Input Fall Time	2.0	ns	
	Input and Output Timing Reference Level	1.5	V	1

1. See AC Test Loading on page 7.

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JTAG AC Characteristics ($T_A = 0$ to $+85^\circ\text{C}$, $V_{DD} = 3.3\text{V} \pm 10\%/-5\%$)

Symbol	Parameter	Min.	Max.	Units	Notes
t_{THTH}	TCK Cycle Time	20	—	ns	
t_{THTL}	TCK High Pulse Width	7	—	ns	
t_{TLTH}	TCK Low Pulse Width	7	—	ns	
t_{MVTH}	TMS Setup	4	—	ns	
t_{THMX}	TMS Hold	4	—	ns	
t_{DVTH}	TDI Setup	4	—	ns	
t_{THDX}	TDI Hold	4	—	ns	
t_{TLOV}	TCK Low to Valid Data	—	7	ns	

JTAG Timing Diagram




Scan Register Definition

Register Name	Bit Size x18	Bit Size x36
Instruction	3	3
Bypass	1	1
ID	32	32
Boundary Scan *	51	70

* The Boundary Scan chain consists of the following bits:

- 36 or 18 bits for Data Inputs depending on x18 or x36 configuration
- 17 bits for SA0 - SA16 for x36, 18 bits for SA0 - SA17 for x18
- 4 bits for SBW_a - SBW_d in x36, 2 bits for SBW_a and SBW_b in x18
- 8 bits for K, \bar{K} , SS, \bar{G} , SW, ZZ, M1 and M2
- 5 bits for Place Holders

* K and \bar{K} clocks connect to a differential receiver that generates a single-ended clock signal. This signal and its inverted value are used for Boundary Scan sampling.

ID Register Definition

Part	Field Bit Number and Description				
	Revision Number (31:28)	Device Density and Configuration (27:18)	Vendor Definition (17:12)	Manufacture JEDEC Code (11:1)	Start Bit (0)
256K x 18	0001	011 100 1011	001110	000 101 001 00	1
128K x 36	0001	011 010 1100	001110	000 101 001 00	1

Instruction Set

Code	Instruction	Notes
000	SAMPLE-Z	1
001	IDCODE	2
010	SAMPLE-Z	1
011	PRIVATE	5
100	SAMPLE	4
101	PRIVATE	5
110	PRIVATE	5
111	BYPASS	3

1. Places DQs in High-Z in order to sample all input data regardless of other SRAM inputs.
2. TDI is sampled as an input to the first ID register to allow for the serial shift of the external TDI data.
3. BYPASS register is initiated to V_{SS} when BYPASS instruction is invoked. The BYPASS register also holds the last serially loaded TDI when exiting the Shift DR state.
4. SAMPLE instruction does not place DQs in High-Z and does not affect SRAM operation.
5. This instruction is reserved for the exclusive use of IBM. Invoking this instruction may cause improper SRAM functionality.

List of IEEE 1149.1 Standard Violations:

- 7.2.1.b, e
- 7.7.1.a-f
- 10.1.1.b, e
- 10.7.1.a-d
- 6.1.1.d



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Boundary Scan Order (x36) (PH =Place Holder)

Exit Order	Signal	Bump #	Exit Order	Signal	Bump #	Exit Order	Signal	Bump #
1	M2	5R	25	DQ13	6F	49	DQ26	2H
2	SA1	4P	26	DQ11	7E	50	DQ25	1H
3	SA2	4T	27	DQ12	6E	51	\overline{SBWc}	3G
4	SA12	6R	28	DQ9	7D	52	ZQ= 0 (PH)	4D
5	SA13	5T	29	DQ10	6D	53	SS	4E
6	ZZ	7T	30	SA14	6A	54	C=0 ²	4G
7	DQ1	6P	31	SA15	6C	55	C=1 ²	4H
8	DQ0	7P	32	SA10	5C	56	SW	4M
9	DQ3	6N	33	SA16	5A	57	\overline{SBWd}	3L
10	DQ2	7N	34	PH ¹	6B	58	DQ34	1K
11	DQ4	6M	35	SA11	5B	59	DQ35	2K
12	DQ6	6L	36	SA8	3B	60	DQ32	1L
13	DQ5	7L	37	PH ¹	2B	61	DQ33	2L
14	DQ8	6K	38	SA7	3A	62	DQ31	2M
15	DQ7	7K	39	SA9	3C	63	DQ29	1N
16	\overline{SBWa}	5L	40	SA6	2C	64	DQ30	2N
17	\overline{K}^3	4L	41	SA5	2A	65	DQ27	1P
18	K	4K	42	DQ19	2D	66	DQ28	2P
19	G	4F	43	DQ18	1D	67	SA3	3T
20	\overline{SBWb}	5G	44	DQ21	2E	68	SA4	2R
21	DQ16	7H	45	DQ20	1E	69	SA0	4N
22	DQ17	6H	46	DQ22	2F	70	M1	3R
23	DQ14	7G	47	DQ24	2G			
24	DQ15	6G	48	DQ23	1G			

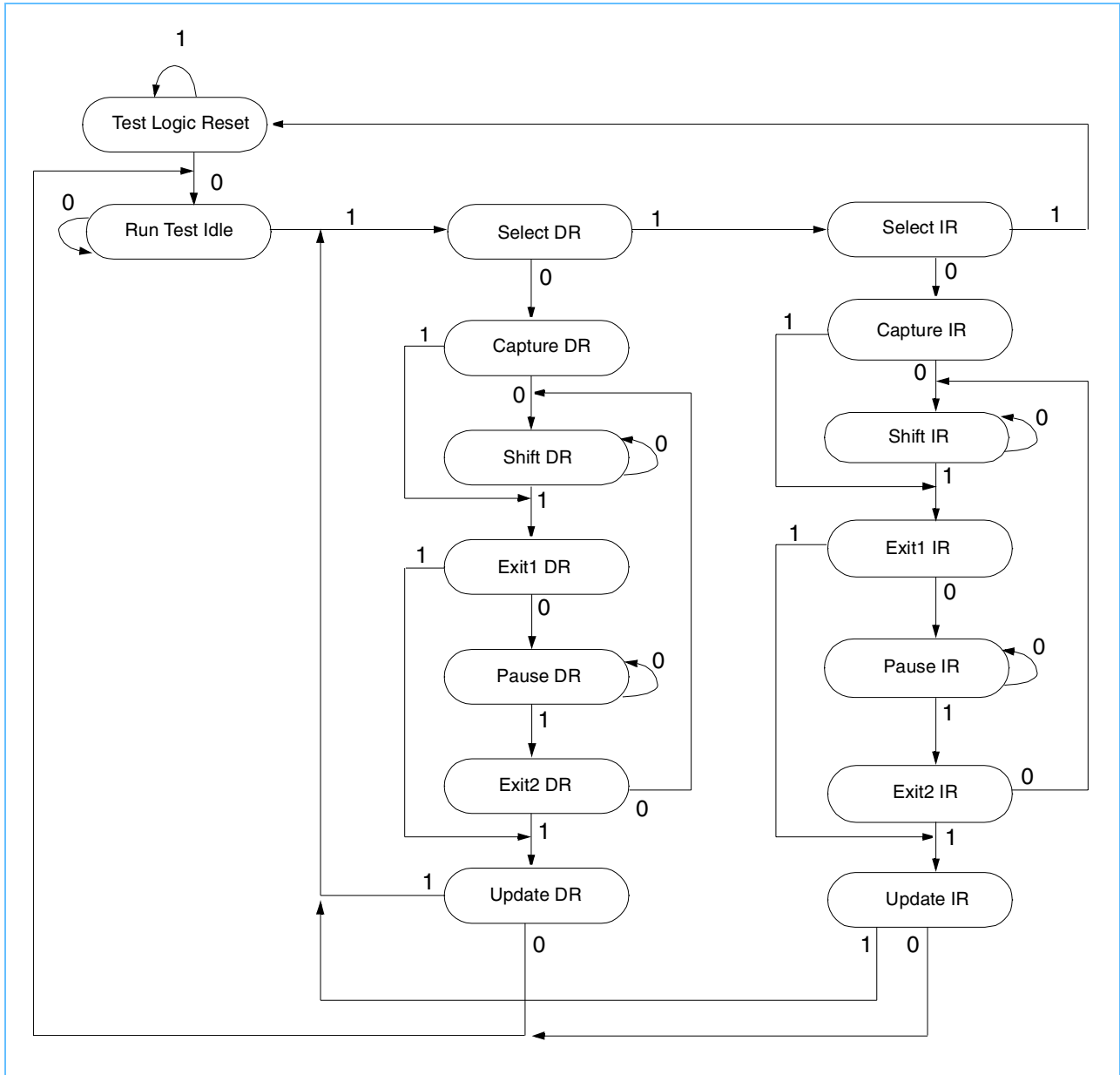
1. Input of PH register connected to V_{SS}.
2. Balls 4G and 4H are unused C Clock pins in this application.
3. \overline{K} is inverse of K.

Boundary Scan Order (x18) (PH =Place Holder)

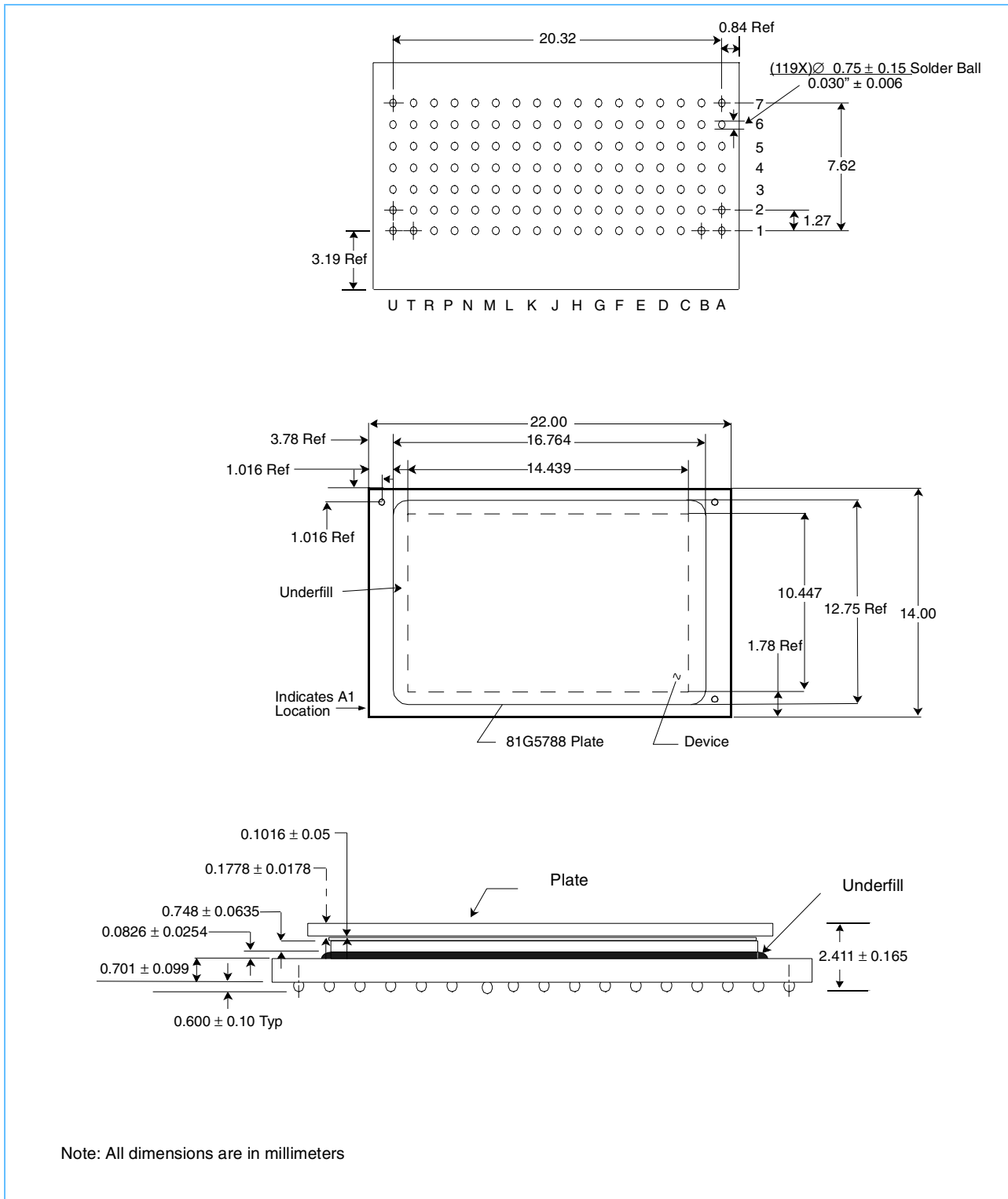
Exit Order	Signal	Bump #	Exit Order	Signal	Bump #
1	M2	5R	27	PH ¹	2B
2	SA12	6T	28	SA7	3A
3	SA1	4P	29	SA9	3C
4	SA13	6R	30	SA6	2C
5	SA17	5T	31	SA5	2A
6	ZZ	7T	32	DQ9	1D
7	DQ0	7P	33	DQ12	2E
8	DQ3	6N	34	DQ15	2G
9	DQ6	6L	35	DQ16	1H
10	DQ7	7K	36	$\overline{\text{SBWb}}$	3G
11	$\overline{\text{SBWa}}$	5L	37	ZQ= 0 (PH)	4D
12	$\overline{\text{K}}^3$	4L	38	SS	4E
13	K	4K	39	C=0 ²	4G
14	G	4F	40	C=1 ²	4H
15	DQ8	6H	41	SW	4M
16	DQ5	7G	42	DQ17	2K
17	DQ4	6F	43	DQ14	1L
18	DQ2	7E	44	DQ13	2M
19	DQ1	6D	45	DQ11	1N
20	SA14	6A	46	DQ10	2P
21	SA15	6C	47	SA3	3T
22	SA10	5C	48	SA4	2R
23	SA16	5A	49	SA0	4N
24	PH ¹	6B	50	SA2	2T
25	SA11	5B	51	M1	3R
26	SA8	3B			

1. Input of PH register connected to V_{SS}.
2. Balls 4G and 4H are unused C Clock pins in this application.
3. $\overline{\text{K}}$ is inverse of K.

TAP Controller State Machine



7 x 17 BGA Dimensions



Note: All dimensions are in millimeters



Related Documentation

The following documents provide recommendations, restrictions and limitations for the second level attach process:

[C4 SRAM Assembly Guide for Single Sided Assembly](#)

[Double Sided 4Meg Coupled Cap PBGA Card Assembly Guide](#)

Qualification information, including the scope of application conditions qualified, is available from your IBM sales representative.



Revision Log

Rev	Contents of Modification
July 18, 2000	Initial Release.
July 25, 2000	Added note #4 to Recommended DC Operating Conditions Table.