8M X 64 Bits (64MB) 144-Pin SDRAM SO-DIMM (PC100)—Preliminary

FEATURES

- PC100/Intel 1.0 Compliant
  (see *Ordering Information* for options)
- Burst Mode Operation
- Auto and self refresh capability
  (4096 cycles/64ms refresh)
- LVTTL compatible inputs and outputs
- +3.3V ± 0.3V power supply
- MRS cycle with address key programs
  - Latency (access from column address)
  - Burst Length (1, 2, 4, 8, and full page)
  - Data scramble (sequential and interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial Presence Detect with EEPROM

GENERAL DESCRIPTION

The SiliconTech SL64G6E8M4G-A10xV is a 8M x 64 bits Synchronous Dynamic RAM (SDRAM) Small-Outline Dual In-line Memory Module (SO-DIMM). The module consists of four CMOS 2M x 16 bits x 4 banks SDRAMs in 54-pin 400-mil TSOP II packages mounted on a 144-pin glass epoxy substrate. A serial EEPROM using the two pin I^2C protocol is also mounted to provide for the Serial Presence Detects (SPD). Decoupling capacitors of 0.1µF are mounted for the SDRAMs and the EEPROM. Damping resistors are added to the data lines.

The module has gold edge connections and is intended for mounting into 144-pin SO-DIMM edge connector sockets keyed for 3.3V.

See *Ordering Information* for PC100 performance options.

PIN CONFIGURATION

Pin Symbols

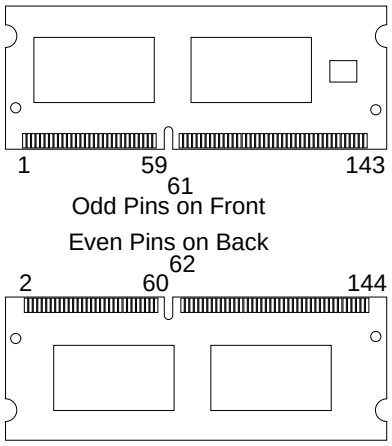
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	V_{SS}	21	V_{SS}	41	DQ_{10}	61	CLK_0	81	V_{DD}	101	V_{DD}	121	DQ_{24}	141	SDA
2	V_{SS}	22	V_{SS}	42	DQ_{42}	62	CKE_0	82	V_{DD}	102	V_{DD}	122	DQ_{56}	142	SCL
3	DQ_0	23	$DQMB_0$	43	DQ_{11}	63	V_{DD}	83	DQ_{16}	103	A_6	123	DQ_{25}	143	V_{DD}
4	DQ_{32}	24	$DQMB_4$	44	DQ_{43}	64	V_{DD}	84	DQ_{48}	104	A_7	124	DQ_{57}	144	V_{DD}
5	DQ_1	25	$DQMB_1$	45	V_{DD}	65	$\overline{RAS}$	85	DQ_{17}	105	A_8	125	DQ_{26}		
6	DQ_{33}	26	$DQMB_5$	46	V_{DD}	66	$\overline{CAS}$	86	DQ_{49}	106	BA_0	126	DQ_{58}		
7	DQ_2	27	V_{DD}	47	DQ_{12}	67	$\overline{WE}$	87	DQ_{18}	107	V_{SS}	127	DQ_{27}		
8	DQ_{34}	28	V_{DD}	48	DQ_{44}	68	CKE_1*	88	DQ_{50}	108	V_{SS}	128	DQ_{59}		
9	DQ_3	29	A_0	49	DQ_{13}	69	$\overline{S}_0$	89	DQ_{19}	109	A_9	129	V_{DD}		
10	DQ_{35}	30	A_3	50	DQ_{45}	70	A_{12}*	90	DQ_{51}	110	BA_1	130	V_{DD}		
11	V_{DD}	31	A_1	51	DQ_{14}	71	$\overline{S}_1$*	91	V_{SS}	111	A_{10}/AP	131	DQ_{28}		
12	V_{DD}	32	A_4	52	DQ_{46}	72	A_{13}*	92	V_{SS}	112	A_{11}	132	DQ_{60}		
13	DQ_4	33	A_2	53	DQ_{15}	73	NC	93	DQ_{20}	113	V_{DD}	133	DQ_{29}		
14	DQ_{36}	34	A_5	54	DQ_{47}	74	CLK_1	94	DQ_{52}	114	V_{DD}	134	DQ_{61}		
15	DQ_5	35	V_{SS}	55	V_{SS}	75	V_{SS}	95	DQ_{21}	115	$DQMB_2$	135	DQ_{30}		
16	DQ_{37}	36	V_{SS}	56	V_{SS}	76	V_{SS}	96	DQ_{53}	116	$DQMB_6$	136	DQ_{62}		
17	DQ_6	37	DQ_8	57	NC	77	NC	97	DQ_{22}	117	$DQMB_3$	137	DQ_{31}		
18	DQ_{38}	38	DQ_{40}	58	NC	78	NC	98	DQ_{54}	118	$DQMB_7$	138	DQ_{63}		
19	DQ_7	39	DQ_9	59	NC	79	NC	99	DQ_{23}	119	V_{SS}	139	V_{SS}		
20	DQ_{39}	40	DQ_{41}	60	NC	80	NC	100	DQ_{55}	120	V_{SS}	140	V_{SS}		

* Not used

(continued on the next page)

PIN CONFIGURATION *(continued)*

Pin Arrangement



Pin Functions

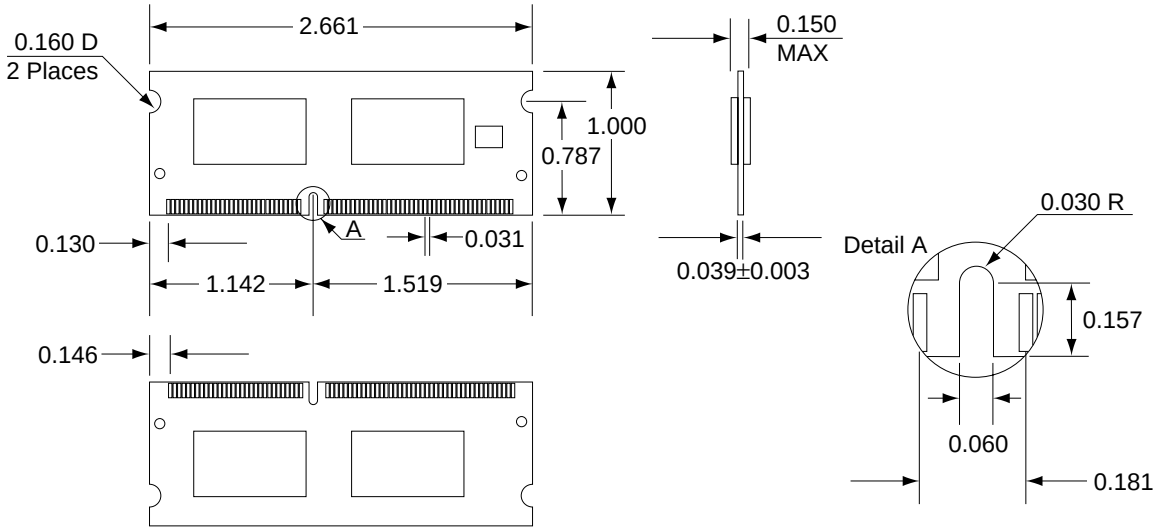
Pin Name	Pin Function
A_0-A_{10}/AP, A_{11}	Address Inputs (multiplexed)
BA_0, BA_1	Select Bank
DQ_0-DQ_{63}	Data In/Out
$\overline{WE}$	Read/Write Enable
CLK_0, CLK_1	Clock Input
CKE_0	Clock Enable Input
$\overline{RAS}$	Row Adress Strobe
$\overline{CAS}$	Column Address Strobe
$DQMB_0$-$DQMB_7$	Data Input/Output Mask
$\overline{S}_0$	Chip Select Input
SDA	Serial Data I/O
SCL	Serial Clock
V_{DD}	Power (+3.3V)
V_{SS}	Ground
NC	No Connection

ORDERING INFORMATION

Part Number	PC100 100MHz Parameters					
	CL	t_{RCD}	t_{RP}	t_{RC}	Units	Comment
SL64G6E8M4G-A10AV	3	3	3	8	clks	slowest supported (option “A”)
SL64G6E8M4G-A10BV	3	2	3	8	clks	2nd choice (option “B”)
SL64G6E8M4G-A10CV	3	2	2	7	clks	target (option “C”)
SL64G6E8M4G-A10DV	2	2	2	7	clks	goal (option “D”)

PACKAGE DIMENSIONS

Units: Inches



749-1

TOLERANCES: ±0.005 UNLESS OTHERWISE SPECIFIED

SERIAL PRESENCE DETECT INFORMATION

Serial PD Interface Protocol: I^2C; Current sink capability of SDA driver ≤ 3mA; Maximum clock frequency: 100 KHz

Byte #	Function Described	Function Supported				Hex Value			
		A	B	C	D	A	B	C	D
0	# of bytes written into serial memory at module manufacturer	128 bytes				80h			
1	Total # of bytes of SPD memory device	256Bytes (2K-bit)				08h			
2	Fundamental memory type	SDRAM				04h			
3	# of row addresses on this assembly	12				0Ch			
4	# of column addresses on this assembly	9				09h			
5	# of module banks on this assembly	1 bank				01h			
6	Data width of this assembly	64 bits				40h			
7	…Data width of this assembly (continued)	—				00h			
8	Voltage interface standard of this assembly	LVTTL				01h			
9	SDRAM cycle time at CL=3 (t_{CYC})	10ns	—	10ns	10ns	A0h	—	A0h	A0h
10	SDRAM access time from clock at CL=3 (t_{AC})	6ns	—	6ns	6ns	60h	—	60h	60h
11	DIMM configuration type	None				00h			
12	Refresh rate/type	15.625µs, Self-refresh				80h			
13	SDRAM width	16 bits				10h			
14	Error Checking DRAM data width	0 bits				00h			
15	Min. CLK delay for back-to-back rand. col. addr.	t_{CCD}=1 CLK				01h			
16	SDRAM device attributes: burst lengths supported	1,2,4,8, and full page				8Fh			
17	SDRAM device attributes: # of banks on SDRAM device	4 banks				04h			
18	SDRAM device attributes: CAS latency	CAS latency = 2,3				06h			
19	SDRAM device attributes: CS latency	CS latency = 0				01h			
20	SDRAM device attributes: Write latency	Write Latency = 0				01h			
21	SDRAM module attributes	non-buff., non-reg.				00h			
22	SDRAM device attributes: general	V_{CC}10%, B/R, S/W, P/A, A/P				0Eh			
23	Minimum clock cycle time at CL=2 (t_{CYC})	12ns	—	12ns	10ns	C0h	—	C0h	A0h
24	Max. data access time form clock at CL=2 (t_{AC})	8ns	—	8ns	6ns	80h	—	80h	60h
25	Minimum clock cycle time at CL=1 (t_{CYC})	—	—	—	—	00h	—	00h	00h
26	Max. data access time from clock at CL=1 (t_{AC})	—	—	—	—	00h	—	00h	00h
27	Minimum row precharge time (t_{RP})	30ns	—	20ns	20ns	1Eh	—	14h	14h
28	Minimum row active to row active delay (t_{RRD})	20ns	—	20ns	20ns	14h	—	14h	14h
29	Minumum RAS to CAS (t_{RCD})	30ns	—	20ns	20ns	1Eh	—	14h	14h
30	Minumum RAS pulse width (t_{RAS})	50ns	—	50ns	50ns	32h	—	32h	32h
31	Module bank density	64MB				10h			
32	Min. command and address signal setup time (t_{AS})	2ns				20h			
33	Min. command and address signal hold time (t_{AH})	1ns				10h			
34	Min. data signal input setup time (t_{DS})	2ns				20h			

continued on the next page

Byte #	Function Described	Function Supported				Hex Value			
		A	B	C	D	A	B	C	D
35	Min. data signal input hold time (t_{DH})	1ns				10h			
36-61	Superset information (may be used in future)	—				00h			
62	SPD revision	1.2	—	1.2	1.2	12h	—	12h	12h
63	Checksum for bytes 0-62	JEDEC calculation				xxh			
64	Manufacturer's JEDEC ID code per JEP-106E	Continuation code				7Fh			
65	Man. JEDEC ID code (continued)	SiliconTech's ID				A8h			
66-71						FFh			
72	Manufacturing location	SiliconTech USA				01h			
73-90	Manufacturer's part number					xxh			
91	Revision code of PCB	Eng(00),RevA(01),RevB(02)				01h			
92						FFh			
93	Manufacturing date	Year (BCD)				yy			
94		Calender Week (BCD)				ww			
95	Assembly serial number	Tester number				ss			
96		Serial number (bits 7-0)				ss			
97		Serial number (bits 15-8)				ss			
98		Serial number (bits 23-16)				ss			
99	Manufacture's specific data	S				53h			
100		i				69h			
101		l				6Ch			
102		i				69h			
103		c				63h			
104		o				6Fh			
105		n				6Eh			
106		T				54h			
107		e				65h			
108		c				63h			
109		h				68h			
110						FFh			
111						FFh			
112						FFh			
113						FFh			
114						FFh			
115						FFh			
115-125						FFh			
126	Intel specification frequency	100MHz				64h			
127	Intel specification details	Detailed 100MHz Info				8Fh	—	8Fh	8Fh

FUNCTIONAL BLOCK DIAGRAM