

## ADJUSTABLE LCD BOOST CONVERTER

### FEATURES

- Input Voltage Range . . . 1.8 V to 6.0 V
- Up to 85% Efficiency
- Digitally Adjustable Output Voltage Control
- Disconnects Output From Input During Shutdown
- Switching Frequency . . . Up to 1 MHz
- No Load Quiescent Current . . . 40  $\mu$ A Typ
- Thermal Shutdown Mode
- Shutdown Current . . . 0.1  $\mu$ A Typ
- Available in Small 3mm  $\times$  3mm QFN package

### DESCRIPTION

The TPS61045 is a high frequency boost converter with digitally programmable output voltage and true shutdown. During shutdown the output is disconnected from the input by opening the internal input switch. This allows a controlled power up/down sequencing of the display. The output voltage can be increased or decreased in digital steps by applying a low pulse to the CTRL pin. The output voltage range, as well as the output voltage step size, can be programmed with the feedback divider network. With a high switching frequency of up to 1 MHz the TPS61045 allows the use of small external components and together, with the small 8-pin QFN package, a minimum system solution size is achieved.

### APPLICATIONS

- LCD Bias Supply For Small to Medium LCD Displays
- OLED Display Power Supply
  - PDA, Pocket PC, Smart Phones
  - Handheld Devices
  - Cellular Phones

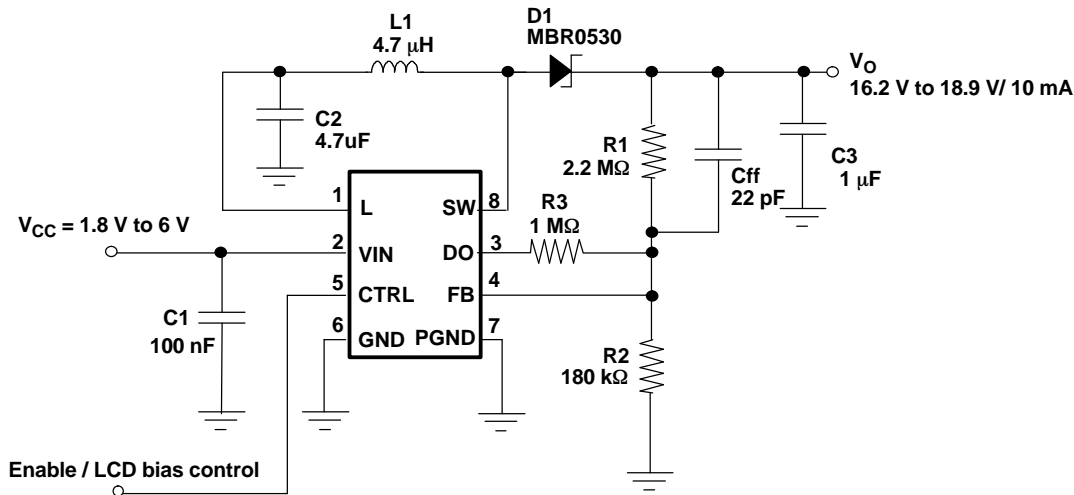


Figure 1. Typical Application



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

# TPS61045

SLVS440 — JANUARY 2003



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## ORDERING INFORMATION (1)

TA	8 Pin QFN Package (DRB)	Package Marking
-40°C to 85°C	TPS61045DRB	BHT

- (1) The DRB package is available taped and reeled. Add R suffix (TPS61045DRBR) to order quantities of 3000 units per reel. Add T suffix (TPS61045DBRT) to order quantities of 250 units per reel.

## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)

	TPS61045
Supply Voltage, $V_{(VIN)}$ (2)	-0.3 V to 7 V
Voltages, $V_{(CTRL)}$ , $V_{(FB)}$ , $V_{(L)}$ , $V_{(DO)}$ (2)	-0.3 V to $V_I + 0.3$ V
Voltage, $V_{(SW)}$ (2)	30 V
Continuous power dissipation	See Dissipation Rating Table
Operating junction temperature range	-40°C to 150°C
Storage temperature range, $T_{STG}$	-65°C to 150°C
Lead temperature (soldering, 10 sec)	260°C

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to network ground terminal.

## DISSIPATION RATING

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 85^\circ\text{C}$ POWER RATING
8 pin QFN (DRB) (1)	370 mW	3.7 mW/°C	204 mW	148 mW

- (1) The thermal resistance junction to ambient of the 8 pin QFN package is 270°C/W. Standard 2 layer PCB without vias for the thermal pad. See the application section on how to improve the thermal resistance  $R_{\theta JA}$ .

## RECOMMENDED OPERATING CONDITIONS

	MIN	TYP	MAX	UNIT
$V_I$ Input voltage range	1.8		6.0	V
$V_S$ Switch voltage			30	V
L Inductor (1)		4.7		μH
f Switching frequency (1)			1	MHz
$C_{I(C2)}$ Input capacitor (C2) (1)		4.7		μF
$C_{O(C3)}$ Output capacitor (C3) (1)		1		μF
$T_A$ Operating ambient temperature	-40		85	°C
$T_J$ Operating junction temperature	-40		125	°C

- (1) See application section for further information.

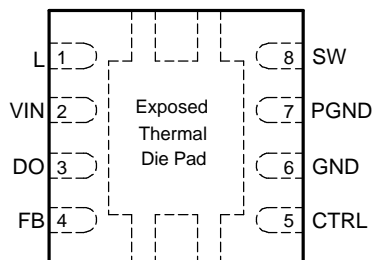
**ELECTRICAL CHARACTERISTICS**
 $V_I = 2.4\text{ V}$ ,  $CTRL = V_I$ ,  $V_O = 18.0\text{ V}$ ,  $I_O = 10\text{ mA}$ ,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$ , typical values are at  $T_A = 25^\circ\text{C}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>Supply current</b>						
$V_I$	Input voltage range		1.8		6.0	V
$I_Q$	Operating quiescent current	$I_O = 0\text{ mA}$ , not switching		40	65	$\mu\text{A}$
$I_{O(SD)}$	Shutdown current	$CTRL = GND$		0.1	1	$\mu\text{A}$
$V_{UVLO}$	Under-voltage lockout threshold	$V_I$ falling		1.5	1.7	V
<b>CTRL and DAC output</b>						
$V_{IH}$	CTRL high level input voltage		1.3			V
$V_{IL}$	CTRL low level input voltage				0.3	V
$I_{lkg}$	CTRL input leakage current	$CTRL = GND$ or $V_{IN}$			0.1	$\mu\text{A}$
$V_{O(DO)}$	DAC output voltage range		0		1.233	V
	DAC resolution	6 Bit		19.6		mV
$V_{O(DO)}$	DAC center output voltage	$CTRL = \text{high}$		607		mV
$I_{O(SINK)}$	Maximum DAC sink current				30	$\mu\text{A}$
$t_{(UP)}$	Increase output voltage one step	$CTRL = \text{high to low}$	1		60	$\mu\text{s}$
$t_{(DWN)}$	Decrease the output voltage one step	$CTRL = \text{high to low}$	140		240	$\mu\text{s}$
$t_{d1}$	Delay time between up/down steps	$CTRL = \text{low to high}$	1			$\mu\text{s}$
$t_{(OFF)}$	Shutdown	$CTRL = \text{high to low}$	560			$\mu\text{s}$
<b>Input switch (Q1), main switch (Q2) and current limit</b>						
$V_{SW(Q2)}$	Main switch maximum voltage (Q2)				30	V
$r_{ds(ON)}$	Main switch MOSFET on-resistance	$V_I = 2.4\text{ V}$ ; $I_S = 200\text{ mA}$		400	800	$\text{m}\Omega$
$I_{lkg(MAIN)}$	Main switch MOSFET leakage current	$V_S = 28\text{ V}$		0.1	10	$\mu\text{A}$
$I_{(LIM)}$	Main switch MOSFET current limit		350	375	450	mA
$r_{ds(ON)}$	Input switch MOSFET on-resistance	$V_I = 2.4\text{ V}$ ; $I_S = 200\text{ mA}$		1	2	$\Omega$
$I_{lkg(IN)}$	Input switch MOSFET leakage current	$V_L = \text{TBD}$		0.1	10	$\mu\text{A}$
<b>Output</b>						
$V_O$	Output voltage range		$V_{in}$		28	V
$V_{ref}$	Internal voltage reference			1.233		V
$I_{(FB)}$	Feedback input bias current	$V_{FB} = 1.3\text{ V}$		30	100	nA
$V_{(FB)}$	Feedback trip point voltage	$1.8\text{ V} \leq V_I \leq 6.0\text{ V}$ ; $V_O = 18\text{ V}$ , $I_{(LOAD)} = 10\text{ mA}$	1.208	1.233	1.258	V

# TPS61045

SLVS440 — JANUARY 2003

## DRB PACKAGE (TOP VIEW)

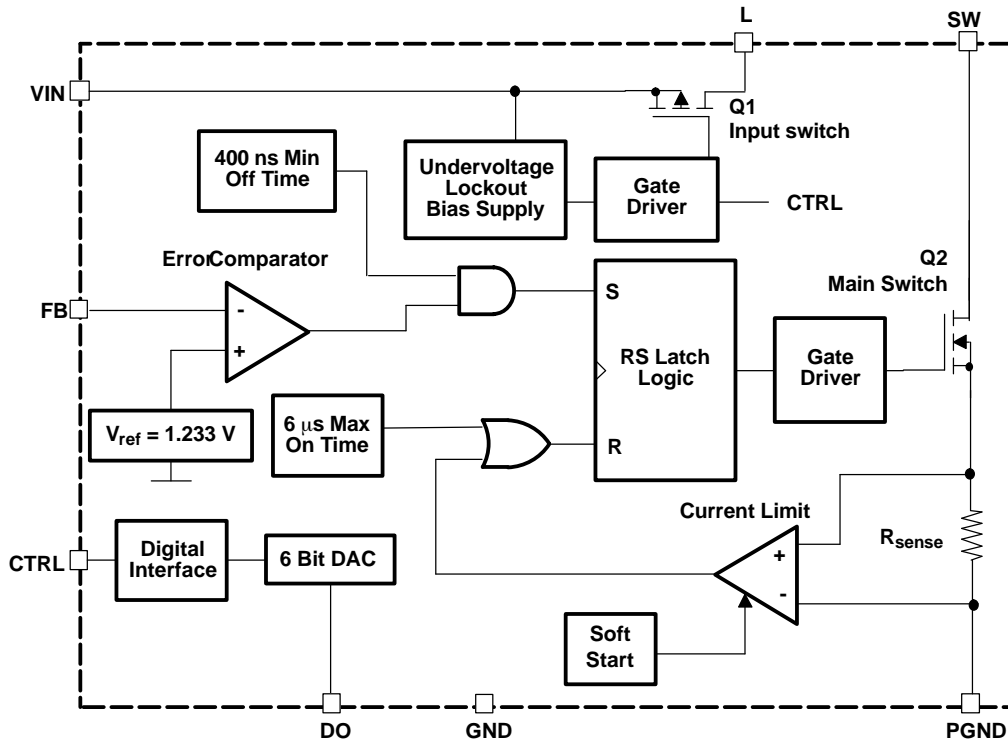


NOTES: The Exposed Thermal Die Pad is connected to PGND. Connect this pad directly with the GND pin.

## TERMINAL FUNCTIONS

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
CTRL	5	I	Combined enable and output voltage pin. Pulling CTRL constantly high enables the device. When CTRL is pulled to GND, the device is disabled and the input is disconnected from the output by opening the integrated switch Q1. Pulsing CTRL low increases or decreases the output voltage. Refer to the <i>application information</i> section for further information.
DO	3	O	Internal DAC output. DO programs the output voltage via the CTRL pin. Refer to the <i>application information</i> section for further information.
FB	4	I	Feedback. FB must be connected to the output voltage-feedback divider.
GND	7		Analog ground. GND must be directly connected to the PGND pin. Refer to the <i>application information</i> section for further information.
L	1	O	Drain of the internal switch (Q2). Connect L to the inductor.
PGND	6		Power ground.
SW	8	I	Drain of the integrated switch Q2. SW is connected to the inductor and anode of the Schottky rectifier diode.
VIN	2	I	Input supply pin

**FUNCTIONAL BLOCK DIAGRAM**



## TYPICAL CHARACTERISTICS TABLE OF GRAPHS

			FIGURE
$\eta$	Efficiency	vs Load current	Figure 2
		vs Input voltage	Figure 3
$I_{DD(Q)}$	Quiescent current	vs Input voltage	Figure 4
$V_{(FB)}$	Feedback voltage	vs Temperature	Figure 5
$I_{(FB)}$	Feedback current	vs Temperature	Figure 6
$r_{ds(on)}$	$r_{ds(on)}$ Main switch Q2	vs Temperature	Figure 7
		vs Input voltage	Figure 8
	$r_{ds(on)}$ Input switch Q1	vs Temperature	Figure 9
		vs Input voltage	Figure 10
$V_{(DO)}$	$V_{(DO)}$ Voltage	vs CTRL input step	Figure 11
	Line transient response		Figure 12
	Load transient response		Figure 13
	PFM operation		Figure 14
	Soft start		Figure 15

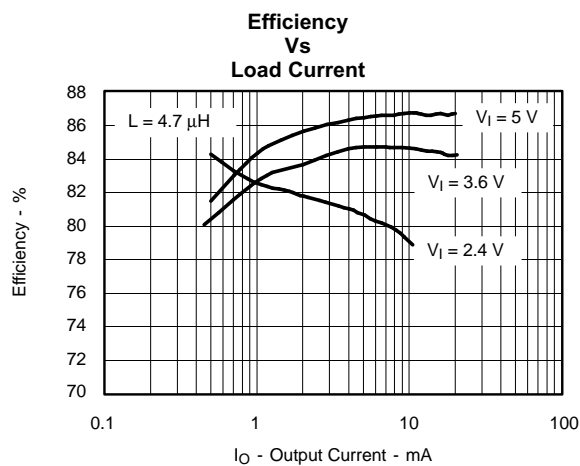


Figure 2

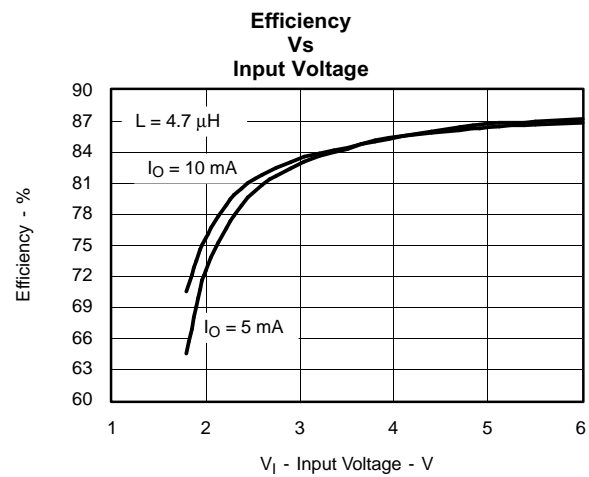


Figure 3

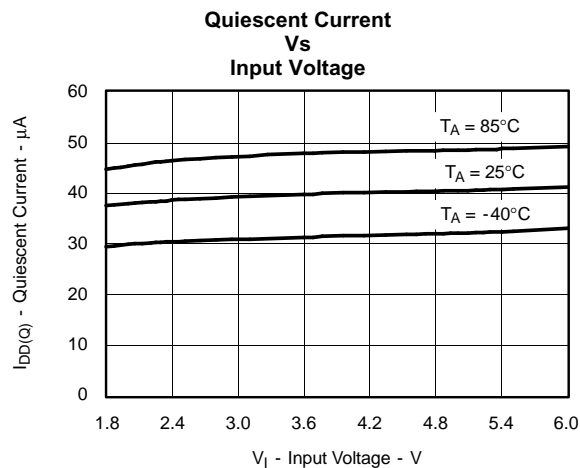


Figure 4

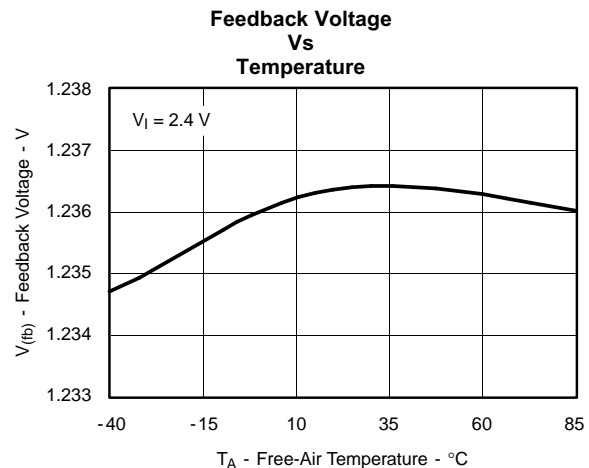
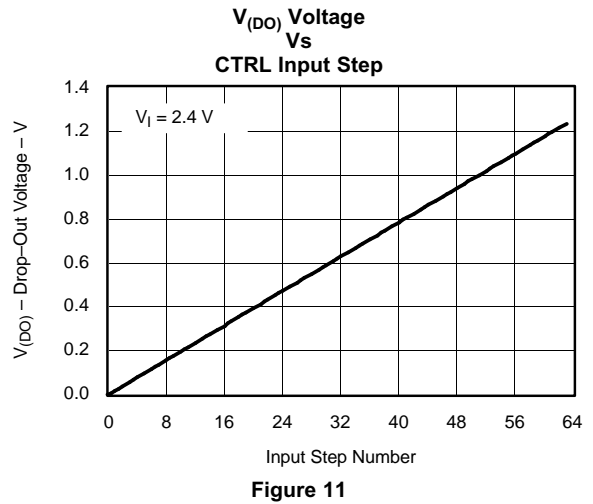
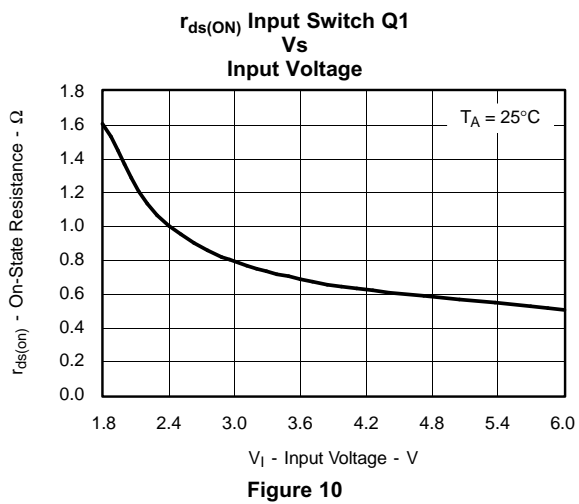
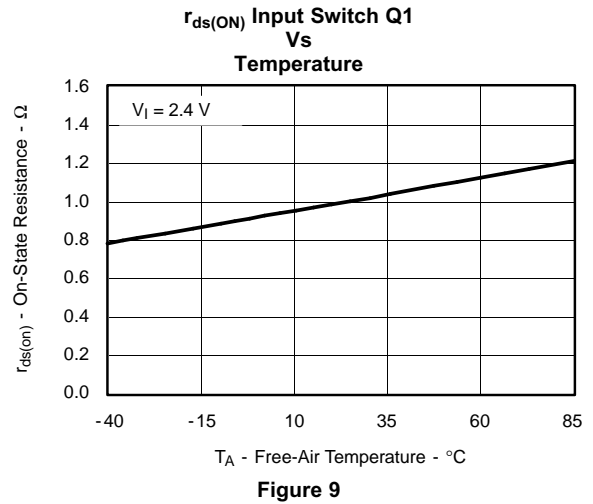
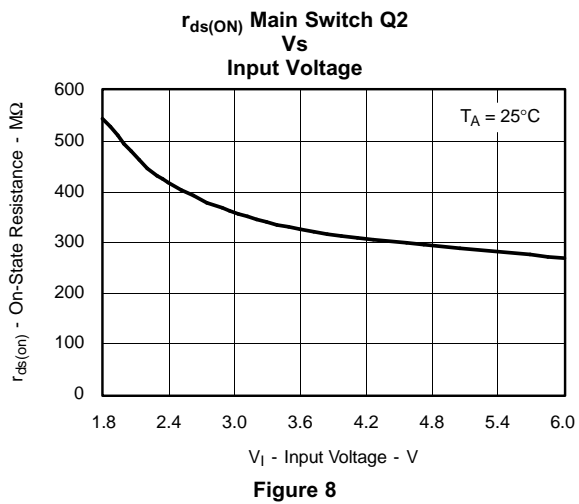
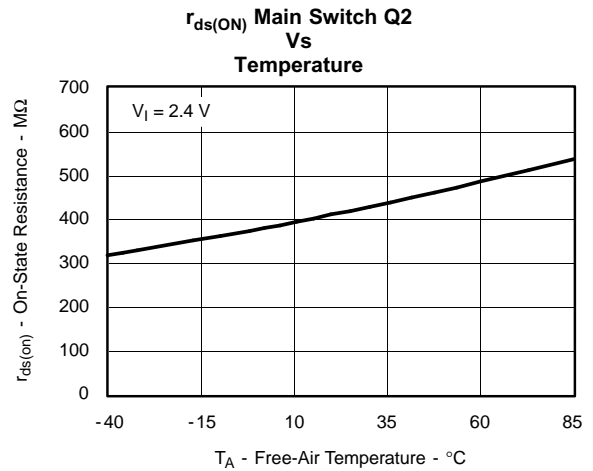
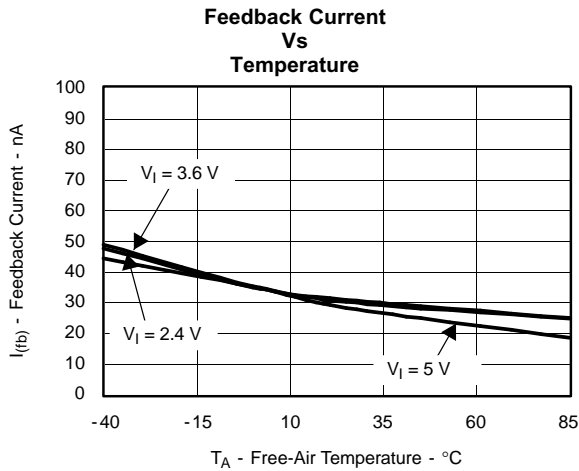


Figure 5



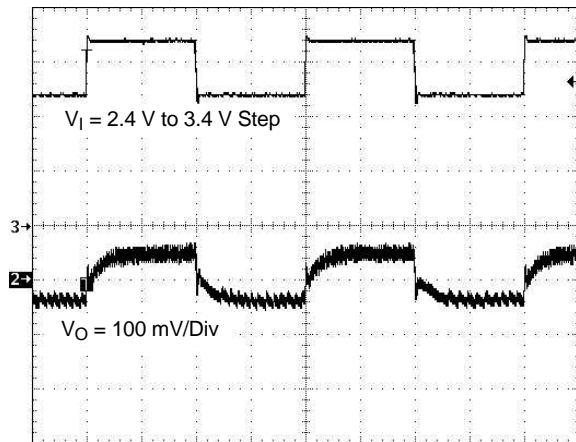


Figure 12 . Line Transient Response

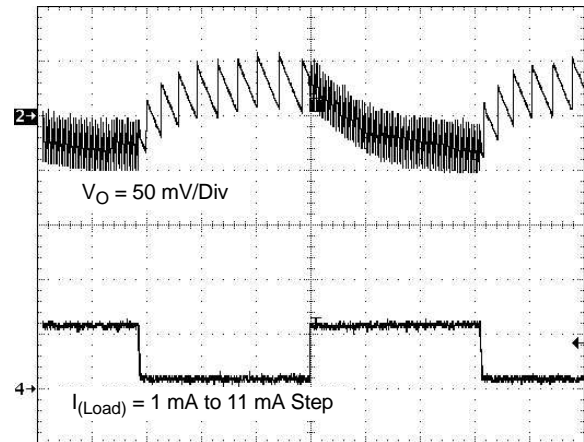


Figure 13 . Load Transient Response

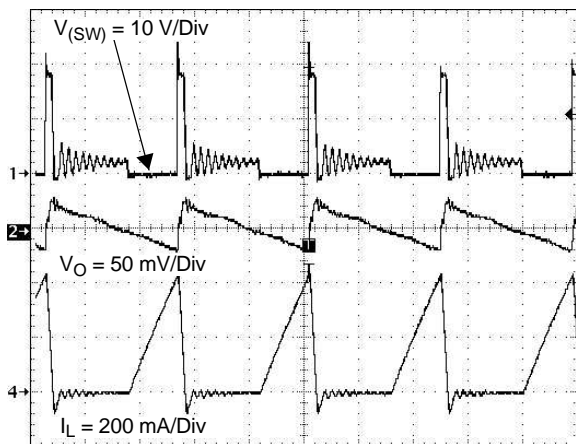


Figure 14 . PFM Operation

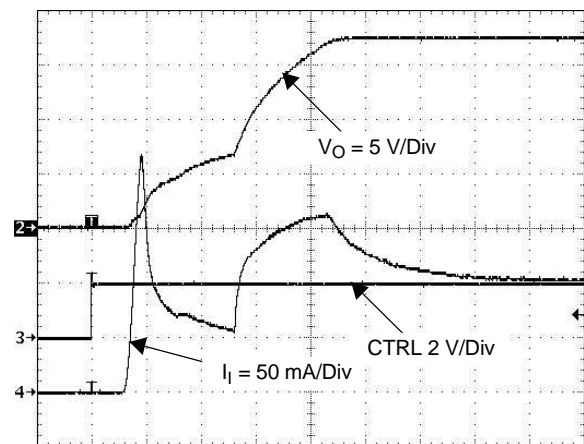


Figure 15 . Soft Start



## DETAILED DESCRIPTION

### OPERATION

The TPS61045 operates with an input voltage range of 1.8 V to 6.0 V and generates output voltages of up to 28 V. The device operates in a pulse frequency modulation (PFM) scheme with constant peak current control. This control scheme maintains high efficiency over the entire load current range and, with a switching frequency of up to 1 MHz, the device enables the use of small external components.

The converter monitors the output voltage and when the feedback voltage falls below the reference voltage of 1.233 V (typ) the main switch turns on and the current ramps up. The main switch turns off when the inductor current reaches the internally set peak current of 375 mA (typ). Refer to the *peak current control* section for more information. The second criteria that turns off the main switch is the maximum on-time of 6  $\mu$ s (typ). This limits the maximum on-time of the converter in extreme conditions. As the switch is turned off, the external Schottky diode is forward biased delivering the current to the output. The main switch remains off until the minimum off time of 400 ns (typ) has passed and the feedback voltage is below the reference voltage again. Using this PFM peak current control scheme, the converter operates in discontinuous conduction mode (DCM) where the switching frequency depends on the input voltage, output voltage and output current. This gives a high efficiency over the entire load current range. This regulation scheme is inherently stable which allows a wider range for the selection of the inductor and output capacitor.

### PEAK CURRENT CONTROL

The internal switch is turned on until the inductor current reaches the typical DC current limit ( $I_{LIM}$ ) of 375 mA. Due to the internal current limit delay of 100 ns (typ) the actual current exceeds the DC current limit threshold by a small amount. The typical peak current limit can be calculated:

$$I_{P(typ)} = I_{(LIM)} + \frac{V_L}{L} \times 100 \text{ ns}$$

$$I_{P(typ)} = 400 \text{ mA} + \frac{V_L}{L} \times 100 \text{ ns}$$

The higher the input voltage and the lower the inductor value, the greater the current limit overshoot.

### SOFTSTART

All inductive step-up converters exhibit high inrush current during start up if no special precaution are taken. This can cause voltage drops at the input rail during start-up, which may result in an unwanted or premature system shut down.

When the device is enabled, the internal input switch (Q1) is slowly turned on to reduce the in-rush current charging the capacitor (C2) connected to pin L. Furthermore, the TPS61045 limits this in-rush current during start-up by increasing the current limit in two steps starting from  $I_{LIM}/4$  for 256 switch cycles to  $I_{LIM}/2$  for the next 256 switch cycles.

### ENABLE (CTRL PIN)

The CTRL pin serves two functions. One is the enable and disable of the device. The other is the output voltage programming of the device. If the digital interface is not required, the CTRL pin is used as a standard enable pin for the device.

Pulling the CTRL pin high enables the device beginning with the softstart cycle.

Pulling the CTRL pin to ground for a period of  $\geq 560 \mu$ s shuts down the device, reducing the shutdown current to 0.1  $\mu$ A (typ). During shutdown the internal input switch (Q1) remains open and disconnects the load from the input supply of the device.

This pin must be terminated.

## TPS61045

SLVS440 — JANUARY 2003

### DAC OUTPUT (DO)

The TPS61045 allows digital adjustment of the output voltage using the digital CTRL interface as described in the next section. The DAC output pin (DO) drives an external resistor (R3) connected to the external feedback divider. The DO output has a typical output voltage range from 0 V to  $V_{ref}$  (1.233V). If the DO output voltage is set to 0 V, the external resistor (R3) is more or less in parallel to the lower feedback resistor (R2) giving the highest output voltage. Programming the DO output to  $V_{ref}$  gives the lowest output voltage. Internally, a 6-bit DAC is used with 64-steps and 0 as the first step. This gives a typical voltage step of 19.6 mV which is calculated as:

$$\left( V_{O(DO)} = \frac{V_{ref}}{2^{6-1}} \right)$$

See the section *setting the output voltage* for further information.

After start-up, when the CTRL pin is pulled high, the DO output voltage is set to its center voltage which is the 32nd step of typically  $V_{(DO)} = 607\text{mV}$ .

### DIGITAL INTERFACE (CTRL)

When the CTRL pin is pulled high the device starts up with softstart and the DAC output voltage (DO) sets to its center voltage with a typical output voltage of 607 mV.

The output voltage can be programmed by pulling the CTRL pin low for a certain period of time. Depending on this time period the internal DAC increases or decreases the output voltage  $V_{(DO)}$  one digital step, as outlined in the timing table and timing diagram below. Programming the DAC output  $V_{(DO)}$  to 0 V places R3 in parallel to R2, which gives the maximum output voltage. If the DAC is programmed to its maximum output voltage equal to the internal reference voltage, typically  $V_{(DO)}=1.233\text{ V}$ , then the output has its minimum output voltage.

DAC output DO	Time	Logic Level
Increase one step	$t_{(UP)} = 1\ \mu\text{s}$ to $60\ \mu\text{s}$	Low
Decrease one step	$t_{(DWN)} = 140\ \mu\text{s}$ to $240\ \mu\text{s}$	Low
Shutdown	$t_{(OFF)} \geq 560\ \mu\text{s}$	Low
Delay between steps	$t_{d1} = 1\ \mu\text{s}$	High

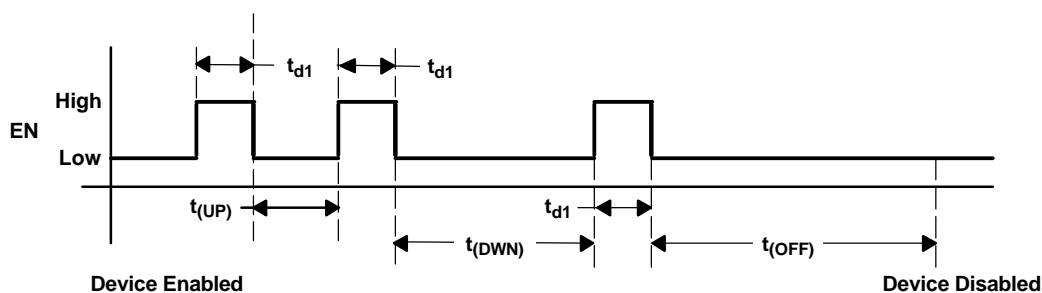


Figure 16. CTRL Timing Diagram

### UNDERVOLTAGE LOCKOUT

An undervoltage lockout feature prevents misoperation of the device at input voltages below 1.5 V (typ). As long as the input voltage is below the undervoltage threshold the device remains off, with the input switch (Q1) and the main switch (Q2) open.

### THERMAL SHUTDOWN

An internal thermal shutdown is implemented in the TPS61045 that shuts down the device if the typical junction temperature of 160°C is exceeded. If the device is in thermal shutdown mode, the input switch (Q1) and the main switch (Q2) are open.

## APPLICATION INFORMATION

### INDUCTOR SELECTION, MAXIMUM LOAD CURRENT

Since the PFM peak current control scheme is inherently stable the inductor and capacitor value does not affect the stability of the regulator. The selection of the inductor together with the nominal load current, input, and output voltage of the application determines the switching frequency of the converter. Depending on the application, inductor values between 2.2  $\mu\text{H}$  up to 47  $\mu\text{H}$  are recommended. The maximum inductor value is determined by the maximum switch on-time of 6  $\mu\text{s}$  (typ). The peak current limit of 375 mA (typ) must be reached within this 6  $\mu\text{s}$  for proper operation.

The inductor value determines the maximum switching frequency of the converter. Therefore, the inductor value must be selected that the maximum switching frequency, at maximum load current of the converter, is not exceeded. A good inductor value to start with is 4.7  $\mu\text{H}$ . The maximum switching frequency is calculated as:

$$f_{s(\text{max})} = \frac{V_I \times (V_O - V_I)}{I_P \times L \times V_O}$$

with:

$I_P$  = peak current as described in the previous *peak current control* section.

$$I_{P(\text{typ})} = 375 \text{ mA} + \frac{V_I}{L} \times 100 \text{ ns}$$

$L$  = selected inductor value

If the selected inductor does not exceed the maximum switching frequency of the converter, as a next step, the switching frequency at the nominal load current is estimated as follows:

$$f_{s(I\text{LOAD})} = \frac{2 \times I_{\text{LOAD}} \times (V_O - V_I + V_F)}{I_P^2 \times L}$$

with:

$I_P$  = peak current as described in the previous *chapter peak current control* section

$$I_{P(\text{typ})} = 375 \text{ mA} + \frac{V_I}{L} \times 100 \text{ ns}$$

$L$  = selected inductor value

$I_{(\text{LOAD})}$  = nominal load current

$V_F$  = rectifier diode forward voltage (typically 0.3 V)

The smaller the inductor value, the higher the switching frequency of the converter but the lower the efficiency.

The maximum load current of the converter is determined at the operation point where the converter starts to enter continuous conduction mode. Usually, the converter must always operate in discontinuous conduction mode to maintain regulation.

Two conditions exist for determining the maximum output current of the converter. One is when the inductor current fall time is <400 ns, and the other is when the inductor current fall time is >400 ns.

One way to calculate the maximum available load current under certain operation conditions is to estimate the expected converter efficiency at the maximum load current. This number can be taken out of the efficiency graphs shown in Figure 2 and Figure 3. Then the maximum load current can be estimated:

Inductor fall time:

$$t_{\text{fall}} = \frac{I_P \times L}{V_O - V_I}$$

## TPS61045

SLVS440 — JANUARY 2003

 For  $t_f \geq 400$  ns

$$I_{\text{load max}} = \eta \frac{I_P \times V_I}{2 \times V_O}$$

 $t_f \leq 400$  ns

$$I_{\text{load max}} = \eta \times \frac{I_P^2 \times L \times V_I}{(V_O - V_I) \times (2 \times I_P \times L + 2 \times 400 \text{ ns} \times V_I)}$$

with:

L = selected inductor value

 $\eta$  = expected converter efficiency (typically between 70% to 85%)

 $I_P$  = peak current as described in the previous *peak current control* section.

$$I_P = 300 \text{ mA} + \frac{V_I}{2} \times 100 \text{ ns}$$

The above formula contains the expected converter efficiency that allows calculating the expected maximum load current the converter can support. The efficiency can be taken out of the efficiency graphs shown in Figures 2 and 3 or 80% can be used as a good estimation.

The selected inductor must have a saturation current which meets the maximum peak current of the converter as calculated in the *peak current control* section. Use the maximum value for  $I_{L\text{lim}}$  (450mA) for this calculation.

Another important inductor parameter is the DC resistance. The lower the DC resistance, the higher the efficiency of the converter. Refer to the Table 1 and the *inductor selection* section under *typical applications*.

**TABLE 1: POSSIBLE INDUCTOR SELECTION**

Inductor Value	Component Supplier	Comments
10 $\mu$ H	Sumida CR32-100	High efficiency
10 $\mu$ H	Sumida CDRH3D16-100	High efficiency
10 $\mu$ H	muRata LQH43CN100K01	
4.7 $\mu$ H	Sumida CDRH3D16-4R7	Small solution size
4.7 $\mu$ H	muRata LQH32CN4R7M51	Small solution size

### SETTING THE OUTPUT VOLTAGE

When the converter is programmed to the minimum output voltage, the DAC output (DO) equals the reference voltage of 1.233 V (typ). Therefore, only the feedback resistor network (R1) and (R2) determines the output voltage under these conditions. This gives the minimum output voltage possible and can be calculated as:

$$V_{O(\text{min})} = V_{(\text{FB})} \times \left( \frac{R1}{R2} + 1 \right)$$

The maximum output voltage is determined as the DAC output (DO) is set to 0 V:

$$V_{O(\text{max})} = V_{(\text{FB})} \times \frac{R1}{R3} + V_{(\text{FB})} \times \left( \frac{R1}{R2} + 1 \right)$$

The output voltage can be digitally programmed by pulling the CTRL pin low for a certain period of time as described in the *Digital Interface* section. Pulling the signal applied to the CTRL pin low increases or decreases the DAC output DO (pin 3) one-step where one step is equal to typically 19.6 mV. A voltage step on DO of 19.6mV (typ) changes the output voltage by one step and is calculated as:

$$V_{O(\text{step})} = \frac{19.6 \text{ mV} \times R1}{R3}$$

The possible output voltage range is determined by selecting R1, R2 and R3. A possible larger output voltage range gives a larger output voltage step size. The smaller the possible output voltage range, the smaller the output voltage step size.

For battery powered applications a high impedance voltage divider must be used with a typical value for R2 of  $\leq 200 \text{ k}\Omega$  and a maximum value for R1 of  $2.2 \text{ M}\Omega$ .

Some applications may not need the digital interface to program the output voltage. In this case the output DO can be left open as shown in Figure 18 and the output voltage is calculated as for any standard boost converter:

$$V_O = 1.233 \text{ V} \times \left( 1 + \frac{R1}{R2} \right)$$

In such a configuration a high impedance voltage divider must also be used to minimize ground current and a typical value for R2 of  $\leq 200 \text{ k}\Omega$  and a maximum value for R1 of  $2.2 \text{ M}\Omega$  are recommended.

A feed-forward capacitor ( $C_{(FF)}$ ), across the upper feedback resistor (R1), is required to provide sufficient overdrive for the error comparator. Without a feed-forward capacitor or a too small feed-forward capacitor value, the device shows double pulses or a pulse burst instead of single pulses at the switch node (SW). This can cause higher output voltage ripple. If a higher output voltage ripple is acceptable, the feedforward capacitor can be left out too.

The lower the switching frequency of the converter, the larger the feed-forward capacitor value needs to be. A good starting point is the use of a  $10 \text{ pF}$  feed-forward capacitor. As a first estimation, the required value for the feed-forward capacitor can be calculated at the operation point:

$$C_{FF} \approx \frac{1}{2 \times \pi \times \frac{f_S}{20} \times R1}$$

with:

R1 = upper resistor of voltage divider

$f_S$  = switching frequency of the converter at the nominal load current. (For the calculation of the switching frequency see previous section)

For  $C_{(FF)}$  choose a value which comes closest to the calculation result.

The larger the feed-forward capacitor, the worse the line regulation of the device. Therefore, the feed-forward capacitor must be selected as small as possible if good line regulation is of concern.

## OUTPUT CAPACITOR SELECTION

For better output voltage filtering a low ESR output capacitor is recommended. Ceramic capacitors have low ESR values but depending on the application, tantalum capacitors can also be used. Refer to Table 2 and *typical applications* for the selection of the output capacitor.

Assuming the converter does not show double pulses or pulse bursts on the switch node (SW) the output voltage ripple is calculated as:

$$\Delta V_O = \frac{I_O}{C_O} \times \left( \frac{1}{f_{S(ILOAD)}} - \frac{I_P \times L}{V_O + V_F - V_I} \right) + I_P \times \text{ESR}$$

with:

$I_P$  = peak current as described in the previous section *peak current control*

$$I_P = 375 \text{ mA} + \frac{V_I}{2} \times 100 \text{ ns}$$

L = selected inductor value

$I_{O(LOAD)}$  = Nominal load current

$f_{S(Iload)}$  = switching frequency at the nominal load current as calculated previously.

## TPS61045

SLVS440 — JANUARY 2003

$V_F$  = rectifier diode forward voltage (typically 0.3 V)

$C_O$  = selected output capacitor

ESR = output capacitor ESR value

### INPUT CAPACITOR SELECTION

The input capacitor (C1) filters the high frequency noise and must be directly connected to the input pin (VIN) of the device. The capacitor (C2) connected to the L pin of the device is the main capacitor for input voltage filtering.

The main purpose of the capacitor (C2), that is connected directly to the L pin, is to smooth the inductor current. A larger capacitor reduces the inductor ripple current present at the L pin. The smaller the ripple current at the L pin, the higher the efficiency of the converter. If a sufficiently large capacitor is used, the input switch must carry only the DC current, filtered by the capacitor (C2), and not the high switching currents of the converter. A 4.7  $\mu$ F or 10- $\mu$ F ceramic capacitor (C2) is sufficient for most applications. For better filtering this value can be increased without limit. Refer to Table 2 and *typical applications* for input capacitor recommendations.

**TABLE 2: POSSIBLE INPUT AND OUTPUT CAPACITOR SELECTION**

Capacitor	Voltage Rating	Component Supplier	Comments
4.7 F/X5R/0805	6.3 V	Tayo Yuden JMK212BY475MG	$C_I/C_O$
10 $\mu$ F/X5R/0805	6.3 V	Tayo Yuden JMK212BJ106MG	$C_I/C_O$
1.0 $\mu$ F/X7R/1206	25 V	Tayo Yuden TMK316BJ105KL	$C_O$
1.0 $\mu$ F/X7R/1206	35 V	Tayo Yuden GMK316BJ105KL	$C_O$
4.7 $\mu$ F/X5R/1210	25 V	Tayo Yuden TMK325BJ475MG	$C_O$

### DIODE SELECTION

To achieve high efficiency a Schottky diode must be used. The current rating of the diode must meet the peak current rating of the converter as it is calculated in the *peak current control* section. Use the maximum value for  $I_{(LIM)}$  (450mA) for this calculation. Refer to Table 3 and the *typical applications* for the selection of the Schottky diode.

**TABLE 3: POSSIBLE SCHOTTKY DIODE SELECTION**

Component Supplier	Reverse voltage
ON Semiconductor MBR0530	30 V
ON Semiconductor MBR0520	20 V
ON Semiconductor MBRM120L	20 V
Toshiba CRS02	30 V
Zetex CHZS400	40 V

### LAYOUT CONSIDERATIONS

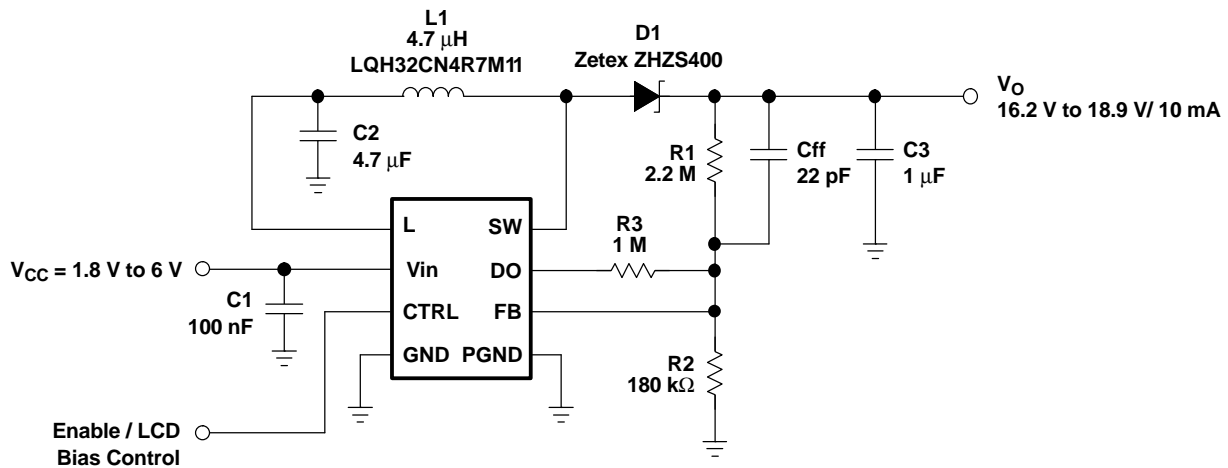
As for all switching power supplies the layout is an important step in the design, especially at high peak currents and switching frequencies. If the layout is not carefully implemented the regulator can show noise problems and duty cycle jitter.

The input capacitor must be placed as close as possible to the input pin for good input-voltage filtering. The inductor and diode must be placed as close as possible to the switch pin (SW) to minimize noise coupling into other circuits. Since the feedback pin and network is a high impedance circuit, the feedback network must be routed away from the inductor.

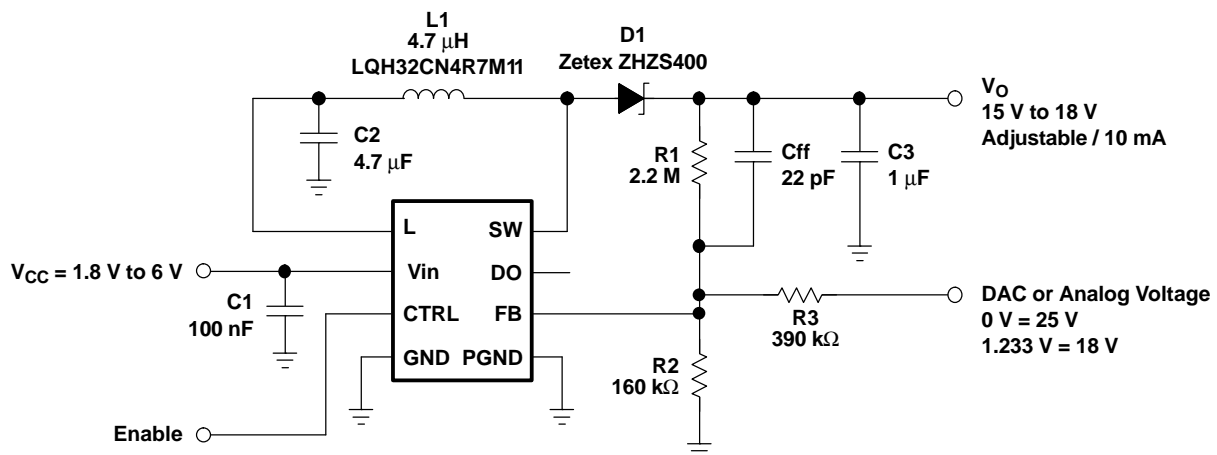
**thermal considerations**

The TPS61045 is available in a thermally enhanced QFN package. The package includes a thermal pad, improving the thermal capabilities of the package. See QFN/SON PCB Attachment Application Note (SLUA271).

The thermal resistance junction to ambient ( $R_{\theta JA}$ ) of the QFN package depends on the PCB layout. By using thermal vias and wide PCB traces improve thermal resistance ( $R_{\theta JA}$ ). Under normal operation conditions no PCB vias are required for the thermal pad. However, the thermal pad must be soldered to the PCB.



**Figure 17. Typical Application With Digital Adjusted Output Voltage**



**Figure 18. Typical Application With Analog Adjusted Output Voltage**

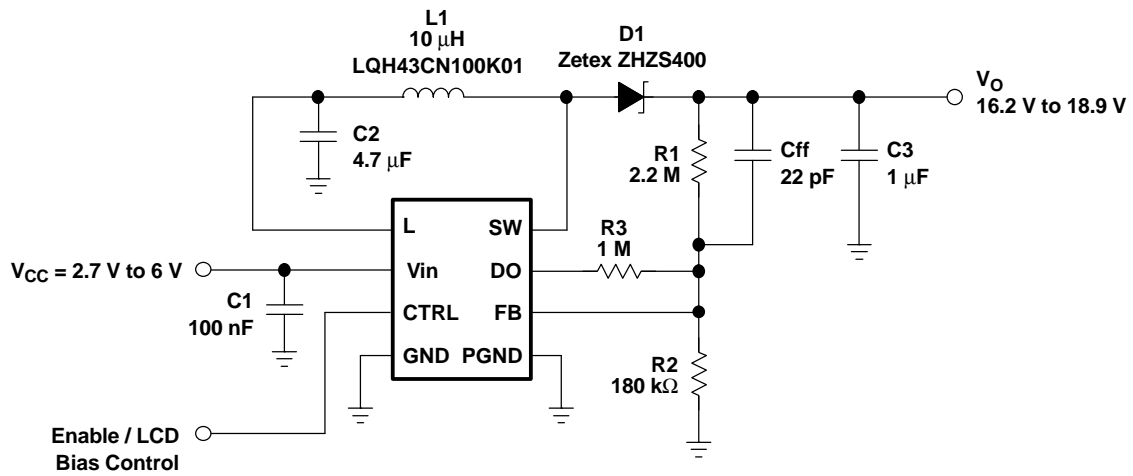
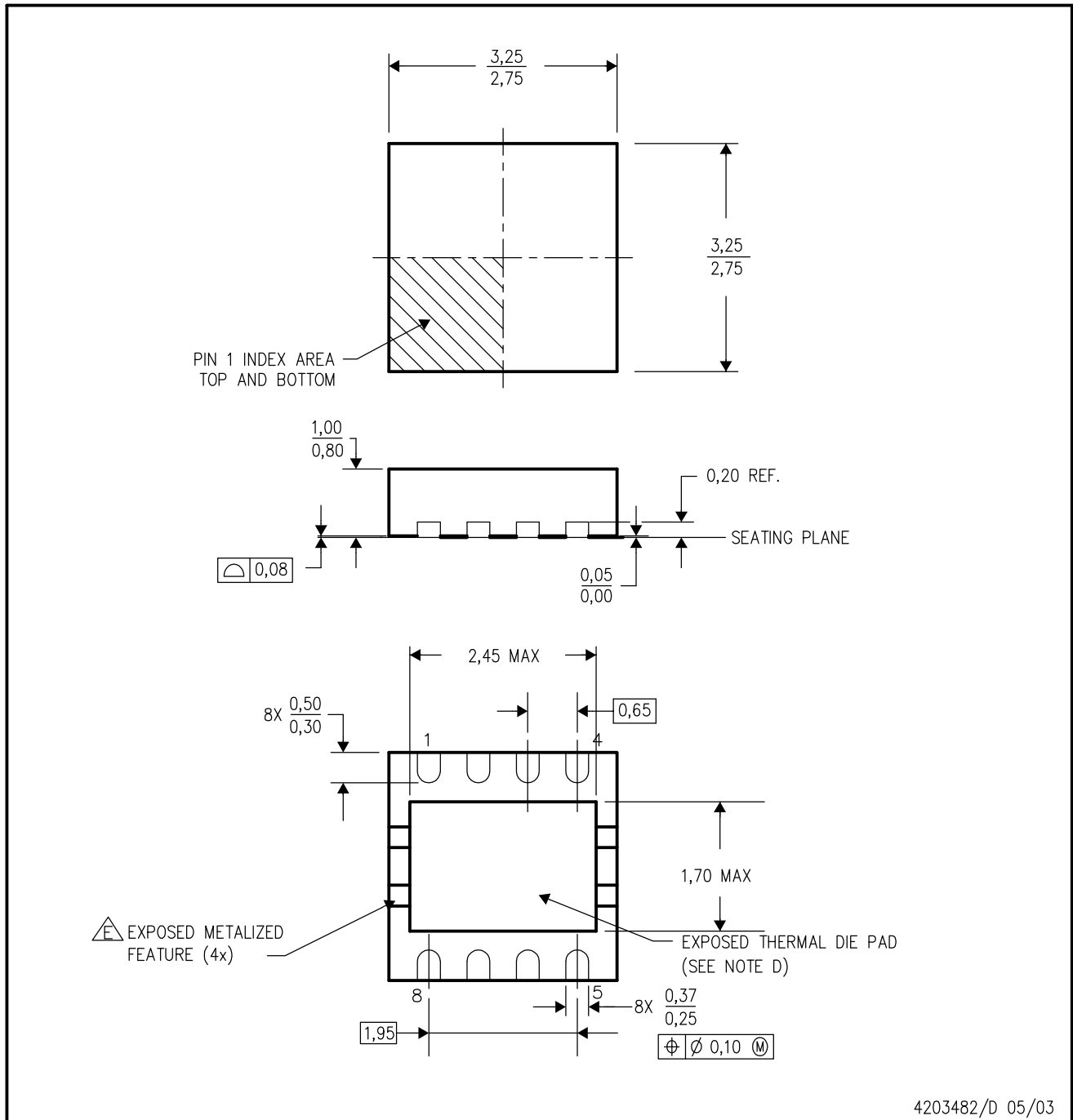


Figure 19. OLED Supply Providing Higher Output Current



DRB (S-PDSO-N8)

PLASTIC SMALL OUTLINE



4203482/D 05/03

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Small Outline No-Lead (SON) package configuration.
  - D. The package thermal performance may be enhanced by bonding the thermal die pad to an external thermal plane.
  - E. Metalized features are supplier options and may not be on the package.

## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

### Mailing Address:

Texas Instruments  
Post Office Box 655303  
Dallas, Texas 75265