

## 74ALVC162835

### Low Voltage 18-Bit Universal Bus Driver with 3.6V Tolerant Inputs/Outputs and 26Ω Series Resistors in Outputs

#### General Description

The ALVC162835 low voltage 18-bit universal bus driver combines D-type latches and D-type flip-flops to allow data flow in transparent, latched and clocked modes.

Data flow is controlled by output-enable ( $\overline{OE}$ ), latch-enable (LE), and clock (CLK) inputs. The device operates in Transparent Mode when LE is held HIGH. The device operates in clocked mode when LE is LOW and CLK is toggled. Data transfers from the Inputs ( $I_n$ ) to Outputs ( $O_n$ ) on a Positive Edge Transition of the Clock. When  $\overline{OE}$  is LOW, the output data is enabled. When  $\overline{OE}$  is HIGH the output port is in a high impedance state.

The ALVC162835 is designed with 26Ω series resistors in the outputs. This design reduces noise in applications such as memory address drivers, clock drivers, and bus transceivers/transmitters.

The 74ALVC162835 is designed for low voltage (1.65V to 3.6V)  $V_{CC}$  applications with I/O capability up to 3.6V.

The 74ALVC162835 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining low CMOS power dissipation.

#### Features

- Compatible with PC100 DIMM module specifications
- 1.65V–3.6V  $V_{CC}$  specifications provided
- 3.6V tolerant inputs and outputs
- 26Ω series resistors in outputs
- $t_{PD}$  (CLK to  $O_n$ )
  - 5.4 ns max for 3.0V to 3.6V  $V_{CC}$
  - 6.3 ns max for 2.3V to 2.7V  $V_{CC}$
  - 9.2 ns max for 1.65V to 1.95V  $V_{CC}$
- Power-down high impedance inputs and outputs
- Supports live insertion/withdrawal (Note 1)
- Latchup conforms to JEDEC JED78
- ESD performance:
  - Human body model > 2000V
  - Machine model >200V

**Note 1:** To ensure the high impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pulldown resistor; the minimum value of the resistor is determined by the current sourcing capability of the driver.

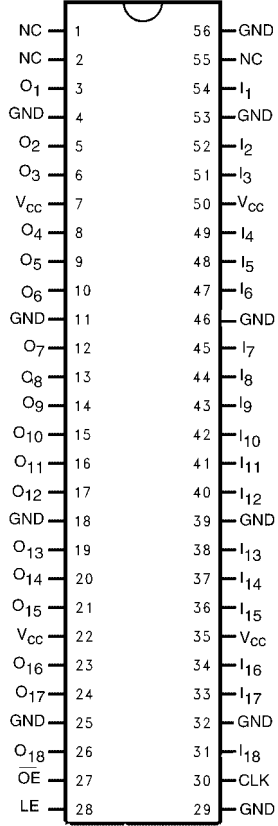
#### Ordering Code:

Order Number	Package Number	Package Description
74ALVC162835MTD	MTD56	56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

74ALVC162835 Low Voltage 18-Bit Universal Bus Driver with 3.6V Tolerant Inputs/Outputs and 26Ω Series Resistors in Outputs

### Connection Diagram



### Pin Descriptions

Pin Names	Description
$\overline{OE}$	Output Enable Input (Active LOW)
LE	Latch Enable Input
CLK	Clock Input
$I_1 - I_{18}$	Data Inputs
$O_1 - O_{18}$	3-STATE Outputs

### Truth Table

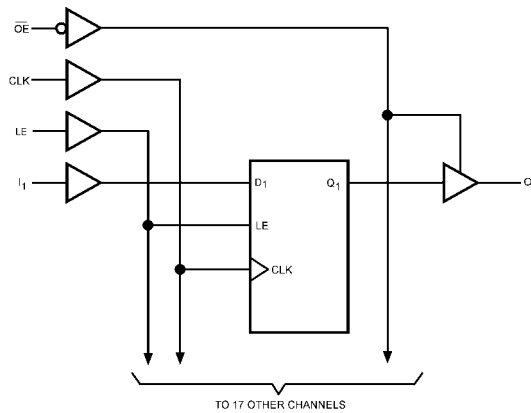
Inputs				Outputs
$\overline{OE}$	LE	CLK	$I_n$	$O_n$
H	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	↑	L	L
L	L	↑	H	H
L	L	H	X	$O_0$ (Note 2)
L	L	L	X	$O_0$ (Note 3)

H = Logic HIGH  
 L = Logic LOW  
 X = Don't Care, but not floating  
 Z = High Impedance  
 ↑ = LOW-to-HIGH Clock Transition

**Note 2:** Output level before the indicated steady-state input conditions were established provided that CLK was HIGH before LE went LOW.

**Note 3:** Output level before the indicated steady-state input conditions were established.

### Logic Diagram



**Absolute Maximum Ratings**(Note 4)

Supply Voltage ( $V_{CC}$ )	-0.5V to +4.6V
DC Input Voltage ( $V_I$ )	-0.5V to +4.6V
Output Voltage ( $V_O$ ) (Note 5)	-0.5V to $V_{CC} + 0.5V$
DC Input Diode Current ( $I_{IK}$ )	
$V_I < 0V$	-50 mA
DC Output Diode Current ( $I_{OK}$ )	
$V_O < 0V$	-50 mA
DC Output Source/Sink Current ( $I_{OH}/I_{OL}$ )	$\pm 50$ mA
DC $V_{CC}$ or Ground Current per Supply Pin ( $I_{CC}$ or Ground)	$\pm 100$ mA
Storage Temperature Range ( $T_{STG}$ )	-65°C to +150°C

**Recommended Operating Conditions** (Note 6)

Power Supply	
Operating	1.65V to 3.6V
Input Voltage	0V to $V_{CC}$
Output Voltage ( $V_O$ )	0V to $V_{CC}$
Free Air Operating Temperature ( $T_A$ )	-40°C to +85°C
Minimum Input Edge Rate ( $\Delta t/\Delta V$ )	
$V_{IN} = 0.8V$ to 2.0V, $V_{CC} = 3.0V$	10 ns/V

**Note 4:** The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The Recommended Operating Conditions tables will define the conditions for actual device operation.

**Note 5:**  $I_O$  Absolute Maximum Rating must be observed.

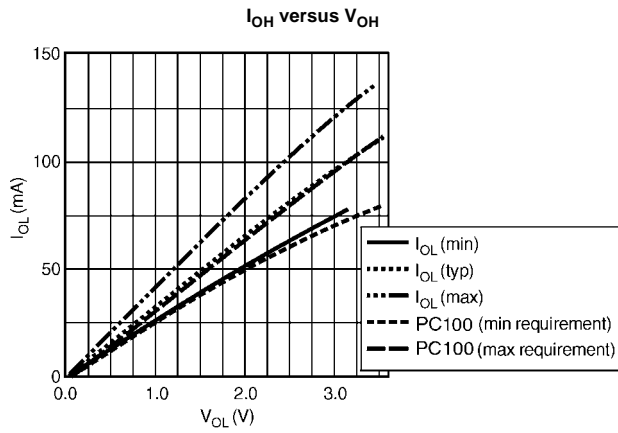
**Note 6:** Floating or unused pin (inputs or I/O's) must be held HIGH or LOW.

**DC Electrical Characteristics**

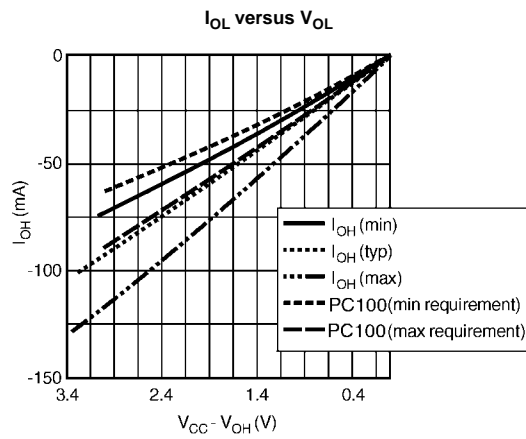
Symbol	Parameter	Conditions	$V_{CC}$ (V)	Min	Max	Units
$V_{IH}$	HIGH Level Input Voltage		1.65 - 1.95 2.3 - 2.7 2.7 - 3.6	$0.65 \times V_{CC}$ 1.7 2.0		V
$V_{IL}$	LOW Level Input Voltage		1.65 - 1.95 2.3 - 2.7 2.7 - 3.6		$0.35 \times V_{CC}$ 0.7 0.8	V
$V_{OH}$	HIGH Level Output Voltage	$I_{OH} = -100 \mu A$	1.65 - 3.6	$V_{CC} - 0.2$		V
		$I_{OH} = -2$ mA	1.65	1.2		
		$I_{OH} = -4$ mA	2.3	1.9		
		$I_{OH} = -6$ mA	2.3	1.7		
		$I_{OH} = -8$ mA	3.0	2.4		
		$I_{OH} = -12$ mA	2.7	2		
$V_{OL}$	LOW Level Output Voltage	$I_{OL} = 100 \mu A$	1.65 - 3.6		0.2	V
		$I_{OL} = 2$ mA	1.65		0.45	
		$I_{OL} = 4$ mA	2.3		0.4	
		$I_{OL} = 6$ mA	2.3		0.55	
		$I_{OL} = 8$ mA	3.0		0.55	
		$I_{OL} = 12$ mA	2.7		0.6	
$I_{OH}$	High Level Output Current		1.65		-2	mA
			2.3		-6	
			2.7		-8	
			3.0		-12	
$I_{OL}$	LOW Level Output Current		1.65		2	mA
			2.3		6	
			2.7		8	
			3		12	
$I_I$	Input Leakage Current	$0 \leq V_I \leq 3.6V$	3.6		$\pm 5.0$	$\mu A$
$I_{OZ}$	3-STATE Output Leakage	$0 \leq V_O \leq 3.6V$	3.6		$\pm 10$	$\mu A$
$I_{CC}$	Quiescent Supply Current	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6		40	$\mu A$
$\Delta I_{CC}$	Increase in $I_{CC}$ per Input	$V_{IH} = V_{CC} - 0.6V$	3 - 3.6		750	$\mu A$

AC Electrical Characteristics											
Symbol	Parameter		T <sub>A</sub> = -40°C to +85°C, R <sub>L</sub> = 500Ω								Units
			C <sub>L</sub> = 50 pF				C <sub>L</sub> = 30 pF				
			V <sub>CC</sub> = 3.3V ± 0.3V		V <sub>CC</sub> = 2.7V		V <sub>CC</sub> = 2.5V ± 0.2V		V <sub>CC</sub> = 1.8V ± 0.15V		
			Min	Max	Min	Max	Min	Max	Min	Max	
f <sub>CLOCK</sub>	Clock Frequency			150		150		150		100	MHz
t <sub>W</sub>	Pulse Width	LE High	3.3		3.3		3.3		4.0		ns
		CLK High or Low	3.3		3.3		3.3		4.0		
t <sub>S</sub>	Setup Time	Data Before CLK ↑	1.7		2.1		2.2		2.5		ns
		Data Before CLK ↓	CLK High	1.5		1.6		1.9			
			CLK Low	1.0		1.1		1.3			
t <sub>H</sub>	Hold Time	Data After CLK ↑	0.7		0.6		0.6		1.0		ns
		Data After LE ↓	1.4		1.7		1.4				
f <sub>MAX</sub>	Maximum Clock Frequency		150		150		150		100		MHz
t <sub>PHL</sub> , t <sub>PLH</sub>	Propagation Delay	I to O	1.0	4.2		5.0	1.0	5.0	1.5	9.8	ns
		LE to O	1.3	5.1		5.8	1.3	5.9	1.5	9.8	
		CLK to O	1.4	5.4		6.1	1.4	6.3	2.0	9.2	
t <sub>PZL</sub> , t <sub>PZH</sub>	Output Enable Time		1.1	5.5		6.5	1.4	6.3	1.5	9.8	ns
t <sub>PLZ</sub> , t <sub>PHZ</sub>	Output Disable Time		1.3	4.5		4.9	1.0	4.9	1.5	7.9	ns
AC Electrical Characteristics Over Load (Note 7)											
Symbol	Parameter		R <sub>L</sub> = 500Ω, V <sub>CC</sub> = 3.3V ± 0.15V						Units		
			T <sub>A</sub> = -0°C to +85°C			T <sub>A</sub> = -0°C to +65°C					
			C <sub>L</sub> = 0 pF								
			Min	Max	Min	Max					
t <sub>PHL</sub> , t <sub>PLH</sub>	Propagation Delay Bus to Bus		0.9	2.0	1.0	4.0		ns			
t <sub>PHL</sub> , t <sub>PLH</sub>	Propagation Delay Clock to Bus		1.4	2.9	1.9	5.0		ns			
<b>Note 7:</b> Characterized only.											
Capacitance											
Symbol	Parameter		Conditions	T <sub>A</sub> = +25°C		Units					
				V <sub>CC</sub>	Typical						
C <sub>IN</sub>	Input Capacitance	Control	V <sub>I</sub> = 0V or V <sub>CC</sub>	3.3	3.5	pF					
		Data	V <sub>I</sub> = 0V or V <sub>CC</sub>	3.3	5						
C <sub>OUT</sub>	Output Capacitance		V <sub>I</sub> = 0V, or V <sub>CC</sub>	3.3	7	pF					
C <sub>PD</sub>	Power Dissipation Capacitance	Outputs Enabled	f = 10 MHz, C <sub>L</sub> = 0 pF	3.3	40	pF					
				2.5	35						
		Outputs Disabled	f = 10 MHz, C <sub>L</sub> = 0 pF	3.3	14						
				2.5	125						

**I<sub>OUT</sub> - V<sub>OUT</sub> Characteristics**



**FIGURE 1. Characteristics for Output - Pull Up Drive**



**FIGURE 2. Characteristics for Output - Pull Down Driver**

AC Loading and Waveforms

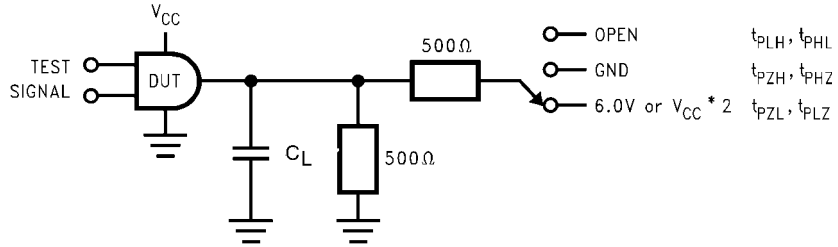


FIGURE 3. AC Test Circuit

TEST	SWITCH
$t_{PLH}, t_{PHL}$	Open
$t_{PZL}, t_{PLZ}$	6V at $V_{CC} = 3.3 \pm 0.3V$ ; $V_{CC} \times 2$ at $V_{CC} = 2.5 \pm 0.2V; 1.8V \text{ to } \pm 0.15V$
$t_{PZH}, t_{PHZ}$	GND

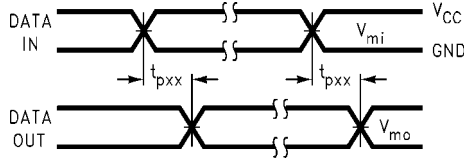


FIGURE 4. Waveform for Inverting and Non-inverting Functions  
 $t_r = t_f \leq 2.0ns, 10\% \text{ to } 90\%$

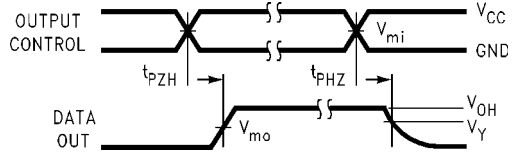


FIGURE 5. 3-STATE Output High Enable and Disable Times for Low Voltage Logic  
 $t_r = t_f \leq 2.0ns, 10\% \text{ to } 90\%$

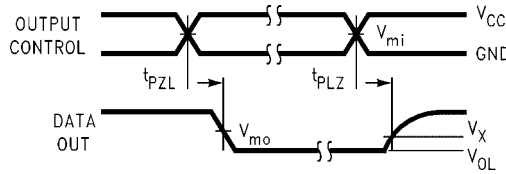
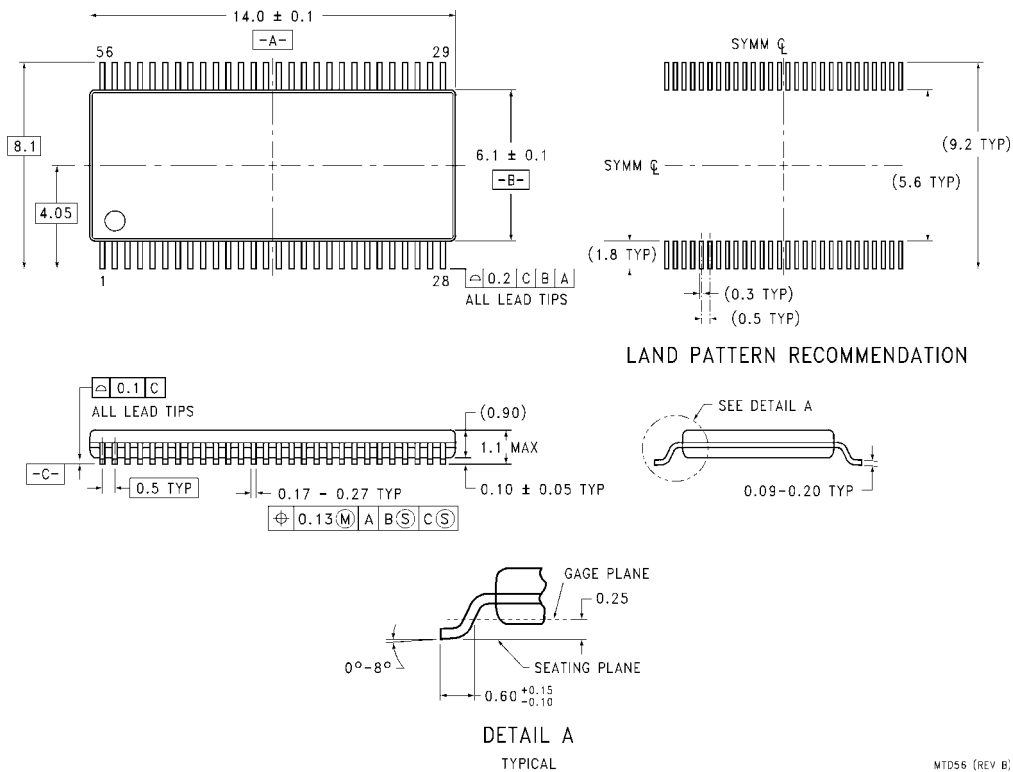


FIGURE 6. 3-STATE Output Low Enable and Disable Times for Low Voltage Logic  
 $t_r = t_f \leq 2.0ns, 10\% \text{ to } 90\%$

Symbol	$V_{CC}$		
	$3.3V \pm 0.3V$	$2.5V \pm 0.2V$	$1.8 \pm 0.15V$
$V_{mi}$	1.5V	$V_{CC}/2$	$V_{CC}/2$
$V_{mo}$	1.5V	$V_{CC}/2$	$V_{CC}/2$
$V_x$	$V_{OL} + 0.3V$	$V_{OL} + 0.15V$	$V_{OL} + 0.15V$
$V_y$	$V_{OH} - 0.3V$	$V_{OH} - 0.15V$	$V_{OH} - 0.15V$

**Physical Dimensions** inches (millimeters) unless otherwise noted



**56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide  
Package Number MTD56**

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

**LIFE SUPPORT POLICY**

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

[www.fairchildsemi.com](http://www.fairchildsemi.com)