



FAST CMOS 16-BIT BIDIRECTIONAL TRANSCEIVER

IDT54/74FCT16245T/AT/CT/ET

FEATURES:

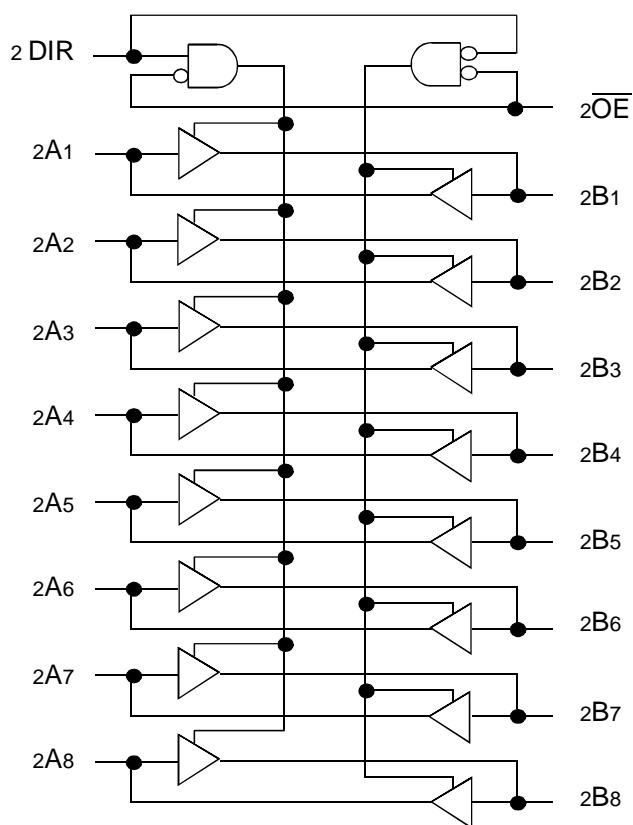
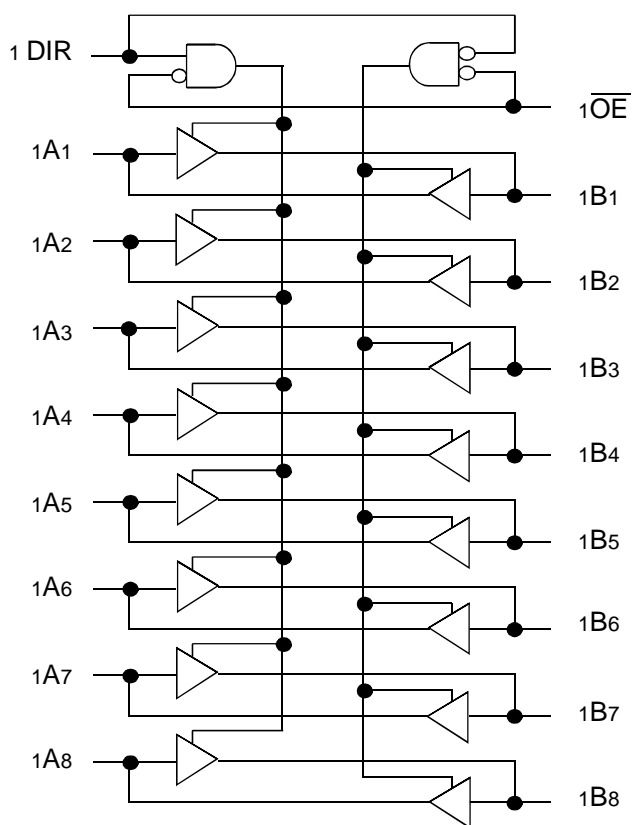
- 0.5 MICRON CMOS Technology
- High-speed, low-power CMOS replacement for ABT functions
- Typical $t_{sk(o)}$ (Output Skew) < 250ps
- Low input and output leakage $\leq 1\mu A$ (max.)
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- High drive outputs (-32mA IOH, 64mA IOL)
- Power off disable outputs permit "live insertion"
- Typical VOLP (Output Ground Bounce) < 1.0V at Vcc = 5V, TA = 25°C
- Available in the following packages:
 - Industrial: SSOP, TSSOP, TVSOP
 - Military: CERPACK

DESCRIPTION:

The FCT16245T 16-bit transceiver is built using advanced dual metal CMOS technology. These high-speed, low-power transceivers are ideal for synchronous communication between two busses (A and B). The Direction and Output Enable controls operate these devices as either two independent 8-bit transceivers or one 16-bit transceiver. The direction control pin (xDIR) controls the direction of data flow. The output enable pin (xOE) overrides the direction control and disables both ports. All inputs are designed with hysteresis for improved noise margin.

The FCT16245T is ideally suited for driving high-capacitance loads and low-impedance backplanes. The output buffers are designed with power off disable capability to allow "live insertion" of boards when used as backplane drivers.

FUNCTIONAL BLOCK DIAGRAM

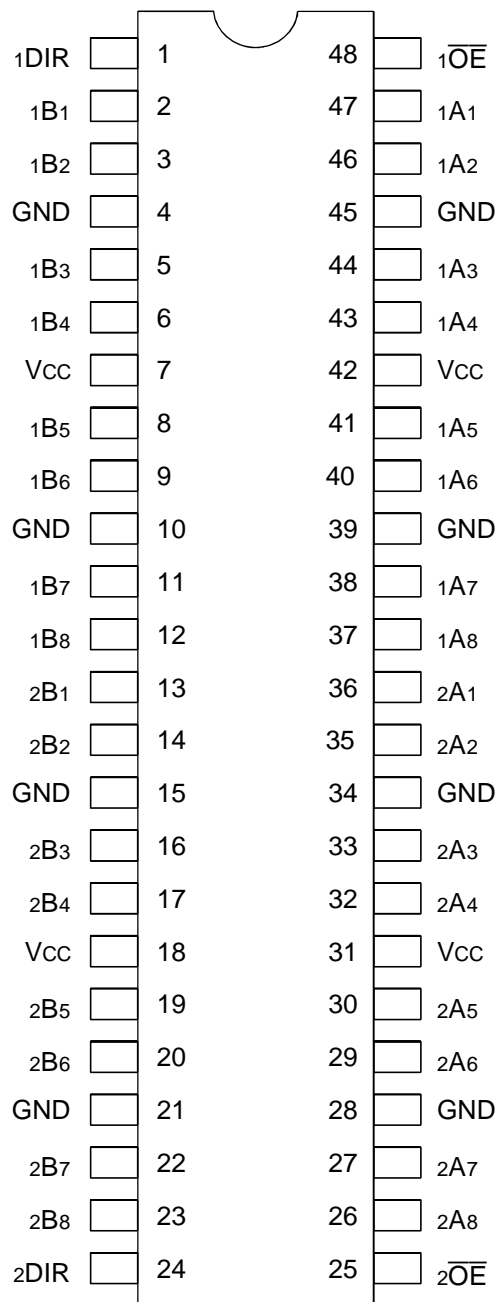


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MILITARY AND INDUSTRIAL TEMPERATURE RANGES

OCTOBER 2003

PIN CONFIGURATION



SSOP/ TSSOP/ TVSOP/ CERPACK
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Description	Max	Unit
VTERM ⁽²⁾	Terminal Voltage with Respect to GND	-0.5 to +7	V
VTERM ⁽³⁾	Terminal Voltage with Respect to GND	-0.5 to Vcc+0.5	V
TSTG	Storage Temperature	-65 to +150	°C
IOUT	DC Output Current	-60 to +120	mA

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. All device terminals except FCT162XXXT and FCT166XXXT (A-Port) Output and I/O terminals.
3. Output and I/O terminals terminals for FCT162XXX and FCT166XXXT (A-Port).

CAPACITANCE (TA = +25°C, F = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
CIN	Input Capacitance	VIN = 0V	3.5	6	pF
COU	Output Capacitance	VOUT = 0V	3.5	8	pF

NOTE:

1. This parameter is measured at characterization but not tested.

PIN DESCRIPTION

Pin Names	Description
xOE	Output Enable Inputs (Active LOW)
xDIR	Direction Control Inputs
xAx	Side A Inputs or 3-State Outputs
xBx	Side B Inputs or 3-State Outputs

FUNCTION TABLE(1)

Inputs		Outputs
xOE	xDIR	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	High Z State

NOTE:

1. H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High-Impedance

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Industrial: $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = 5.0\text{V} \pm 10\%$; Military: $T_A = -55^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{CC} = 5.0\text{V} \pm 10\%$

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
V _{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2	—	—	V
V _{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I _{IH}	Input HIGH Current (Input pins) ⁽⁵⁾	V _{CC} = Max.	V _I = V _{CC}	—	—	±1	μA
	Input HIGH Current (I/O pins) ⁽⁵⁾			—	—	±1	
I _{IL}	Input LOW Current (Input pins) ⁽⁵⁾		V _I = GND	—	—	±1	
	Input LOW Current (I/O pins) ⁽⁵⁾			—	—	±1	
I _{OZH}	High Impedance Output Current (3-State Output pins) ⁽⁵⁾	V _{CC} = Max.	V _O = 2.7V	—	—	±1	μA
I _{OZL}			V _O = 0.5V	—	—	±1	
V _{IK}	Clamp Diode Voltage	V _{CC} = Min., I _{IN} = -18mA		—	-0.7	-1.2	V
I _{OS}	Short Circuit Current	V _{CC} = Max., V _O = GND ⁽³⁾		-80	-140	-250	mA
V _H	Input Hysteresis	—		—	100	—	mV
I _{CCL} I _{CCH} I _{CCZ}	Quiescent Power Supply Current	V _{CC} = Max. V _{IN} = GND or V _{CC}		—	5	500	μA

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
I _O	Output Drive Current	V _{CC} = Max., V _O = 2.5V ⁽³⁾		-50	—	-180	mA
V _{OH}	Output HIGH Voltage	V _{CC} = Min. V _{IN} = V _{IH} or V _{IL}	I _{OH} = -3mA,	-2.5	3.5	—	V
			I _{OH} = -12mA MIL	2.4	3.5	—	V
			I _{OH} = -15mA IND	—	—	—	—
			I _{OH} = -24mA MIL I _{OH} = -32mA IND ⁽⁴⁾	2	3	—	V
V _{OL}	Output LOW Voltage	V _{CC} = Min. V _{IN} = V _{IH} or V _{IL}	I _{OL} = 48mA MIL I _{OL} = 64mA IND	—	0.2	0.55	V
I _{OFF}	Input/Output Power Off Leakage ⁽⁵⁾	V _{CC} = 0V, V _{IN} or V _O ≤ 4.5V		—	—	±1	μA

NOTES:

1. For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
4. Duration of the condition can not exceed one second.
5. The test limit for this parameter is ±5μA at T_A = -55°C.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	$V_{CC} = \text{Max.}$ $V_{IN} = 3.4V^{(3)}$		—	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current ⁽⁴⁾	$V_{CC} = \text{Max.}$ Outputs Open $\overline{xOE} = xDIR = \text{GND}$ One Input Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	60	100	$\mu\text{A}/$ MHz
I_C	Total Power Supply Current ⁽⁶⁾	$V_{CC} = \text{Max.}$ Outputs Open $f_i = 10\text{MHz}$ 50% Duty Cycle $\overline{xOE} = xDIR = \text{GND}$ One Bit Toggling	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	0.6	1.5	mA
			$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$	—	0.9	2.3	
		$V_{CC} = \text{Max.}$ Outputs Open $f_i = 2.5\text{MHz}$ 50% Duty Cycle $\overline{xOE} = xDIR = \text{GND}$ Sixteen Bits Toggling	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	2.4	4.5 ⁽⁵⁾	
			$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$	—	6.4	16.5 ⁽⁵⁾	

NOTES:

1. For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.

2. Typical values are at $V_{CC} = 5.0V$, $+25^\circ\text{C}$ ambient.

3. Per TTL driven input ($V_{IN} = 3.4V$). All other inputs at V_{CC} or GND.

4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.

5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$

$$I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP} / 2 + f_i N_i)$$

I_{CC} = Quiescent Current (I_{CCL} , I_{CCH} and I_{CCZ})

ΔI_{CC} = Power Supply Current for a TTL High Input ($V_{IN} = 3.4V$)

D_H = Duty Cycle for TTL Inputs High

N_T = Number of TTL Inputs at D_H

I_{CCD} = Dynamic Current caused by an Input Transition Pair (HLH or LHL)

f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)

N_{CP} = Number of Clock Inputs at f_{CP}

f_i = Input Frequency

N_i = Number of Inputs at f_i

SWITCHING CHARACTERISTICS OVER OPERATING RANGE - INDUSTRIAL

Symbol	Parameter	Condition ⁽¹⁾	74FCT16245AT		74FCT16245CT		74FCT16245ET		Unit
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
tPLH	Propagation Delay	CL = 50pF RL = 500Ω	1.5	4.6	1.5	4.1	1.5	3.2	ns
tPHL	A to B, B to A								
tPZH	Output Enable Time		1.5	6.2	1.5	5.8	1.5	4.4	ns
tPZL	xOE to A or B								
tPHZ	Output Disable Time		1.5	5	1.5	4.8	1.5	4	ns
tPLZ	xOE to A or B								
tPZH	Output Enable Time		1.5	6.2	1.5	5.8	1.5	4.8	ns
tPZL	xDIR to A or B ⁽⁴⁾								
tPHZ	Output Disable Time	1.5	5	1.5	4.8	1.5	4	ns	
tPLZ	xDIR to A or B ⁽⁴⁾								
tSK(o)	Output Skew ⁽³⁾	—	0.5	—	0.5	—	0.5	ns	

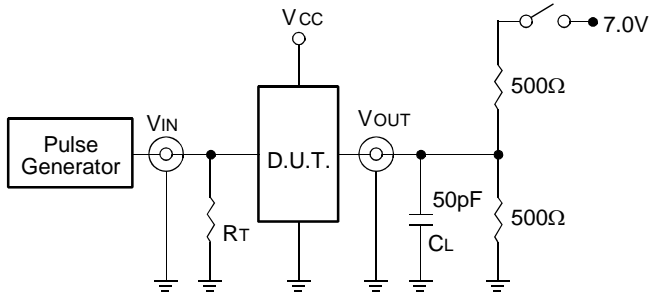
SWITCHING CHARACTERISTICS OVER OPERATING RANGE - MILITARY

Symbol	Parameter	Condition ⁽¹⁾	54FCT16245T		54FCT16245AT		54FCT16245CT		Unit
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
tPLH	Propagation Delay	CL = 50pF RL = 500Ω	1.5	7.5	1.5	4.9	1.5	4.5	ns
tPHL	A to B, B to A								
tPZH	Output Enable Time		1.5	10	1.5	6.5	1.5	6.2	ns
tPZL	xOE to A or B								
tPHZ	Output Disable Time		1.5	10	1.5	6	1.5	5.2	ns
tPLZ	xOE to A or B								
tPZH	Output Enable Time		1.5	10	1.5	6.5	1.5	6.2	ns
tPZL	xDIR to A or B ⁽⁴⁾								
tPHZ	Output Disable Time	1.5	10	1.5	6	1.5	5.2	ns	
tPLZ	xDIR to A or B ⁽⁴⁾								
tSK(o)	Output Skew ⁽³⁾	—	0.5	—	0.5	—	0.5	ns	

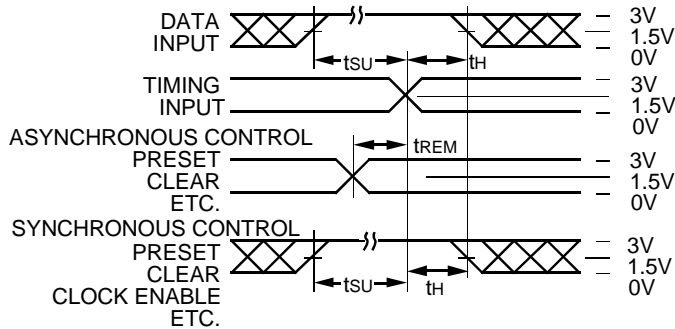
NOTES:

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.
4. This limit is guaranteed but not tested.

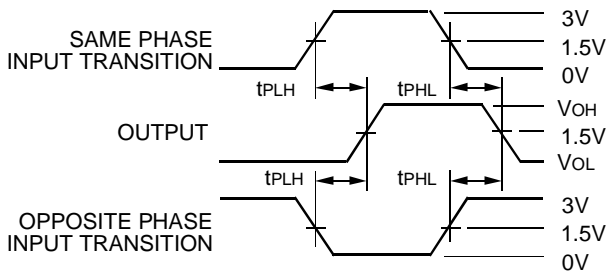
TEST CIRCUITS AND WAVEFORMS



Test Circuits for All Outputs



Set-up, Hold, and Release Times



Propagation Delay

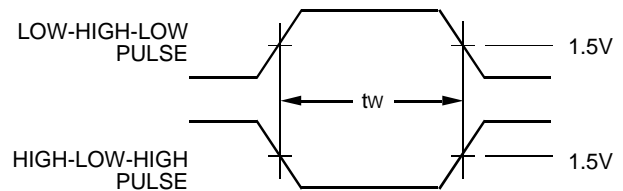
SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

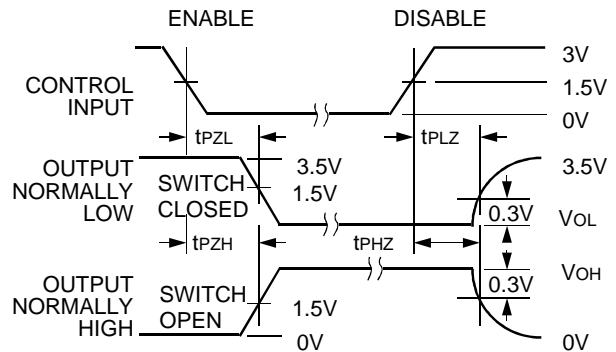
DEFINITIONS:

CL = Load capacitance: includes jig and probe capacitance.

RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.



Pulse Width

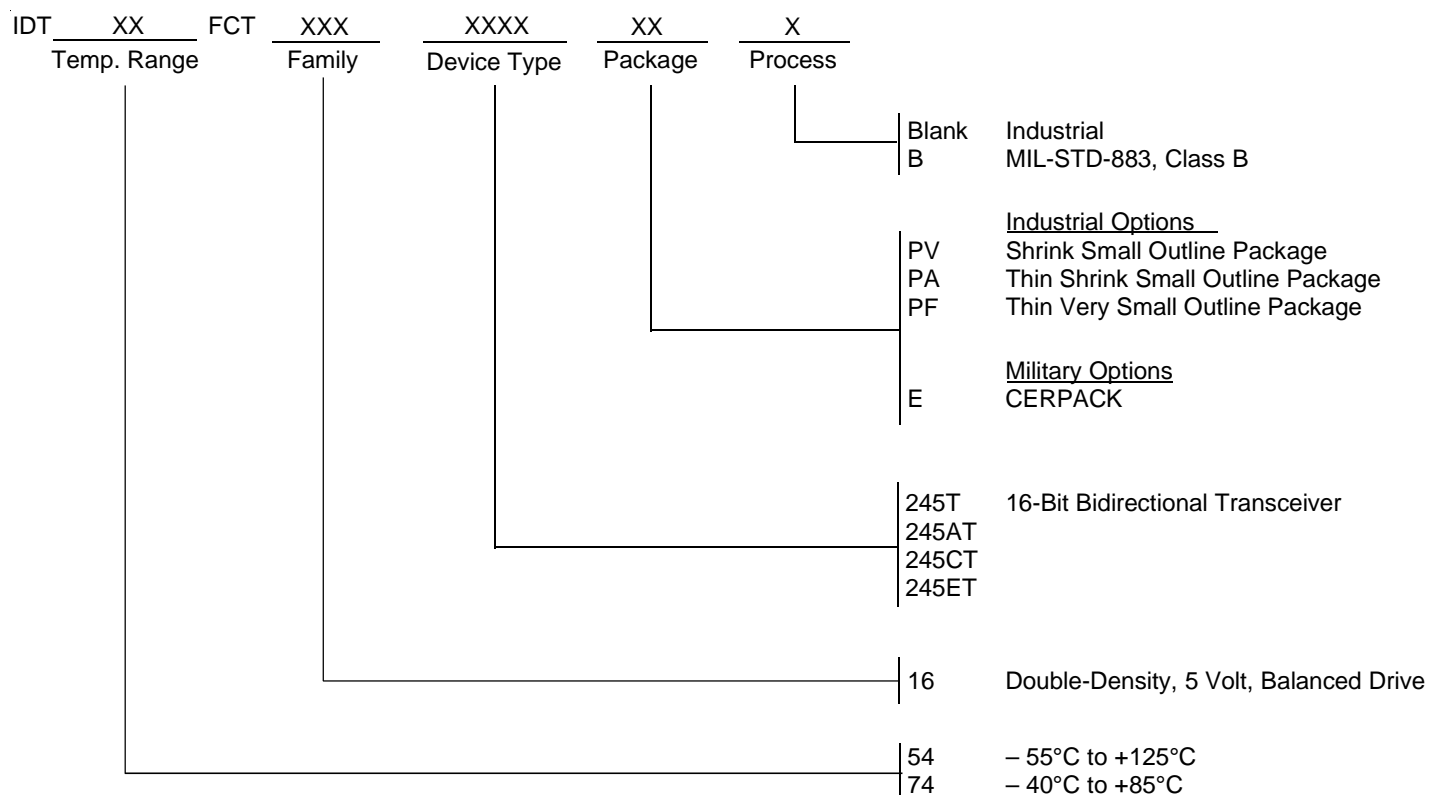


Enable and Disable Times

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate \leq 1.0MHz; $t_f \leq$ 2.5ns; $t_r \leq$ 2.5ns.

ORDERING INFORMATION



DATA SHEET DOCUMENT HISTORY

3/26/2002 Removed standard speed grade

6/26/2002 Updated as per PDNs Logic-00-07 and Logic-01-04

6/5/2003 Removed blank Industrial speed grade as per PDNs Logic-00-07 and Logic-01-04



CORPORATE HEADQUARTERS
2975 Stender Way
Santa Clara, CA 95054

for SALES:
800-345-7015 or 408-727-6116
fax: 408-492-8674
www.idt.com

for Tech Support:
logichelp@idt.com
(408) 654-6459