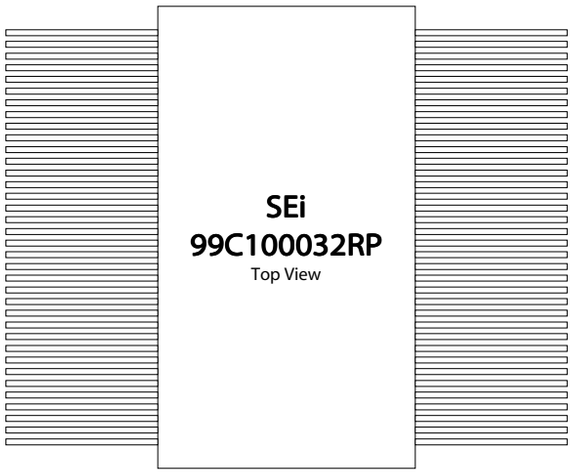
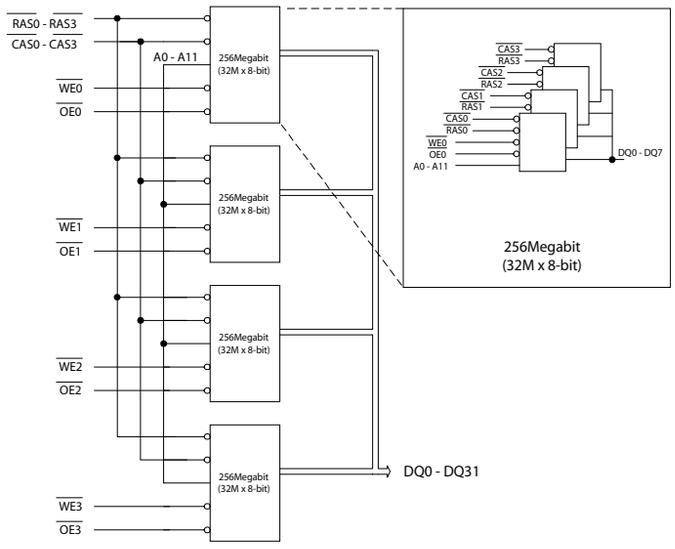
Space Electronics Inc.
Space Products Group

1 Giga Bit Dynamic Random Access Memory (MCM)

99C100032RP



99C100032RP Block Diagram



Features:

- 1 Giga-Bit DRAM
  (Four 256 Megabit DRAM Stacks)
- Rad-Pak® radiation-hardened against natural space radiation
- Total dose hardness: 100 krad (Si) typical; dependent upon orbit
- Single event effect
  -SEL_{TH}: No latchup > 117 MeV/mg/cm^2
- Package:
  - 68 Pin Rad-Pak® flat package
- Access time: 60, 70ns
- Common Data Inputs and Outputs
- EDO or Fast Page Mode Capability
- 4096 Cycles / 64ms Refresh
- 3 Variations of Refresh:
  - $\overline{RAS}$ only Refresh
  - $\overline{CAS}$ before $\overline{RAS}$ Refresh
  - Hidden Refresh
- QCI per TM5005

Description:

Space Electronics' 99C100032RP (RP for Rad-Pak®) 1 Gigabit Dynamic Random Access Memory multi-chip module (MCM) features a typical 100 kilorad (Si) total dose tolerance; dependent upon orbit. The 99C100032RP uses four 256 Megabit stacks to yield a 1 Gigabit product. It has a 32-bit wide data bus that is byte addressable. The 99C100032RP is designed specifically for high-speed, low-power and high-reliability application. The device has $\overline{CAS}$-before $\overline{RAS}$ refresh, $\overline{RAS}$-only refresh and Hidden refresh capabilities. Capable of surviving space environments, the 99C100032RP is ideal for satellite, spacecraft, and space probe missions. Space Electronics' Rad-Pak® incorporates radiation shielding in the microcircuit package. It eliminates box shielding while providing required lifetime in orbit. This product is available with packaging and screening up to Class S.

99C100032RP ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MIN	MAX	UNIT
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-1.0	+7.0	V
Voltage on V_{DD} supply relative to V_{SS}	V_{DD}	-1.0	+7.0	V
Operating Temperature	T_A	-40	+85	°C
Storage Temperature	T_{STG}	-55	+150	°C
Output Current	I_{OUT}	--	200	mA

99C100032RP RECOMMENDED OPERATING CONDITIONS

(VOLTAGE REFERENCED TO V_{SS}, T_A = -40 TO +85 °C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Supply Voltage	V_{DD}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	--	V_{DD} +1.0	V
Input Low Voltage	V_{IL}	-1.0	--	0.8	V

99C100032RP DC CHARACTERISTICS

(RECOMMENDED OPERATING CONDITIONS UNLESS OTHERWISE NOTED.)

PARAMETER	TEST CONDITIONS	SYMBOL	MIN	MAX	UNITS
Input Leakage Current	$\overline{CAS}$, $\overline{RAS}$ A0-A11, $\overline{WE}$, $\overline{OE}$	I_{IN}	-20 -80	+20 +80	uA
Output Leakge Current	Data out is disabled, 0V < V_{OUT} < V_{DD}	I_{OUT}	-20	20	uA
Output High Voltage Level	I_{OH} = -5mA	V_{OH}	2.4	--	V
Output Low Voltage Level	I_{OL} = 4.2mA	V_{OL}	--	0.4	V
Operating Current 99C100032RP-6 99C100032RP-7	$\overline{RAS}$ and $\overline{CAS}$ cycling @ t_{RC} = min	I_{CC1}	 -- --	 584 544	mA
Standby Current	$\overline{RAS}$ = $\overline{CAS}$ = $\overline{WE}$ = V_{IH}	I_{CC2}	--	32	mA
$\overline{RAS}$-only Refresh Current 99C100032RP-6 99C100032RP-7	$\overline{CAS}$ = V_{IH}, $\overline{RAS}$ cycling @ t_{RC} = min	I_{CC3}	 -- --	 584 544	mA
FAST-PAGE-MODE Current 99C100032RP-6 99C100032RP-7	$\overline{RAS}$ = V_{IL} CAS address cycling @ t_{RC} = min	I_{CC4}	 -- --	 304 284	mA
Standby Current	$\overline{RAS}$ = $\overline{CAS}$ = $\overline{WE}$ = V_{DD} - 0.2V	I_{CC5}	--	16	mA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current 99C100032RP-6 99C100032RP-7	$\overline{RAS}$ and $\overline{CAS}$ cycling @ t_{RC} = min	I_{CC6}	 -- --	 584 544	mA

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99C100032RP CAPACITANCE

($T_A = 25°C, V_{DD} = 5.0V, f = 1MHz$)

PARAMETER	SYMBOL	CONDITION	MAX	UNITS
Address Input 1.	C_{ADR}	$V_{IN} = 0V$	120	pF
$\overline{CAS}$ Input 1.	C_{CAS}		45	pF
$\overline{RAS}$ Input 1.	C_{RAS}		45	pF
Write Enable 1.	C_{WE}		140	pF
Output Enable 1.	C_{OE}		140	pF
Data Input/Output 1.	$C_{I/O}$		140	pF

NOTE:
1. NOT TESTED.

99C100032RP AC CHARACTERISTICS

($-40°C \leq T_A \leq 85°C, V_{DD} = 5.0V \pm 10\%, V_{IH}/V_{IL} = 2.0/0.8V, V_{OH}/V_{OL} = 2.0/0.8V$)

PARAMETER	SYMBOL	MIN	MAX	UNITS
Random read or write cycle time 13.	t_{RC}			
99C100032RP-6		110	--	ns
99C100032RP-7		130	--	
Read-modify-write cycle time 13.	t_{RWC}			
99C100032RP-6		155	--	ns
99C100032RP-7		185	--	
Access time for $\overline{RAS}$ 3., 4., 10.	t_{RAC}			
99C100032RP-6		--	60	ns
99C100032RP-7		--	70	
Access time for $\overline{CAS}$ 3., 4., 5.	t_{CAC}			
99C100032RP-6		--	15	ns
99C100032RP-7		--	20	
Access time from column address 3., 10.	t_{AA}			
99C100032RP-6		--	30	ns
99C100032RP-7		--	35	
$\overline{CAS}$ to output in LOW-Z 3.	t_{CLZ}			
99C100032RP-6		0	--	ns
99C100032RP-7		0	--	
Output buffer turn-off delay 6.	t_{OFF}			
99C100032RP-6		0	15	ns
99C100032RP-7		0	20	
Transition time (rise and fall) 2., 12.	t_T			
99C100032RP-6		3	50	ns
99C100032RP-7		3	50	

99C100032RP AC CHARACTERISTICS (cont.)

($-40\,^{\circ}C \leq T_A \leq 85\,^{\circ}C, V_{DD} = 5.0V \pm 10\%, V_{IH}/V_{IL} = 2.0/0.8V, V_{OH}/V_{OL} = 2.0/0.8V$)

PARAMETER	SYMBOL	MIN	MAX	UNITS
$\overline{RAS}$ precharge time 13. 99C100032-6 99C100032-7	t_{RP}	 40 50	 -- --	 ns
$\overline{RAS}$ pulse width 13. 99C100032-6 99C100032-7	t_{RAS}	 60 70	 10K 10K	 ns
$\overline{RAS}$ hold time 99C100032-6 99C100032-7	t_{RSH}	 0 0	 -- --	 ns
$\overline{CAS}$ hold time 99C100032-6 99C100032-7	t_{CSH}	 60 70	 -- --	 ns
$\overline{CAS}$ pulse width 13. 99C100032-6 99C100032-7	t_{CAS}	 15 20	 10K 10K	 ns
$\overline{RAS}$ to $\overline{CAS}$ delay time 4., 12. 99C100032-6 99C100032-7	t_{RCD}	 20 20	 45 50	 ns
$\overline{RAS}$ to column address delay time 10., 14. 99C100032-6 99C100032-7	t_{RAD}	 15 15	 30 35	 ns
$\overline{CAS}$ to $\overline{RAS}$ precharge time 14. 99C100032-6 99C100032-7	t_{CRP}	 5 5	 -- --	 ns
Row address set-up time 99C100032-6 99C100032-7	t_{ASR}	 0 0	 -- --	 ns
Row address hold time 99C100032-6 99C100032-7	t_{RAH}	 10 10	 -- --	 ns
Column address set-up time 99C100032-6 99C100032-7	t_{ASC}	 0 0	 -- --	 ns
Column address hold time 99C100032-6 99C100032-7	t_{CAH}	 10 15	 -- --	 ns
Column address to $\overline{RAS}$ lead time 14. 99C100032-6 99C100032-7	t_{RAL}	 30 35	 -- --	 ns

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99C100032RP AC CHARACTERISTICS (cont.)

($-40\,^{\circ}C \leq T_A \leq 85\,^{\circ}C, V_{DD} = 5.0V \pm 10\%, V_{IH}/V_{IL} = 2.0/0.8V, V_{OH}/V_{OL} = 2.0/0.8V$)

PARAMETER	SYMBOL	MIN	MAX	UNITS
Read command set-up time 99C100032RP-6 99C100032RP-7	t_{RCS}	 0 0	 -- --	 ns
Read command hold time referenced to $\overline{CAS}$ 8., 14. 99C100032RP-6 99C100032RP-7	t_{RCH}	 0 0	 -- --	 ns
Read command hold time referenced to $\overline{RAS}$ 8., 14. 99C100032RP-6 99C100032RP-7	t_{RRH}	 0 0	 -- --	 ns
Write command hold time 13. 99C100032RP-6 99C100032RP-7	t_{WCH}	 10 15	 -- --	 ns
Write command pulse width 13. 99C100032RP-6 99C100032RP-7	t_{WP}	 10 15	 -- --	 ns
Write command to $\overline{RAS}$ lead time 14. 99C100032RP-6 99C100032RP-7	t_{RWL}	 15 20	 -- --	 ns
Write command to $\overline{CAS}$ lead time 14. 99C100032RP-6 99C100032RP-7	t_{CWL}	 15 20	 -- --	 ns
Data set-up time 9. 99C100032RP-6 99C100032RP-7	t_{DS}	 0 0	 -- --	 ns
Data hold time 9. 99C100032RP-6 99C100032RP-7	t_{DH}	 10 15	 -- --	 ns
Refresh Period 99C100032RP-6 99C100032RP-7	t_{REF}	 -- --	 64 64	 ms
Write command set-up time 7., 13. 99C100032RP-6 99C100032RP-7	t_{WCS}	 0 0	 -- --	 ns
$\overline{CAS}$ to $\overline{WE}$ delay time 7., 13. 99C100032RP-6 99C100032RP-7	t_{CWD}	 40 50	 -- --	 ns
$\overline{RAS}$ to $\overline{WE}$ delay time 7., 13. 99C100032RP-6 99C100032RP-7	t_{RWD}	 85 100	 -- --	 ns

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99C100032RP AC CHARACTERISTICS (cont.)

($-40\,^{\circ}C \le T_A \le 85\,^{\circ}C, V_{DD} = 5.0V \pm 10\%, V_{IH}/V_{IL} = 2.0/0.8V, V_{OH}/V_{OL} = 2.0/0.8V$)

PARAMETER	SYMBOL	MIN	MAX	UNITS
Column address to $\overline{WE}$ delay time 7., 14.	t_{AWD}			
99C100032RP-6		55	--	ns
99C100032RP-7		65	--	
$\overline{CAS}$ precharge to $\overline{WE}$ delay time 14.	t_{CPWD}			
99C100032RP-6		60	--	ns
99C100032RP-7		70	--	
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh) 13.	t_{CSR}			
99C100032RP-6		10	--	ns
99C100032RP-7		10	--	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh) 11., 13.	t_{CHR}			
99C100032RP-6		10	--	ns
99C100032RP-7		15	--	
$\overline{RAS}$ to $\overline{CAS}$ precharge time 14.	t_{RPC}			
99C100032RP-6		5	--	ns
99C100032RP-7		5	--	
Fast Page mode cycle time 13.	t_{PC}			
99C100032RP-6		40	--	ns
99C100032RP-7		45	--	
Fast Page mode read-modify-write cycle time 13.	t_{PRWC}			
99C100032RP-6		85	--	ns
99C100032RP-7		100	--	
$\overline{CAS}$ precharge time (Fast Page cycle) 13.	t_{CP}			
99C100032RP-6		10	--	ns
99C100032RP-7		10	--	
$\overline{RAS}$ pulse width (Fast Page cycle) 13.	t_{RASP}			
99C100032RP-6		60	200K	ns
99C100032RP-7		70	200K	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge 14.	t_{RHCP}			
99C100032RP-6		35	--	ns
99C100032RP-7		40	--	
$\overline{OE}$ access time	t_{OEA}			
99C100032RP-6		--	15	ns
99C100032RP-7		--	20	
$\overline{OE}$ to data delay	t_{OED}			
99C100032RP-6		15	--	ns
99C100032RP-7		20	--	
Output to buffer turn off delay time from $\overline{OE}$ 6.	t_{OEZ}			
99C100032RP-6		0	15	ns
99C100032RP-7		0	20	

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99C100032RP AC CHARACTERISTICS (cont.)

($-40\,^{\circ}C \le T_A \le 85\,^{\circ}C, V_{DD} = 5.0V \pm 10\%, V_{IH}/V_{IL} = 2.0/0.8V, V_{OH}/V_{OL} = 2.0/0.8V$)

PARAMETER	SYMBOL	MIN	MAX	UNITS
$\overline{OE}$ command hold time	t_{OEH}			
99C100032RP-6		15	--	ns
99C100032RP-7		20	--	
$\overline{WE}$ to $\overline{RAS}$ precharge time (C-B-R refresh) 13.	t_{WRP}			
99C100032RP-6		10	--	ns
99C100032RP-7		10	--	
$\overline{WE}$ to $\overline{RAS}$ hold time (C-B-R refresh) 13.	t_{WRH}			
99C100032RP-6		10	--	ns
99C100032RP-7		10	--	

NOTE:

1. An initial pause of 200 µs is required after power-up followed by any 8 $\overline{RAS}$ refresh cycles ($\overline{RAS}$-ONLY or CBR) before proper device operation is achieved.
2. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} (min) and V_{IL} (max) and are assumed to be 5ns for all inputs
3. Measured with a load equivalent to 2 TTL load and 100 pF.
4. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \ge t_{RCD}$ (max).
6. t_{OFF} (max) and t_{OEZ} (max) define the time at which the output achieves the open circuit condition and are not referenced to V_{OH} or V_{OL}.
7. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If $t_{WCS} \ge t_{WCS}$ (min), the cycles in an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \ge t_{CWD}$ (min), $t_{RWD} \ge t_{RWD}$ (min) and $t_{AWD} \ge t_{AWD}$ (min), then the cycle is a read-modify-write cycle and the data output will contain the data read from the selection address. If neither of the above conditions is satisfied, the condition of the data out is indeterminable.
8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{WE}$ leading edge in read-modify-write cycles.
10. Operation within the t_{RAD} (max) limit insures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled by t_{AA}.
11. It can get less $\overline{CAS}$-before-$\overline{RAS}$ current loss if $t_{CHR} \ge t_{RAS}$ or $\overline{CAS} < 0.2V$ at $\overline{CAS}$-before-$\overline{RAS}$ refresh mode.
12. Guaranteed by design.
13. Parameters are tested functionally.
14. Not tested.

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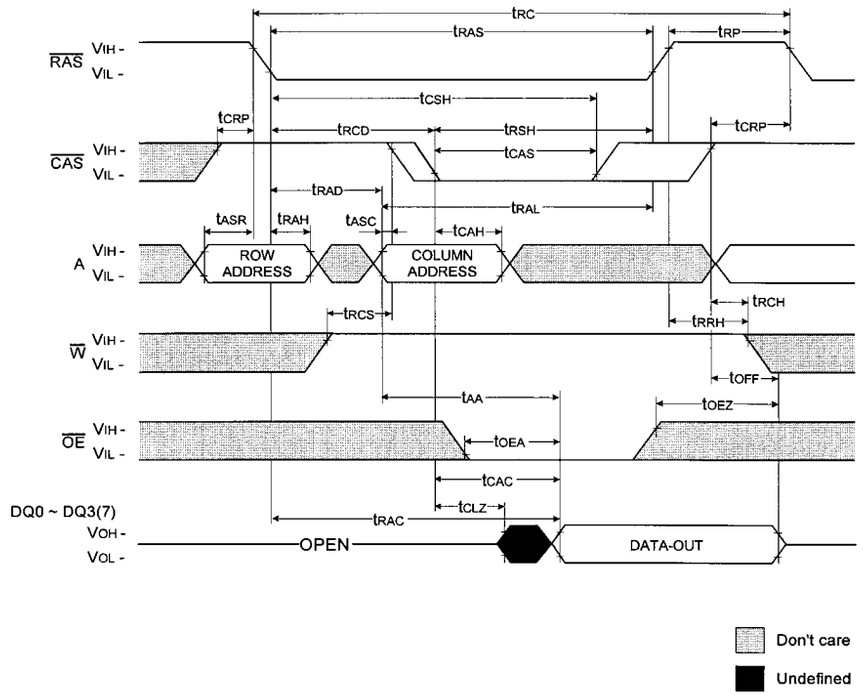
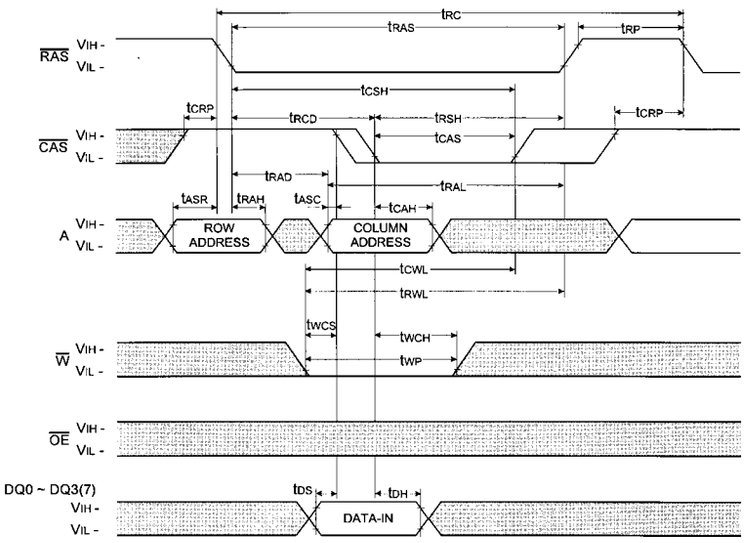
READ CYCLE



WRITE CYCLE (EARLY WRITE)

NOTE : DOUT = OPEN



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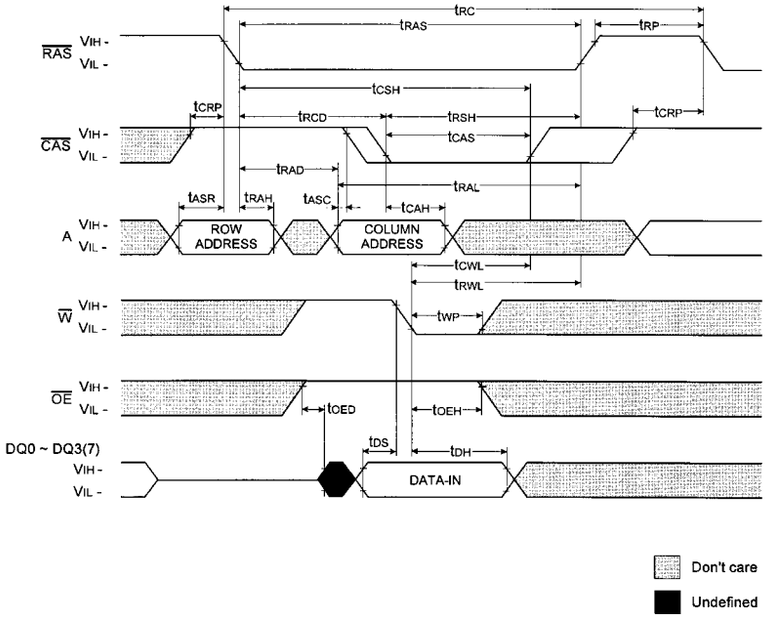
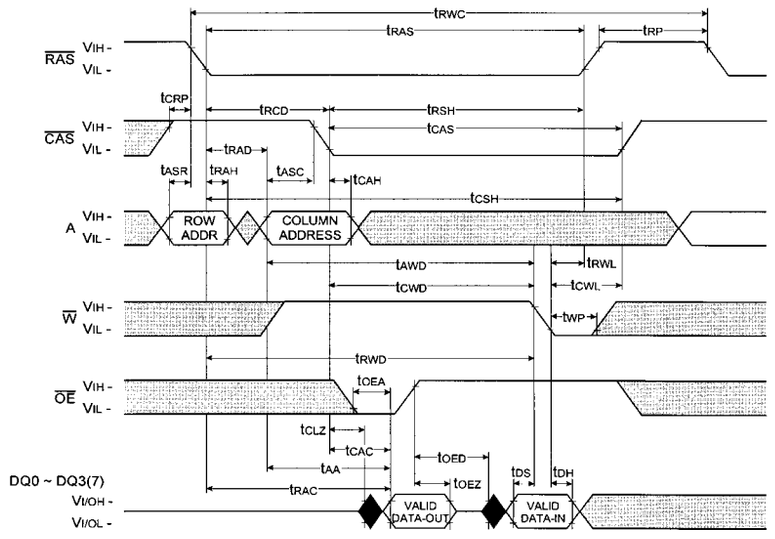
WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

NOTE : DOUT = OPEN



READ - MODIFY - WRTIE CYCLE



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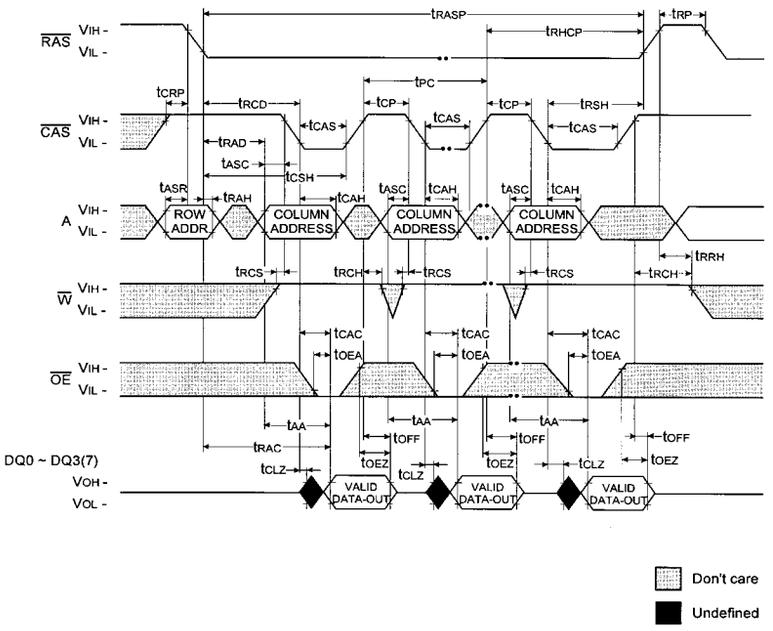
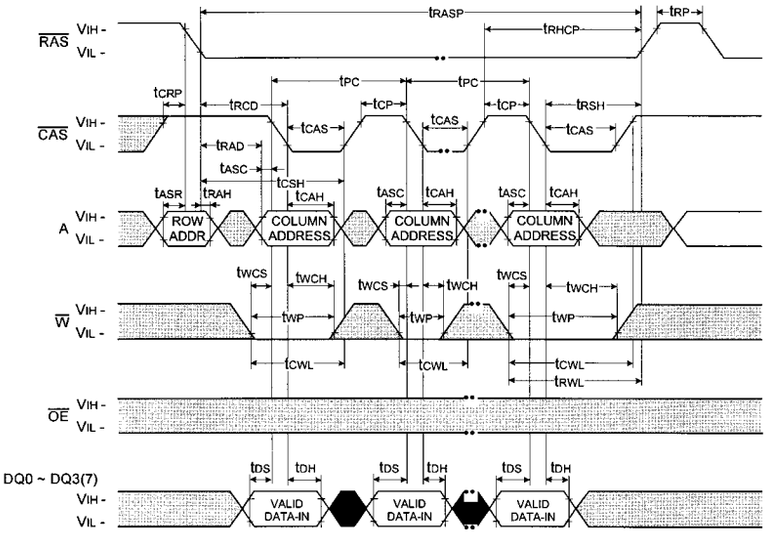
FAST PAGE READ CYCLE

NOTE : DOUT = OPEN



FAST PAGE WRITE CYCLE (EARLY WRITE)

NOTE : DOUT = OPEN



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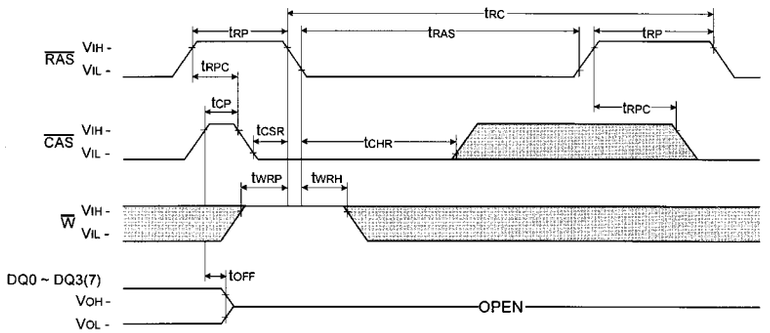
$\overline{CAS}$ - BEFORE - $\overline{RAS}$ REFRESH CYCLE

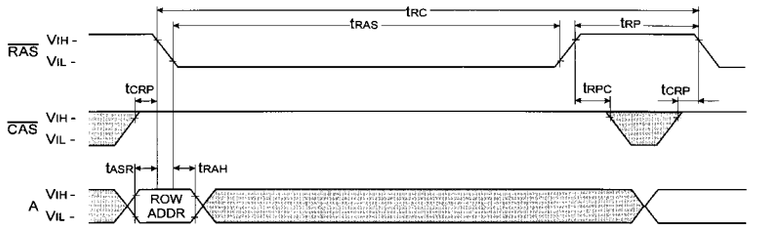
NOTE : $\overline{OE}$, A = Don't care



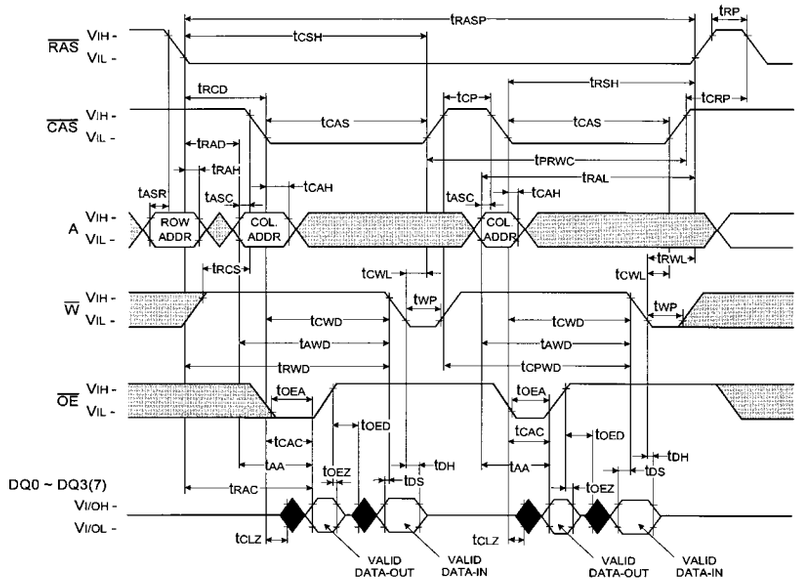
$\overline{RAS}$ - ONLY REFRESH CYCLE

NOTE : $\overline{W}$, $\overline{OE}$, DIN = Don't care

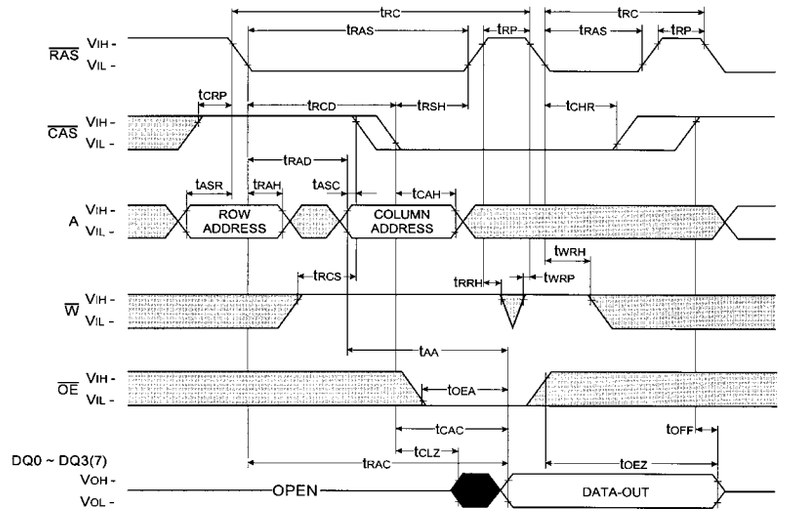
DOUT = OPEN



FAST PAGE READ - MODIFY - WRITE CYCLE

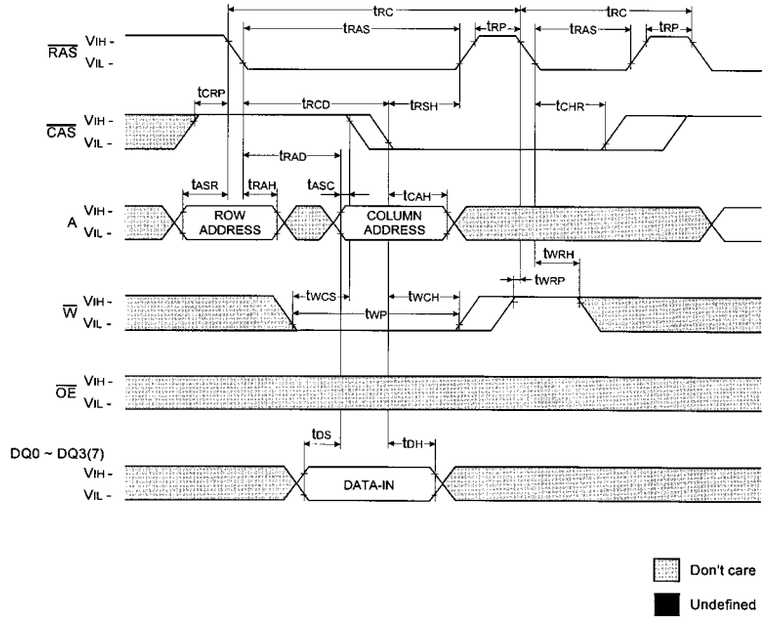


HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)

NOTE : DOUT = OPEN



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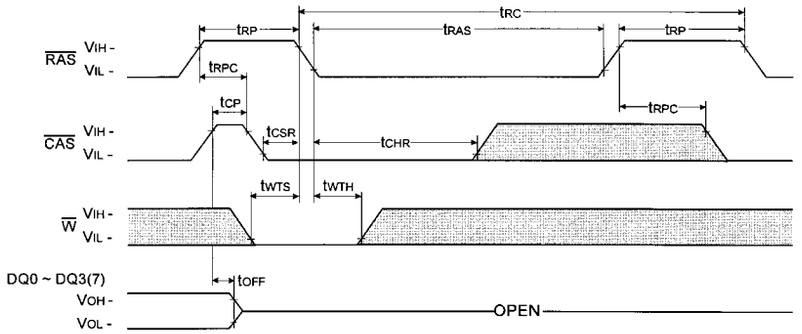
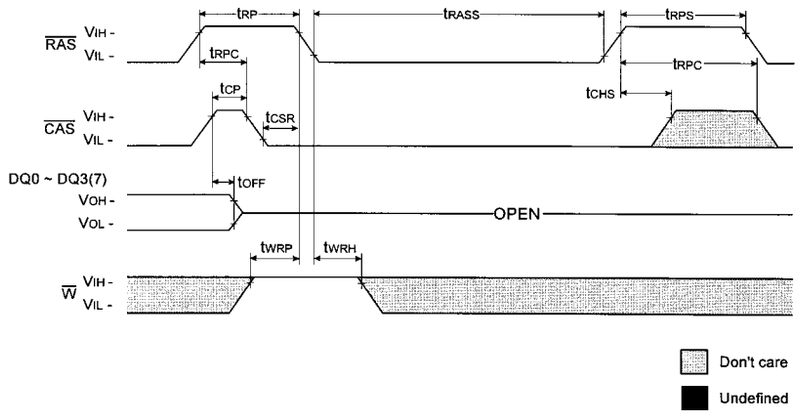
TEST MODE IN CYCLE

NOTE : $\overline{OE}$, A = Don't care



$\overline{CAS}$ - BEFORE - $\overline{RAS}$ SELF REFRESH CYCLE

NOTE : $\overline{OE}$, A = Don't care



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99C100032RP PINOUT DIAGRAM

Vcc	1	68	Vss
DQ0	2	67	DQ31
DQ1	3	66	DQ30
DQ2	4	65	DQ29
DQ3	5	64	DQ28
DQ4	6	63	DQ27
DQ5	7	62	DQ26
DQ6	8	61	DQ25
DQ7	9	60	DQ24
DQ8	10	59	DQ23
DQ9	11	58	DQ22
DQ10	12	57	DQ21
DQ11	13	56	DQ20
DQ12	14	55	DQ19
DQ13	15	54	DQ18
DQ14	16	53	DQ17
DQ15	17	52	DQ16
Vcc	18	51	Vss
$\overline{WE0}$	19	50	$\overline{CAS0}$
$\overline{WE1}$	20	49	$\overline{CAS1}$
$\overline{WE2}$	21	48	$\overline{CAS2}$
$\overline{WE3}$	22	47	$\overline{CAS3}$
$\overline{RAS0}$	23	46	$\overline{OE0}$
$\overline{RAS1}$	24	45	$\overline{OE1}$
$\overline{RAS2}$	25	44	$\overline{OE2}$
RAS3	26	43	OE3
Vcc	27	42	Vss
A0	28	41	A11
A1	29	40	A10
A2	30	39	A9
A3	31	38	A8
A4	32	37	A7
A5	33	36	A6
Vcc	34	35	Vss

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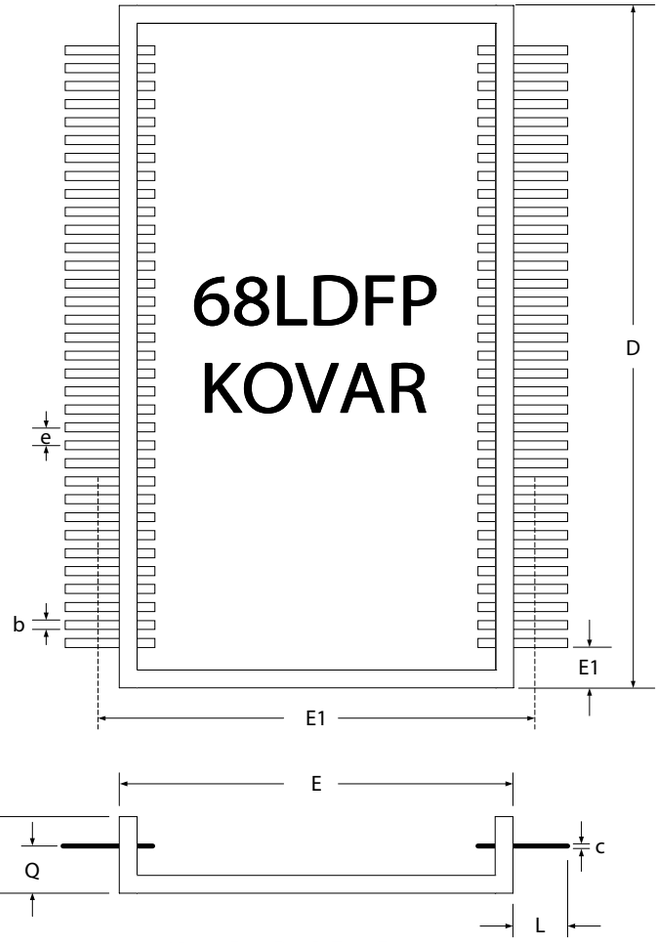

68-PIN RAD-PAK® FLAT PACKAGE

SYMBOL	DIMENSION		
	MIN	NOM	MAX
A	0.363	0.370	0.377
b	0.010	0.015	0.020
c	0.005	0.010	0.015
D	2.395	2.400	2.405
E	1.660	1.665	1.670
E1	--	--	1.865
e	0.050 BSC		
L	0.500	--	
Q	0.182	0.195	0.208
S1	0.363	0.368	0.373
N	68		

F68-01

NOTE: ALL DIMENSIONS IN INCHES.

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