G-LINK Technology

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GLT6100L08/M08/N08

128K x 8 Super Low Power & Low Voltage SRAM

FEATURES

- ◆ Organization: 128K x 8
- ◆ Low Data Retention Voltage: 1.5 V (min)
- ◆ Power Supply Voltage
  - GLT6100L08: 2.7 V ~ 3.6 V
  - GLT6100M08: 2.3 V ~ 2.7 V
  - GLT6100N08: 1.8 V ~ 2.3 V
- ◆ Maximum 1 μA Standby Current
- ◆ Three-state output status and TTL compatible
- ◆ Package type; JEDEC standard 32-Pin SOP, 32-Pin TSOP I, 32-Pin Shrink TSOP I

Product Family

Organization	Part Number	V_{CC}	Isb1	Speed	Temperature
128Kx8	GLT6100L/LI	2.7 ~ 3.6 V	1 μa	70/85/100	Commercial: 0 to +70°C Industrial: -40 to +85°C
128Kx8	GLT6100M/MI	2.3 ~2.7 V	1 μa	85/100/120	
128Kx8	GLT6100N/NI	1.8 ~ 2.3 V	1 μa	120/150/300	

GENERAL DESCRIPTION

The GLT 6100L08/M08/N08 Super Low-Power SRAM family can support various voltage and operating temperature ranges and has various package types for user flexibility of system design. The family also support low data retention voltage for battery back-up operations with low data retention current.

Functional Block Diagram

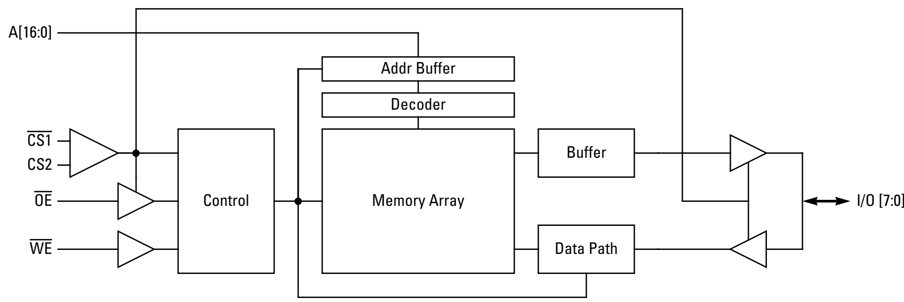


Figure 1. GLT6100L08/M08/N08 128K x 8

Signal Descriptions

Symbol	Type	Description
A[16:0]	Input	Address Inputs
$\overline{WE}$	Control	Write Enable Input
$\overline{CS1}$	Control	Chip Select Input
CS2	Control	Chip Select Input
$\overline{OE}$	Control	Output Enable Input
I/O[7:0]	I/O	Data Input/Output
V_{CC}	Power	Power
V_{SS}	Power	Ground
NC	N/A	No Connection

Functional Truth Table [1]

$\overline{CS1}$	CS2	$\overline{WE}$	$\overline{OE}$	Mode	I/O [7:0]	Current Mode
H	X	X	X	Not Select	High-Z	I_{SB}[1]
X	L	X	X	Not Select	High-Z	I_{SB}[1]
L	H	H	H	Output Disable	High-Z	I_{CC}
L	H	H	L	Read	D_{OUT}	I_{CC}
L	H	L	X	Write	D_{IN}	I_{CC}

1. X means don't care (High or Low)

Electrical Specifications

Absolute Maximum Ratings [1]

Parameter		Rating
Voltage on any Pin Relative to V_{SS}		-0.2 V to V_{CC} + 0.5 V
Voltage on V_{CC} Supply Relative to V_{SS}		-0.2 V to 4.0 V
Power Dissipitation		1.0 W
Storage Temperature		-55 °C to +150 °C
Operation Temperature	Commercial	0 °C to +70 °C
	Industrial	-40 °C to +85 °C
Soldering Temperature and Time		260 °C, 5 Sec (Lead Only)

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions [1] [2]

Symbol	Description	Product	Min	Typ [3]	Max	Units
V_{CC}	Supply Voltage	GLT6100L	2.7	3.3	3.6	V
		GLT6100M	2.3	2.5	2.7	V
		GLT6100N	1.8	2.0	2.3	V
V_{SS}	Ground	All Family	0	0	0	V
V_{IH}	Input High Voltage	GLT6100L	2.2	–	V_{CC} + 0.2 [4]	V
		GLT6100M	2.0	–	V_{CC} + 0.2 [4]	V
		GLT6100N	1.6	–	V_{CC} + 0.2 [4]	V
V_{IL}	Input Low Voltage	All Family	-0.2 [5]	–	0.4	V

1. Commercial product: T_A = 0 to +70 °C, unless otherwise specified.
2. Industrial Product: T_A = -40 to +85 °C, unless specified otherwise
3. T_A = 25 °C
4. V_{IH} (max) = V_{CC} + 1.0 V for ≤ 20 ns pulse width
5. V_{IL} (min) = -1.0V for ≤ 20 ns pulse width

Capacitance [1] (f = 1MHz, T_A = 25°C)

Symbol	Description	Conditions	Min	Max	Units
C_{IN}	Input Capacitance	V_{IN} = 0 V	-	8	pF
C_{IO}	Input/Output Capacitance	V_{IO} = 0 V	-	10	pF

1. Capacitance is sampled, not 100% tested

DC Characteristics

Symbol	Description		Test Conditions [1]			Min	TYP	Max	Units
I_{LI}	Input Leakage Current		$V_{IN} = V_{SS}$ to V_{CC}			-1	–	1	µA
I_{LO}	Output Leakage Current		$\overline{CS1} = V_{IH}$ or $CS2 = V_{IL}$ or $\overline{WE} = V_{IL}$, or $\overline{OE} = V_{IH}$ $V_{IO} = V_{SS}$ to V_{CC}			-1	–	1	µA
I_{CC}	Operating Power Supply Current		$\overline{CS1} = V_{IL}$, $CS2 = V_{IH}$, $V_{IN} = V_{IH}$ or V_{IL}, $I_{IO} = 0$ mA			–	–	3 [2]	mA
I_{CC1}	Average Operating Current		Cycle time = 1 µs, 100% duty, $\overline{CS1} \le 0.2V$, $CS2 \ge V_{CC} - 0.2V$, $I_{IO} = 0$ mA, $V_{IN} \le 0.2$ V, or $V_{IN} \ge V_{CC} - 0.2$ V			–	–	5 [2]	mA
I_{CC2}	Average Operating Current		$\overline{CS1} = V_{IL}$, $CS2 = V_{IH}$, $I_{IO} = 0$ mA Min cycle, 100% duty $V_{IN} = V_{IL}$ or V_{IH}		$V_{CC} = 3.3V$ @ 70 ns	–	–	40 [3]	mA
					$V_{CC} = 2.7V$ @ 85 ns	–	–	25	
					$V_{CC} = 2.2V$ @ 120 ns	–	–	15	
V_{OL}	Output Low Voltage		L_{OL}	$V_{CC} = 3.0/3.3V$	2.1 mA	–	–	0.4	V
				$V_{CC} = 2.5V$	0.5 mA	–	–	0.4	
				$V_{CC} = 2.0V$	0.33 mA	–		0.4	
V_{OH}	Output High Voltage		L_{OH}	$V_{CC} = 3.0/3.3V$	-1.0 mA	2.4	–	–	V
				$V_{CC} = 2.5V$	-0.5 mA	2.0	–	–	
				$V_{CC} = 2.0V$	-0.44 mA	1.6	–	–	
I_{SB}	Standby Current (TTL)		$CS2 \le V_{IL}$ or $\overline{CS1} \ge V_{IH}$, $CS2 \ge V_{IH}$			–	–	0.3	mA
I_{SB1}	Standby Current (CMOS)	GLT6100x08SL	$\overline{CS1} \ge V_{CC} - 0.2V$, $CS2 \ge V_{CC} - 0.2V$ or $CS2 \le 0.2V$		Super Low Power	–	0.05 [4]	1 [5]	µA
		GLT6100x08LL			Low Low Power	–	–	5 [6]	µA

1. Commercial Products
   T_A = 0 to 70°C, V_{CC} = 2.7 ~ 3.6V for GLT6100L Family, VCC = 2.3 (min) ~ 2.7V (max) for GLT6100M Family, V_{CC} = 1.8 (min) ~ 2.3V (max) for GLT6100N Family
   Industrial Product
   T_A = -40 to 85°C, V_{CC} = 2.7 ~ 3.6V for GLT6100LI Family, V_{CC} = 2.3 (min) ~ 2.7V (max) for GLT6100MI Family, V_{CC} = 1.8 (min) ~ 2.3V (max) for GLT6100NI Family
2. The Value is measured at V_{CC} = 3.6V. The value measured at V_{CC} = 2.5/2.0V ± 0.2 is under the value of V_{CC} = 3.6V
3. I_{CC2} = 40 mA with 70 ns cycle at V_{CC} = 2.7 ~ 3.6V, but the value is not 100% tested but obtained statistically
   I_{CC2} = 25 mA with 120 ns cycle at V_{CC} = 2.5V ± 0.2, but the value is not 100% tested but obtained statistically
   I_{CC2} = 15 mA with 300 ns cycle at V_{CC} = 1.8~ 2.3V, but the value is not 100% tested but obtained statistically
4. The value is not 100% tested but obtained statistically at Temp = 25°C
5. The value has a difference by ± 1 µA.
6. I_{SB1} = 5µA for V_{CC} = 2.3 ~ 3.6V
   I_{SB1} = 3µA for V_{CC} = 1.8 ~ 2.3V

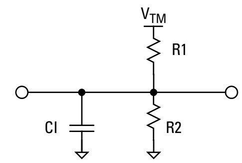
AC Timing Characteristics

Symbol	Parameter		-70		-85		-100		-120		-150		-300		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{RC}	Read	Read Cycle Time	70	-	85	-	100	-	120	-	150	-	300	-	ns
t_{AA}		Address Access Time	-	70	-	85	-	100	-	120	-	150	-	300	ns
t_{CO}		Chip Select to Output	-	70	-	85	-	100	-	120	-	150	-	300	ns
t_{OE}		Output Enable to Valid Output	-	35	-	45	-	50	-	60	-	75	-	150	ns
t_{LZ}		Chip Select To Low-Z Output	10	-	10	-	10	-	10	-	20	-	50	-	ns
t_{OLZ}		Output enable to Low-Z Output	5	-	5	-	5	-	5	-	10	-	30	-	ns
t_{HZ}		Chip Disable To High-Z Output	0	25	0	25	0	30	0	35	0	40	0	60	ns
t_{OHZ}		Output Disable to High-Z Output	0	25	0	25	0	30	0	35	0	40	0	60	ns
t_{OH}		Output Hold From Address Change	10	-	15	-	15	-	15	-	15	-	30	-	ns
t_{WC}	Write	Write Cycle Time	70	-	85	-	100	-	120	-	150	-	300	-	ns
t_{CW}		Chip Select to end of Write	65	-	70	-	80	-	100	-	120	-	300	-	ns
t_{AS}		Address Set-up time	0	-	0	-	0	-	0	-	0	-	0	-	ns
t_{AW}		Address Valid to end of Write	65	-	70	-	80	-	100	-	120	-	300	-	ns
t_{WP}		Write Pulse Width	55	-	60	-	70	-	80	-	100	-	200	-	ns
t_{WR}		Write Recovery time	0	-	0	-	0	-	0	-	0	-	0	-	ns
t_{WHZ}		Write To Output High-Z	0	25	0	25	0	30	0	35	0	40	0	60	ns
t_{DW}		Data to Write Time Overlap	30	-	35	-	40	-	50	-	60	-	120	-	ns
t_{DH}		Data Hold From Write Time	0	-	0	-	0	-	0	-	0	-	0	-	ns
t_{OW}		End Write To Output Low-Z	5	-	5	-	5	-	5	-	5	-	20	-	ns

Test Load and Input/Output Reference [1]

Item	Value	Remark
Input Pulse Level	0.4 V to 2.2 V	V_{CC} = 3.3 V, 3.0 V, 2.5 V
	0.4 V to 1.8 V	V_{CC} = 2.0 V
Input Rise Fall Time	5 ns	-
Input And Output Reference Voltage	1.5 V 1.1 V 0.9 V	V_{CC} = 3.3 V, 3.0 V V_{CC} = 2.5 V V_{CC} = 2.0 V
Output Load	C_L = 100 PF + 1TTL	See Test Condition #2
	C_L = 30 PF + 1TTL	

1. See test condition of DC and Operating Characteristics



NOTE:
1. Including Scope and jig capacitance
2. R1 = 3070Ω, R2 = 3150Ω
3. V_{TM} = 2.8 for V_{CC} = 3.0/3.3V, 2.3V for V_{CC} = 2.5V, 1.8 V for V_{CC} = 2.0V

Figure 2.

Temperature and V_{CC} Conditions

Product Family	Temperature	V_{CC} Range	Typical Supply VCC	Speed (ns)
GLT6100N	Commercial 0 °C to +70°C	1.8 (min) ~ 2.3V (max)	2.0 ± 0.2V	120 [1] / 150 / 300
GLT6100M		2.3 (min) ~ 2.7V (max)	2.5 ± 0.2V	85 [1] / 100 / 120
GLT6100L		2.7 (min) ~ 3.6V (max)	3.0 ± 0.3V	70 [1] / 85 / 100
GLT6100L		3.0 (min) ~ 3.6V (max)	3.3 ± 0.3V	70 [1] / 85 / 100
GLT6100NI	Industrial -40 °C to +85°C	1.8 (min) ~ 2.3V (max)	2.0 ± 0.2V	120 [1] / 150 / 300
GLT6100MI		2.3 (min) ~ 2.7V (max)	2.5 ± 0.2V	85 [1] / 100 / 120
GLT6100LI		2.7 (min) ~ 3.6V (max)	3.0 ± 0.3V	70 [1] / 85 / 100
GLT6100LI		3.0 (min) ~ 3.6V (max)	3.3 ± 0.3V	70 [1] / 85 / 100

1. Parameters are measured with 30 pF test load

Data Retention Characteristics

Symbol	Description	Conditions		Min	Typ	Max	Units
V_{DR}	V_{CC} For Data Retention	$\overline{CS1} \geq V_{CC}$ - 0.2 V, CS2 $\geq V_{CC}$ - 0.2 V or CS2 $\leq$ 0.2 V		1.5	-	3.6	V
I_{DR}	Data Retention Current	V_{CC} = 3.0 V $\overline{CS1} \geq V_{CC}$ - 0.2 V, CS2 $\geq V_{CC}$ - 0.2 V or CS2 $\leq$ 0.2 V	Super Low Power	-	-	1 [1]	μA
			Low Low Power	-	-	5 [1]	
t_{SDR}	Data Retention Set-up Time	See Data Retention Waveform		0	-	-	ns
t_{RDR}	Recovery Time			t_{RC}	-	-	

1. IDR = 2μA for low low power at V_{CC} = 1.5V
   IDR = 0.5μA for super low power at V_{CC} = 1.5V and need special handling.

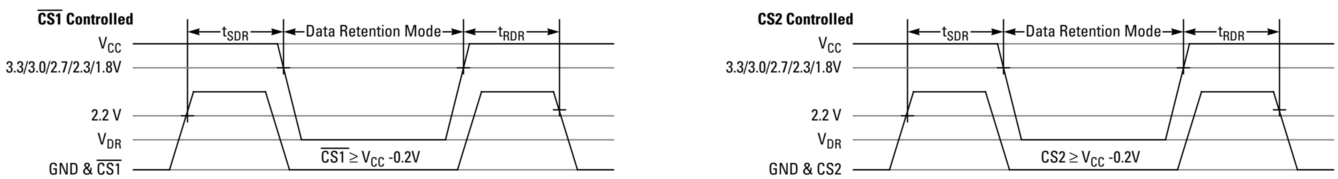
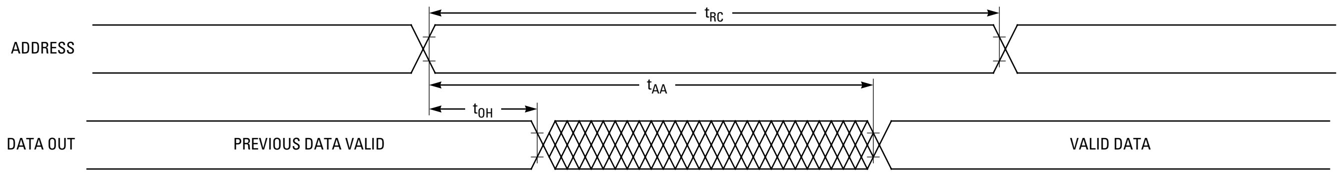
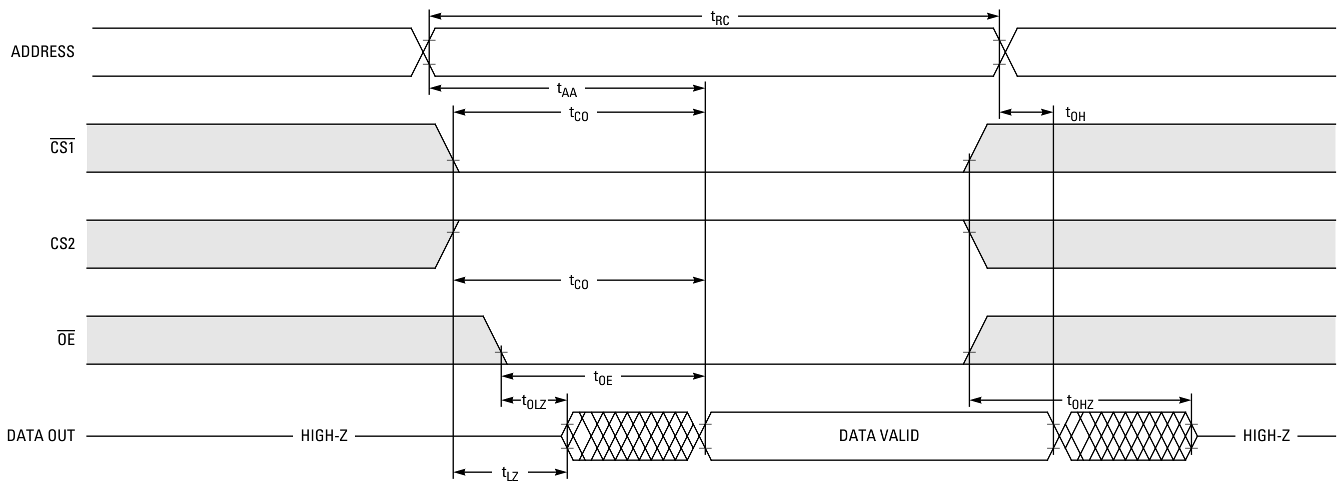


Figure 3. Data Retention Timing Diagram



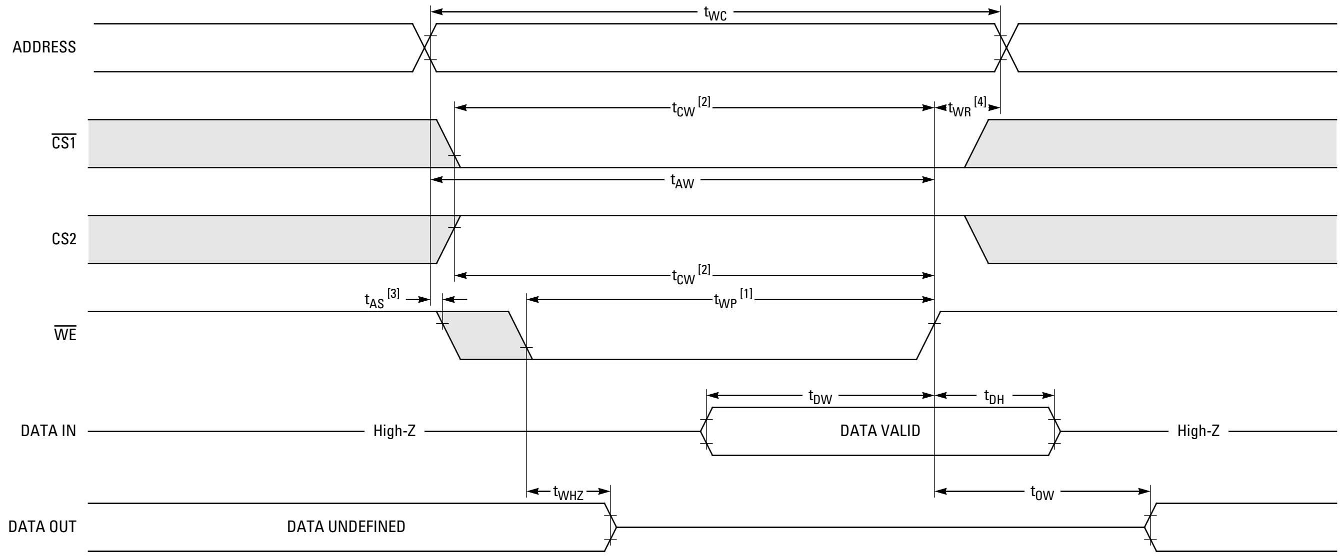
NOTE:
1. t_{HZ} and t_{OHZ} are defined as the time at which the output achieves the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, t_{HZ} (Max) is less than t_{LZ} (Min) both for a given device and device to device interconnection.

Figure 4. Read Cycle Timing (Address Controlled, $\overline{CS1}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = CS2 = V_{IH})



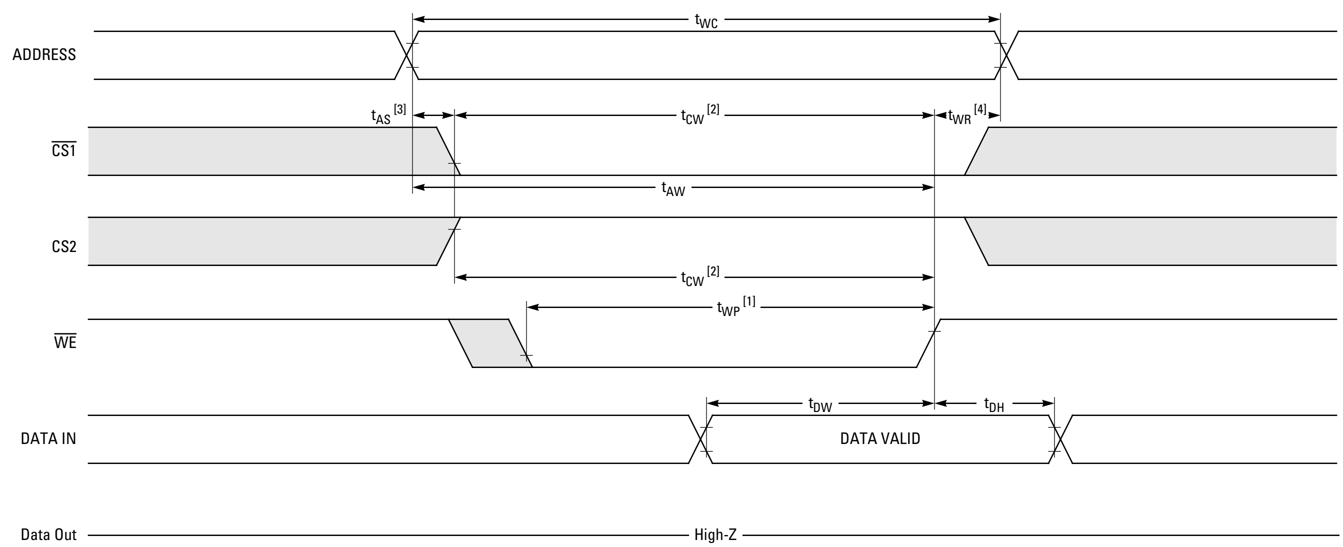
NOTE:
1. t_{HZ} and t_{OHZ} are defined as the time at which the output achieves the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, t_{HZ} (Max) is less than t_{LZ} (Min) both for a given device and device to device interconnection.

Figure 5. Read Cycle Timing ($\overline{WE}$ = V_{IH})



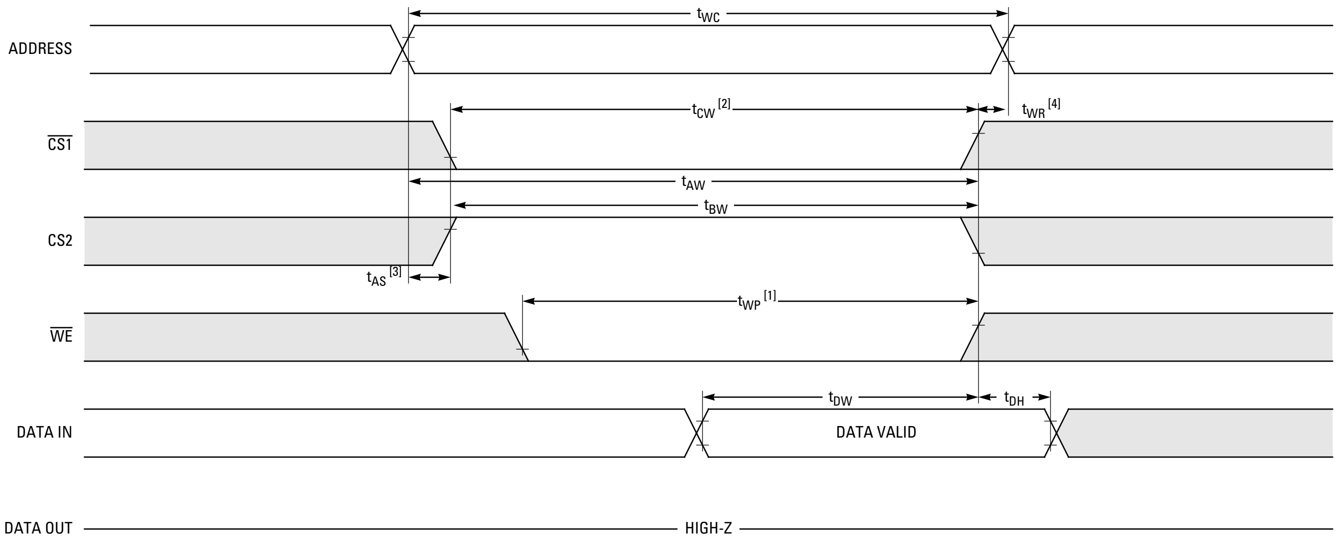
NOTE:
1. A write occurs during the overlap of a low $\overline{CS1}$, A high $\overline{CS2}$ and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS1}$ going and $\overline{WE}$ going low. A write ends at the earliest transition among $\overline{CS1}$ goes high and $\overline{WE}$ going high, t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the later of CS1 going low to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR1} applied encase a write ends at $\overline{CS1}$, or $\overline{WE}$ going high.

Figure 6. Write Cycle Timing ($\overline{WE}$ Controlled)



NOTE:
1. A write occurs during the overlap of a low $\overline{CS1}$, A high $\overline{CS2}$ and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS1}$ going and $\overline{WE}$ going low. A write ends at the earliest transition among $\overline{CS1}$ goes high and $\overline{WE}$ going high, t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the later of CS1 going low to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR1} applied encase a write ends at $\overline{CS1}$, or $\overline{WE}$ going high.

Figure 7. Write Cycle Timing ($\overline{CS1}$ Controlled)



NOTE:
1. A write occurs during the overlap of a low $\overline{CS1}$, A high $\overline{CS2}$ and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS1}$ going and $\overline{WE}$ going low. A write ends at the earliest transition among $\overline{CS1}$ goes high and $\overline{WE}$ going high, t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the later of CS1 going low to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR1} applied encase a write ends at $\overline{CS1}$, or $\overline{WE}$ going high.

Figure 8. Write Cycle Timing (CS2 Controlled)

PACKAGING INFORMATION

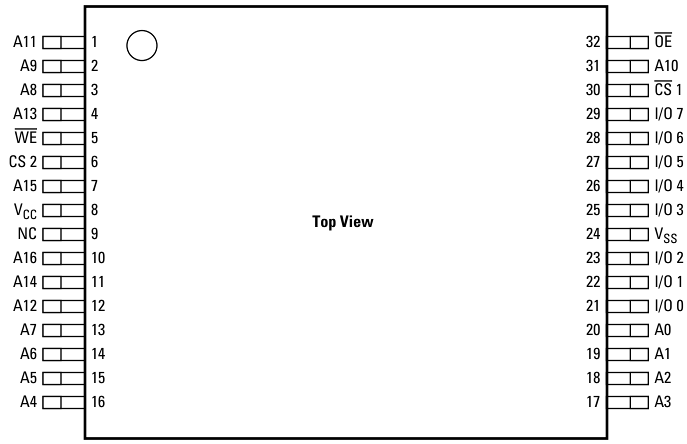
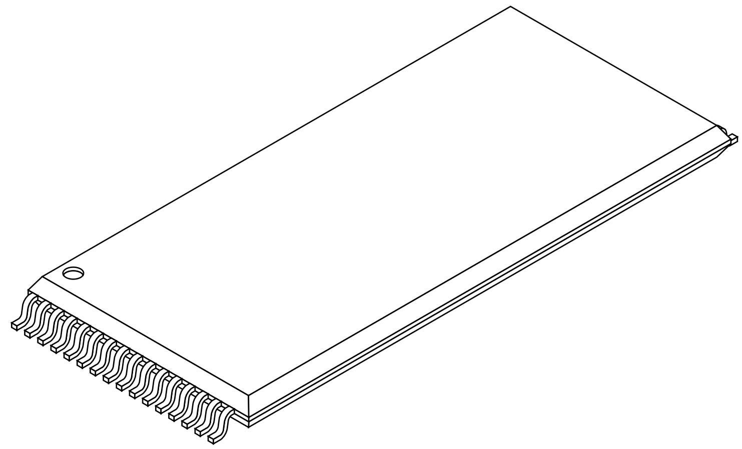
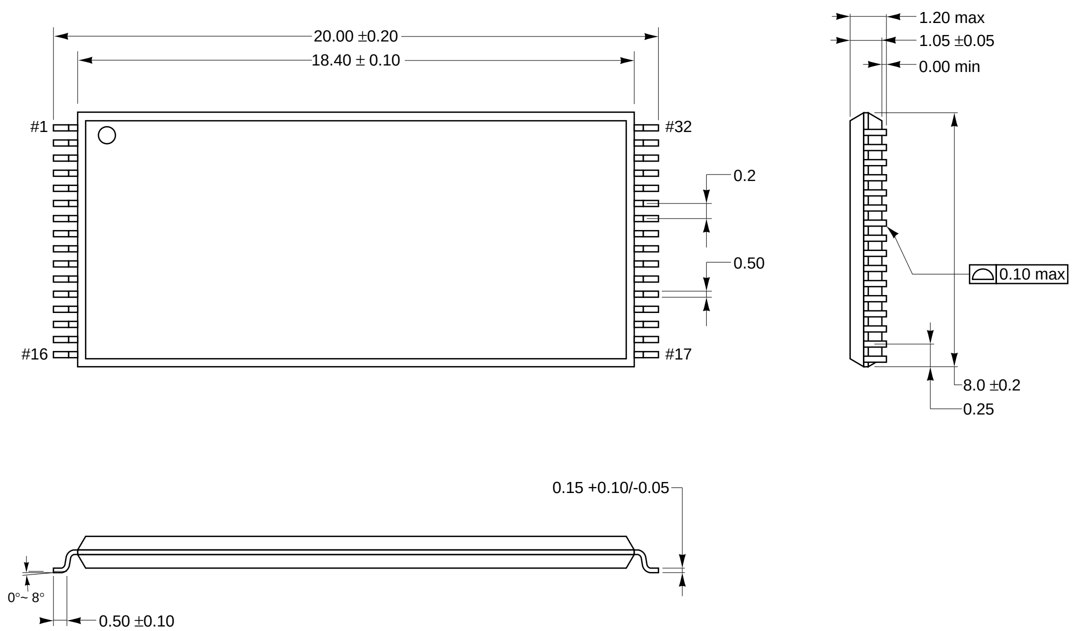


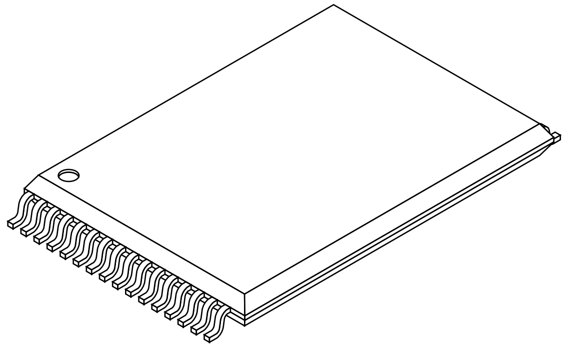
Figure 9. 32-Pin TSOP and sTSOP I Pin Assignment





Dimensions in millimeters

Figure 10. 32-Pin TSOP (Type I) 8 x20 Forward Package Dimensions



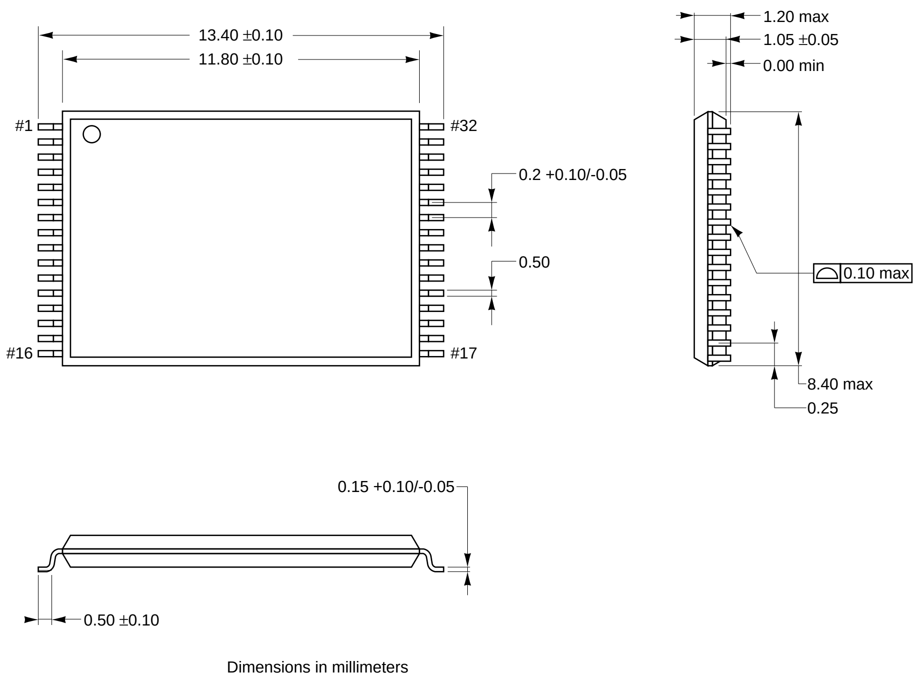


Figure 11. 32-Pin sTSOP (Type I) 8 x13.4 Forward Package Dimensions

GLT6100L08/M08/N08

ORDERING INFO

GLT6100x08LL

Part Number	Standby Current	Cycle Time	V_{CC} Range	Temperature	Orientation	Package
GLT6100L08LL-70TS	5 µA	70 ns	2.7 ~ 3.6	Commercial	Forward	32-Pin TSOP I (330mil)
GLT6100L/M08LL-85TS	5 µA	85 ns	2.3 ~ 2.7, 2.7 ~ 3.6	Commercial	Forward	32-Pin TSOP I (330mil)
GLT6100L08LL-70ST	5 µA	70 ns	2.7 ~ 3.6	Commercial	Forward	32-Pin s-TSOP I (330mil)
GLT6100L/M08LL-85ST	5 µA	85 ns	2.3 ~ 2.7, 2.7 ~ 3.6	Commercial	Forward	32-Pin s-TSOP I (330mil)
GLT6100L/M08LL-100TS	5 µA	100 ns	2.3 ~ 2.7, 2.7 ~ 3.6	Commercial	Forward	32-Pin TSOP I (330mil)
GLT6100M/N08LL-120TS	5 µA	120 ns	1.8 ~ 2.3, 2.3 ~ 2.7	Commercial	Forward	32-Pin TSOP I (330mil)
GLT6100L/M08LL-100ST	5 µA	100 ns	2.3 ~ 2.7, 2.7 ~ 3.6	Commercial	Forward	32-Pin TSOP I (330mil)
GLT6100M/N08LL-120ST	5 µA	120 ns	1.8 ~ 2.3, 2.3 ~ 2.7	Commercial	Forward	32-Pin s-TSOP I (330mil)
GLT6100N08LL-150TS	5 µA	150 ns	1.8 ~ 2.3	Commercial	Forward	32-Pin s-TSOP I (330mil)
GLT6100N08LL-150ST	5 µA	150 ns	1.8 ~ 2.3	Commercial	Forward	32-Pin s-TSOP I (330mil)
GLT6100N08LL-300TS	5 µA	300 ns	1.8 ~ 2.3	Commercial	Forward	32-Pin TSOP I (330mil)
GLT6100N08LL-300ST	5 µA	300 ns	1.8 ~ 2.3	Commercial	Forward	32-Pin s-TSOP I (330mil)

GLT6100x08LLI

Part Number	Standby Current	Cycle Time	VCC Range	Temperature	Orientation	Package
GLT6100L080LLI-70TS	5 µA	70 ns	2.7 ~ 3.6	Industrial	Forward	32-Pin TSOP I (330mil)
GLT6100L/M080LLI-85TS	5 µA	85 ns	2.3 ~ 2.7, 2.7 ~ 3.6	Industrial	Forward	32-Pin TSOP I (330mil)
GLT6100L080LLI-70ST	5 µA	70 ns	2.7 ~ 3.6	Industrial	Forward	32-Pin s-TSOP I (330mil)
GLT6100L/M080LLI-85ST	5 µA	85 ns	2.3 ~ 2.7, 2.7 ~ 3.6	Industrial	Forward	32-Pin s-TSOP I (330mil)
GLT6100L/M08LLI-100TS	5 µA	100 ns	2.3 ~ 2.7, 2.7 ~ 3.6	Industrial	Forward	32-Pin TSOP I (330mil)
GLT6100M/N08LLI-120TS	5 µA	120 ns	1.8 ~ 2.3, 2.3 ~ 2.7	Industrial	Forward	32-Pin TSOP I (330mil)
GLT6100L/M08LLI-100ST	5 µA	100 ns	2.3 ~ 2.7, 2.7 ~ 3.6	Industrial	Forward	32-Pin TSOP I (330mil)
GLT6100M/N08LLI-120ST	5 µA	120 ns	1.8 ~ 2.3, 2.3 ~ 2.7	Industrial	Forward	32-Pin s-TSOP I (330mil)
GLT6100N08LLI-150TS	5 µA	150 ns	1.8 ~ 2.3	Industrial	Forward	32-Pin s-TSOP I (330mil)
GLT6100N08LLI-150ST	5 µA	150 ns	1.8 ~ 2.3	Industrial	Forward	32-Pin s-TSOP I (330mil)
GLT6100N08LLI-300TS	5 µA	300 ns	1.8 ~ 2.3	Industrial	Forward	32-Pin TSOP I (330mil)
GLT6100N08LLI-300ST	5 µA	300 ns	1.8 ~ 2.3	Industrial	Forward	32-Pin s-TSOP I (330mil)

GLT6100x08SL

Part Number	Standby Current	Cycle Time	V_{CC} Range	Temperature	Orientation	Package
GLT6100L08SL-70TS	1 µA	70 ns	2.7 ~ 3.6	Commercial	Forward	32-Pin TSOP I (330mil)
GLT6100L/M08SL-85TS	1 µA	85 ns	2.3 ~ 2.7, 2.7 ~ 3.6	Commercial	Forward	32-Pin TSOP I (330mil)
GLT6100L08SL-70ST	1 µA	70 ns	2.7 ~ 3.6	Commercial	Forward	32-Pin s-TSOP I (330mil)
GLT6100L/M08SL-85ST	1 µA	85 ns	2.3 ~ 2.7, 2.7 ~ 3.6	Commercial	Forward	32-Pin s-TSOP I (330mil)
GLT6100L/M08SL-100TS	1 µA	100 ns	2.3 ~ 2.7, 2.7 ~ 3.6	Commercial	Forward	32-Pin TSOP I (330mil)
GLT6100M/N08SL-120TS	1 µA	120 ns	1.8 ~ 2.3, 2.3 ~ 2.7	Commercial	Forward	32-Pin TSOP I (330mil)
GLT6100L/M08SL-100ST	1 µA	100 ns	2.3 ~ 2.7, 2.7 ~ 3.6	Commercial	Forward	32-Pin TSOP I (330mil)
GLT6100M/N08SL-120ST	1 µA	120 ns	1.8 ~ 2.3, 2.3 ~ 2.7	Commercial	Forward	32-Pin s-TSOP I (330mil)
GLT6100N08SL-150TS	1 µA	150 ns	1.8 ~ 2.3	Commercial	Forward	32-Pin s-TSOP I (330mil)
GLT6100N08SL-150ST	1 µA	150 ns	1.8 ~ 2.3	Commercial	Forward	32-Pin s-TSOP I (330mil)
GLT6100N08SL-300TS	1 µA	300 ns	1.8 ~ 2.3	Commercial	Forward	32-Pin TSOP I (330mil)
GLT6100N08SL-300ST	1 µA	300 ns	1.8 ~ 2.3	Commercial	Forward	32-Pin s-TSOP I (330mil)

GLT6100x08SLI

Part Number	Standby Current	Cycle Time	VCC Range	Temperature	Orientation	Package
GLT6100L080SLI-70TS	1 µA	70 ns	2.7 ~ 3.6	Industrial	Forward	32-Pin TSOP I (330mil)
GLT6100L/M080SLI-85TS	1 µA	85 ns	2.3 ~ 2.7, 2.7 ~ 3.6	Industrial	Forward	32-Pin TSOP I (330mil)
GLT6100L080SLI-70ST	1 µA	70 ns	2.7 ~ 3.6	Industrial	Forward	32-Pin s-TSOP I (330mil)
GLT6100L/M080SLI-85ST	1 µA	85 ns	2.3 ~ 2.7, 2.7 ~ 3.6	Industrial	Forward	32-Pin s-TSOP I (330mil)
GLT6100L/M08SLI-100TS	1 µA	100 ns	2.3 ~ 2.7, 2.7 ~ 3.6	Industrial	Forward	32-Pin TSOP I (330mil)
GLT6100M/N08SLI-120TS	1 µA	120 ns	1.8 ~ 2.3, 2.3 ~ 2.7	Industrial	Forward	32-Pin TSOP I (330mil)
GLT6100L/M08SLI-100ST	1 µA	100 ns	2.3 ~ 2.7, 2.7 ~ 3.6	Industrial	Forward	32-Pin TSOP I (330mil)
GLT6100M/N08SLI-120ST	1 µA	120 ns	1.8 ~ 2.3, 2.3 ~ 2.7	Industrial	Forward	32-Pin s-TSOP I (330mil)
GLT6100N08SLI-150TS	1 µA	150 ns	1.8 ~ 2.3	Industrial	Forward	32-Pin s-TSOP I (330mil)
GLT6100N08SLI-150ST	1 µA	150 ns	1.8 ~ 2.3	Industrial	Forward	32-Pin s-TSOP I (330mil)
GLT6100N08SLI-300TS	1 µA	300 ns	1.8 ~ 2.3	Industrial	Forward	32-Pin TSOP I (330mil)
GLT6100N08SLI-300ST	1 µA	300 ns	1.8 ~ 2.3	Industrial	Forward	32-Pin s-TSOP I (330mil)

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