FAIRCHILD SEMICONDUCTOR™

January 1998

74VHC373 • 74VHCT373
Octal D-Type Latch with 3-STATE Outputs

General Description

The VHC/VHCT373 is an advanced high speed CMOS octal D-type latch with 3-STATE output fabricated with silicon gate CMOS technology. It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation. This 8-bit D-type latch is controlled by a latch enable input (LE) and an output enable input ($\overline{OE}$). The latches appear transparent to data when latch enable (LE) is HIGH. When LE is low, the data that meets the setup time is latched. When the $\overline{OE}$ input is high, the eight outputs are in a high impedance state.

An input protection circuit ensures that 0V–7V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

Features

- High Speed:
  VHC t_{pd} = 5.0 ns (typ) @ V_{CC} = 5V
  VHCT t_{pd} = 5.1 ns (typ) @ V_{CC} = 5V
- High Noise Immunity:
  VHC $V_{NIH} = V_{NIL}$ = 28% V_{CC} (Min)
  VHCT V_{IH} = 2.0V, V_{IL} = 0.8V
- Power Down Protection:
  VHC Inputs Only
  VHCT Inputs and Outputs
- Low Noise:
  VHC V_{OLP} = 0.6V (typ)
  VHCT V_{OLP} = 0.8V (typ)
- Low Power Dissipation:
  I_{CC} = 4 µA (Max) @ T_a = 25˚C
- Pin and Function Compatible with 74HC/HCT373

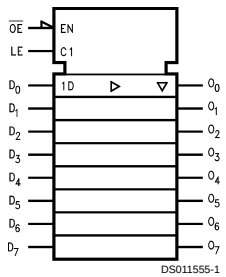
Ordering Code:

Commercial	Package Number	Package Description
74VHC373M	M20B	20-Lead Molded JEDEC SOIC
74VHC373SJ	M20D	20-Lead Molded EIAJ SOIC
74VHC373MTC	MTC20	20-Lead Molded JEDEC Type 1 TSSOP
74VHC373N	N20A	20-Lead Molded DIP
74VHCT373M	M20B	20-Lead Molded JEDEC SOIC
74VHCT373SJ	M20D	20-Lead Molded EIAJ SOIC
74VHCT373MTC	MTC20	20-Lead Molded JEDEC Type 1 TSSOP
74VHCT373N	N20A	20-Lead Molded DIP

Surface mount packages are also available on Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbol

IEEE/IEC



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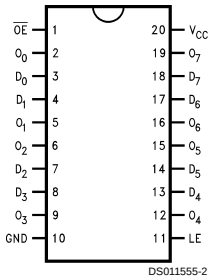
Connection Diagram

Pin Assignment for DIP,TSSOP and SOIC



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Pin Descriptions

Pin Names	Description
D_0–D_7	Data Inputs
LE	Latch Enable Input
$\overline{OE}$	Output Enable Input
O_0–O_7	3-STATE Outputs

Truth Table

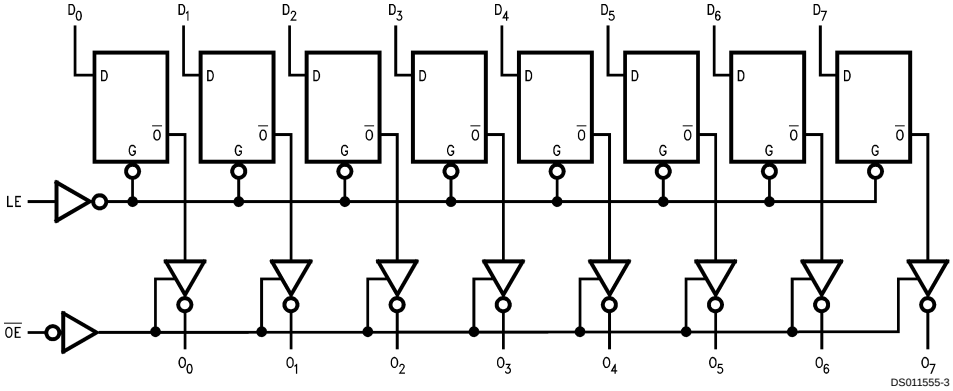
Inputs			Outputs
LE	$\overline{OE}$	D_n	O_n
X	H	X	Z
H	L	L	L
H	L	H	H
L	L	X	O_0

H = HIGH Voltage Level
L = LOW Voltage Level
Z = High Impedance
X = Immaterial
O_0 = Previous O_0 before HIGH to Low transition of Latch Enable

Functional Description

The VHC/VHCT373 contains eight D-type latches with 3-STATE standard outputs. When the Latch Enable (LE) input is HIGH, data on the D_n inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW, the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The 3-STATE standard outputs are controlled by the Output Enable ($\overline{OE}$) input. When $\overline{OE}$ is LOW, the standard outputs are in the 2-state mode. When $\overline{OE}$ is HIGH, the standard outputs are in the high impedance mode but this does not interfere with entering new data into the latches.

Logic Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

Supply Voltage (V_{CC})	−0.5V to + 7.0V
DC Input Voltage (V_{IN})	−0.5V to + 7.0V
DC Output Voltage (V_{OUT})	
VHC	−0.5V to V_{CC} + 0.5V
VHCT (Note 2)	−0.5V to +7.0V
Input Diode Current (I_{IK})	−20 mA
Output Diode Current (VHC)	±20 mA
(VHCT)	−20 mA
DC Output Current (I_{OUT})	±25 mA
DC V_{CC}/GND Current (I_{CC})	±75 mA
Storage Temperature (T_{STG})	−65˚C to +150˚C
Lead Temperature (T_L)	
(Soldering, 10 sec)	260˚C

Recommended Operating Conditions (Note 3)

Supply Voltage (V_{CC})	
VHC	2.0V to + 5.5V
VHCT	4.5V to + 5.5V
Input Voltage (V_{IN})	0V to + 5.5V
Output Voltage (V_{OUT})	0V to V_{CC}
Operating Temperature (T_{OPR})	
VHC/VHCT	−40˚C to +85˚C
Input Rise and Fall Time (t_r, t_f)	
V_{CC} = 3.3V ±0.3V (VHC only)	0 ~ 100 ns/V
V_{CC} = 5.0 ±0.5V	0 ~ 20 ns/V

Note 1: Absolute Maximum Ratings are values beyond which the device may be damaged or have its useful life impaired. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation outside databook specifications.

Note 2: $V_{OUT} > V_{CC}$ only if output is in H or Z state.

Note 3: Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics for VHC

Symbol	Parameter	V_{CC} (V)	T_A = +25˚C			T_A = −40˚C to +85˚C		Units	Conditions	
			Min	Typ	Max	Min	Max			
V_{IH}	High Level Input Voltage	2.0	1.50			1.50		V		
		3.0−5.5	0.7 V_{CC}			0.7 V_{CC}				
V_{IL}	Low Level Input Voltage	2.0			0.50		0.50	V		
		3.0−5.5			0.3 V_{CC}		0.3 V_{CC}			
V_{OH}	High Level Output Voltage	2.0	1.9	2.0		1.9		V	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −50 µA
		3.0	2.9	3.0		2.9				
		4.5	4.4	4.5		4.4				
		3.0	2.58			2.48		V		I_{OH} = −4 mA
		4.5	3.94			3.80				I_{OH} = −8 mA
V_{OL}	Low Level Output Voltage	2.0		0.0	0.1		0.1	V	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50 µA
		3.0		0.0	0.1		0.1			
		4.5		0.0	0.1		0.1			
		3.0			0.36		0.44	V		I_{OL} = 4 mA
		4.5			0.36		0.44			I_{OL} = 8 mA
I_{OZ}	3-STATE Output Off-State Current	5.5			±0.25		±2.5	µA	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND	
I_{IN}	Input Leakage Current	0−5.5			±0.1		±1.0	µA	V_{IN} = 5.5 or GND	
I_{CC}	Quiescent Supply Current	5.5			4.0		40.0	µA	V_{IN} = V_{CC} or GND	

Noise Characteristics for VHC

Symbol	Parameter	V_{CC} (V)	T_A = +25˚C		Units	Conditions
			Typ	Limits		
V_{OLP} (Note 4)	Quiet Output Maximum Dynamic V_{OL}	5.0	0.6	0.9	V	C_L = 50 pF
V_{OLV} (Note 4)	Quiet Output Minimum Dynamic V_{OL}	5.0	−0.6	−0.9	V	C_L = 50 pF
V_{IHD} (Note 4)	Minimum High Level Dynamic Input Voltage	5.0		3.5	V	C_L = 50 pF
V_{ILD} (Note 4)	Maximum Low Level Dynamic Input Voltage	5.0		1.5	V	C_L = 50 pF

Note 4: Parameter guaranteed by design.

DC Electrical Characteristics for VHCT

Symbol	Parameter	V_{CC} (V)	T_A = +25°C			T_A = −40°C to +85°C		Units	Conditions	
			Min	Typ	Max	Min	Max			
V_{IH}	High Level Input Voltage	4.5	2.0			2.0		V		
		5.5	2.0			2.0				
V_{IL}	Low Level Input Voltage	4.5			0.8		0.8	V		
		5.5			0.8		0.8			
V_{OH}	High Level Output Voltage	4.5	3.15	3.65		3.15		V	V_{IN} = V_{IH}	I_{OH} = −50 μA
		4.5	2.5			2.4		V	or V_{IL}	I_{OH} = −8 mA
V_{OL}	Low Level Output Voltage	4.5		0.0	0.1		0.1	V	V_{IN} = V_{IH}	I_{OL} = 50 μA
		4.5			0.36		0.44	V	or V_{IL}	I_{OL} = 8 mA
I_{OZ}	3-STATE Output Off-State Current	5.5			±0.25		±2.5	μA	V_{IN} = V_{IH} or V_{IL}	
									V_{OUT} = V_{CC} or GND	
I_{IN}	Input Leakage Current	0–5.5			±0.1		±1.0	μA	V_{IN} = 5.5V or GND	
I_{CC}	Quiescent Supply Current	5.5			4.0		40.0	μA	V_{IN} = V_{CC} or GND	
I_{CCT}	Maximum I_{CC}/Input	5.5			1.35		1.50	mA	V_{IN} = 3.4V	
									Other Inputs = V_{CC} or GND	
I_{OFF}	Output Leakage Current (Power Down State)	0.0			+0.5		+0.5	μA	V_{OUT} = 5.5V	

Noise Characteristics for VHCT

Symbol	Parameter	V_{CC} (V)	T_A = +25°C		Units	Conditions
			Typ	Limits		
V_{OLP} (Note 5)	Quiet Output Maximum Dynamic V_{OL}	5.0	0.8	1.2	V	C_L = 50 pF
V_{OLV} (Note 5)	Quiet Output Minimum Dynamic V_{OL}	5.0	−0.8	−1.2	V	C_L = 50 pF
V_{IHD} (Note 5)	Minimum High Level Dynamic Input Voltage	5.0		2.0	V	C_L = 50 pF
V_{ILD} (Note 5)	Maximum Low Level Dynamic Input Voltage	5.0		0.8	V	C_L = 50 pF

Note 5: Parameter guaranteed by design.

AC Electrical Characteristics for VHC

Symbol	Parameter	V_{CC} (V)	T_A = +25°C			T_A = −40°C to +85°C		Units	Conditions	
			Min	Typ	Max	Min	Max			
t_{PLH}	Propagation Delay Time (LE to O_n)	3.3 ± 0.3		7.0	11.0	1.0	13.0	ns		C_L = 15 pF
t_{PHL}				9.5	14.5	1.0	16.5			C_L = 50 pF
		5.0 ± 0.5		4.9	7.2	1.0	8.5	ns		C_L = 15 pF
				6.4	9.2	1.0	10.5			C_L = 50 pF
t_{PLH}	Propagation Delay Time (D to O_n)	3.3 ± 0.3		7.3	11.4	1.0	13.5	ns		C_L = 15 pF
t_{PHL}				9.8	14.9	1.0	17.0			C_L = 50 pF
		5.0 ± 0.5		5.0	7.2	1.0	8.5			C_L = 15 pF
				6.5	9.2	1.0	10.5			C_L = 50 pF
t_{PZL}	3-STATE	3.3 ± 0.3		7.3	11.4	1.0	13.5	ns	R_L = 1 kΩ	C_L = 15 pF
t_{PZH}	Output			9.8	14.9	1.0	17.0			C_L = 50 pF
	Enable Time	5.0 ± 0.5		5.5	8.1	1.0	9.5	ns		C_L = 15 pF
				7.0	10.1	1.0	11.5			C_L = 50 pF
t_{PLZ}	3-STATE Output Disable Time	3.3 ± 0.3		9.5	13.2	1.0	15.0	ns	R_L = 1 kΩ	C_L = 50 pF
t_{PHZ}		5.0 ± 0.5		6.5	9.2	1.0	10.5			C_L = 50 pF
t_{OSLH}	Output to Output Skew	3.3 ± 0.3			1.5		1.5	ns	(Note 6)	C_L = 50 pF
t_{OSHL}		5.0 ± 0.5			1.0		1.0			C_L = 50 pF
C_{IN}	Input Capacitance			4	10		10	pF	V_{CC} = Open	
C_{OUT}	Output Capacitance			6				pF	V_{CC} = 5.0V	
C_{PD}	Power Dissipation Capacitance			27				pF	(Note 7)	

Note 6: Parameter guaranteed by design. $t_{OSLH} = |t_{PLH\ max} - t_{PLH\ min}|$; $t_{OSHL} = |t_{PHL\ max} - t_{PHL}\ min|$

Note 7: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC} (opr.) = $C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8$ (per Latch). The total C_{PD} when n pcs. of the Latch operates can be calculated by the equation: C_{PD}(total) = 14 + 13n.

AC Operating Requirements for VHC

Symbol	Parameter	V_{CC} (V)	T_A = +25°C			T_A = −40°C to +85°C		Units
			Min	Typ	Max	Min	Max	
$t_{W(H)}$	Minimum Pulse Width (LE)	3.3 ± 0.3	5.0			5.0		ns
		5.0 ± 0.5	5.0			5.0		
t_S	Minimum Set-Up Time	3.3 ± 0.3	4.0			4.0		ns
		5.0 ± 0.5	4.0			4.0		
t_H	Minimum Hold Time	3.3 ± 0.3	1.0			1.0		ns
		5.0 ± 0.5	1.0			1.0		

AC Electrical Characteristics for VHCT

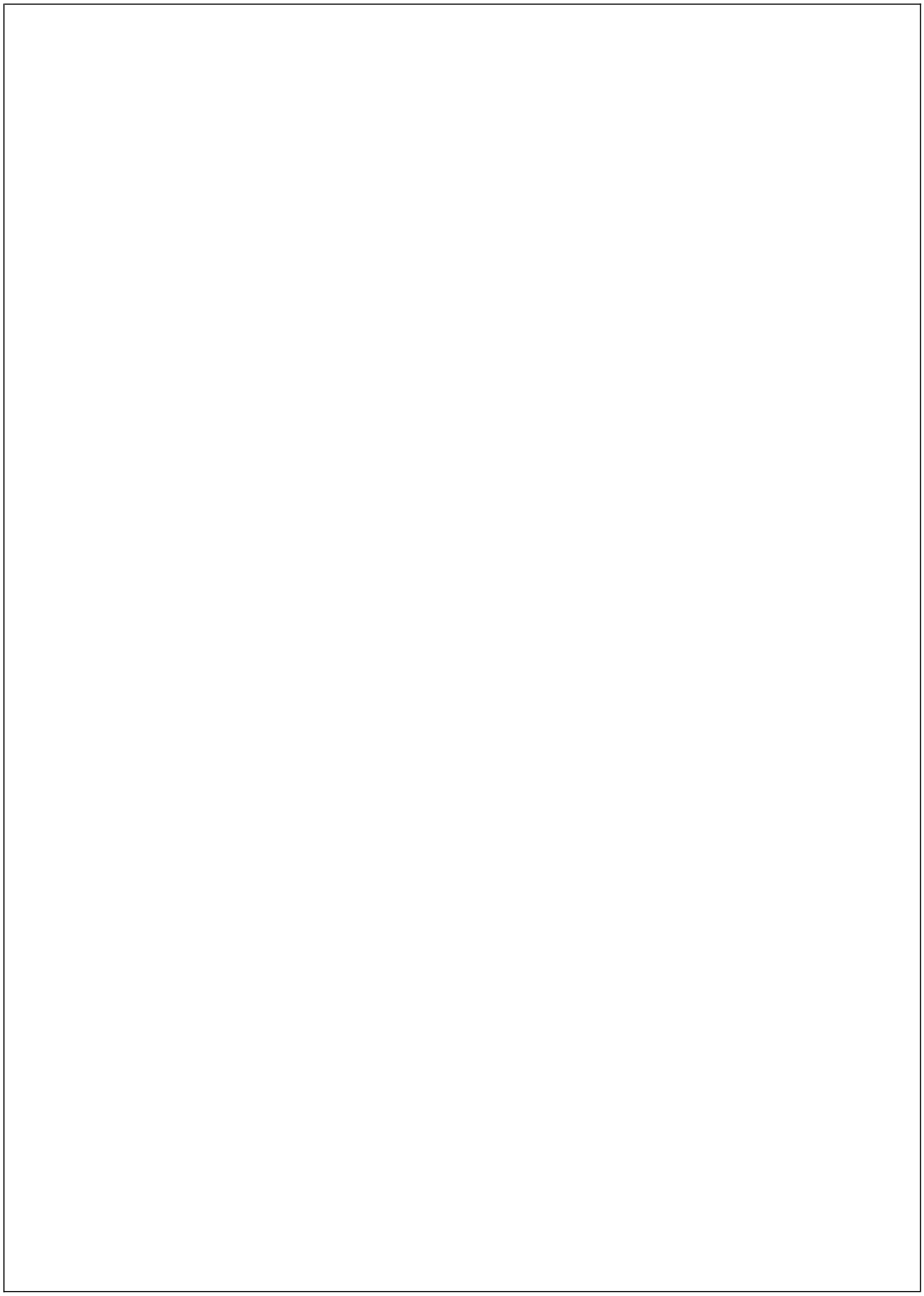
Symbol	Parameter	V_{CC} (V)	T_A = +25°C			T_A = −40°C to +85°C		Units	Conditions	
			Min	Typ	Max	Min	Max			
t_{PLH}	Propagation Delay Time (LE to O_n)	5.0 ± 0.5		7.7	12.3	1.0	13.5	ns		C_L = 15 pF
t_{PHL}				8.5	13.3	1.0	14.5			C_L = 50 pF
t_{PLH}	Propagation Delay Time (D to O_n)	5.0 ± 0.5		5.1	8.5	1.0	9.5	ns		C_L = 15 pF
t_{PHL}				5.9	9.5	1.0	10.5			C_L = 50 pF
t_{PZL}	3-STATE Output Enable Time	5.0 ± 0.5		6.3	10.9	1.0	12.5	ns	R_L = 1 kΩ	C_L = 15 pF
t_{PZH}				7.1	11.9	1.0	13.5			C_L = 50 pF
t_{PLZ}	3-STATE Output Disable Time	5.0 ± 0.5		6.8	11.2	1.0	12.0	ns	R_L = 1 kΩ	C_L = 50 pF
t_{PHZ}										
t_{OSLH}	Output to Output Skew	5.0 ± 0.5			1.0		1.0		(Note 9)	
t_{OSHL}										
C_{IN}	Input Capacitance			4	10		10	pF	V_{CC} = Open	
C_{OUT}	Output Capacitance			9				pF	V_{CC} = 5.0V	
C_{PD}	Power Dissipation Capacitance			27				pF	(Note 9)	

Note 8: Parameter guaranteed by design. $t_{OSLH} = |t_{PLH\ max} - t_{PLH\ min}|$; $t_{OSHL} = |t_{PHL\ max} - t_{PHL\ min}|$

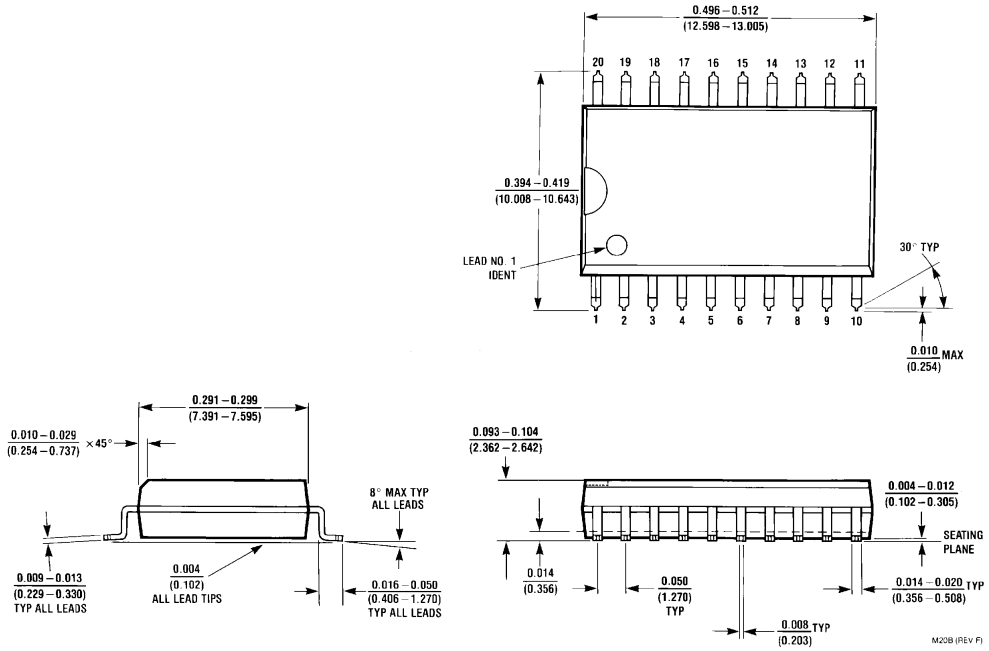
Note 9: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC} (opr.) = $C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8$ (per F/F).

AC Operating Requirements for VHCT

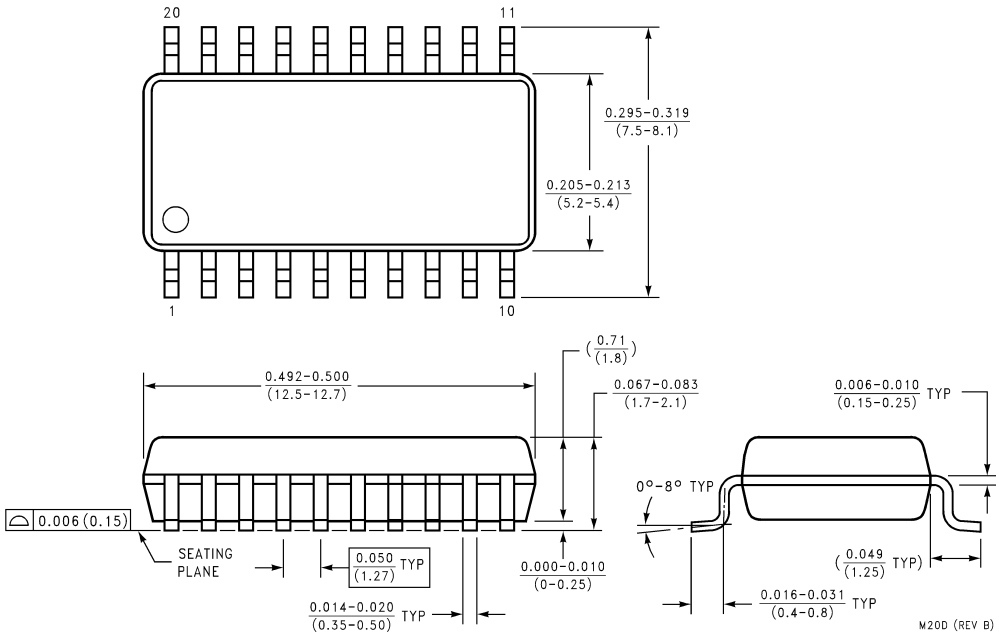
Symbol	Parameter	V_{CC} (V)	T_A = +25°C			T_A = −40°C to +85°C		Units
			Min	Typ	Max	Min	Max	
$t_{W(H)}$	Minimum Pulse Width (LE)	5.0 ± 0.5	6.5			6.5		ns
t_S	Minimum Set-Up Time	5.0 ± 0.5	1.5			1.5		ns
t_H	Minimum Hold Time	5.0 ± 0.5	3.5			3.5		ns



Physical Dimensions inches (millimeters) unless otherwise noted

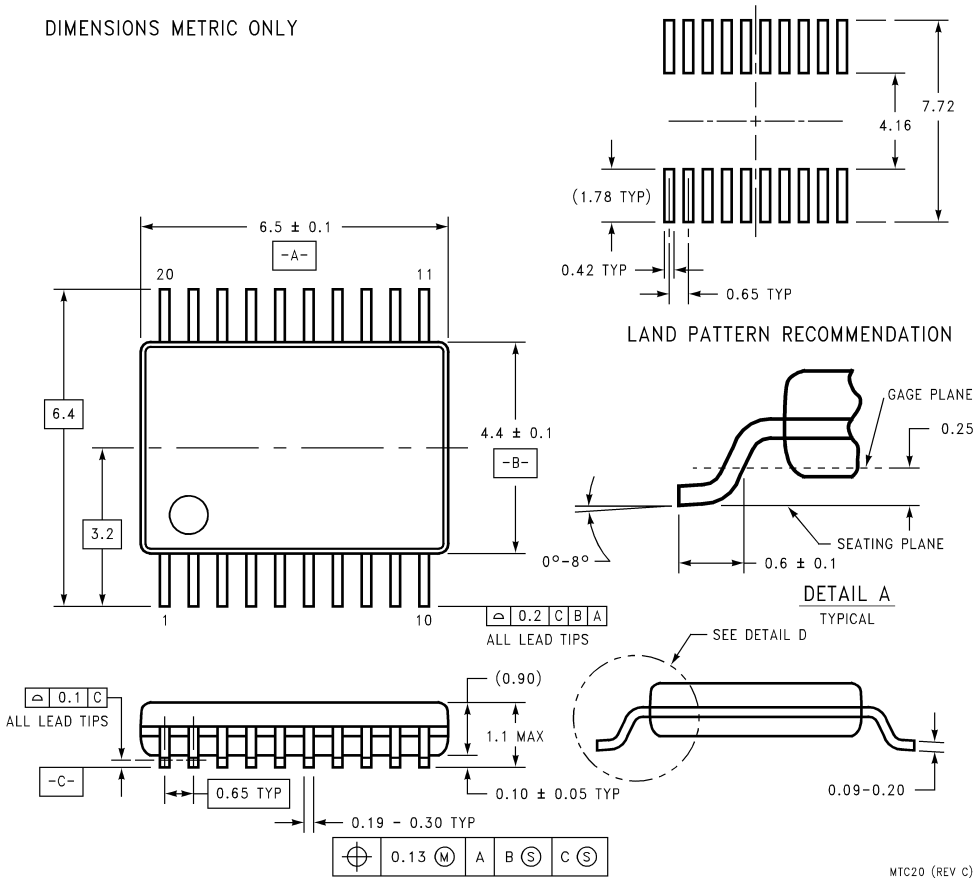


20-Lead Small Outline Integrated Circuit—JEDEC SOIC (M)
Package Number M20B



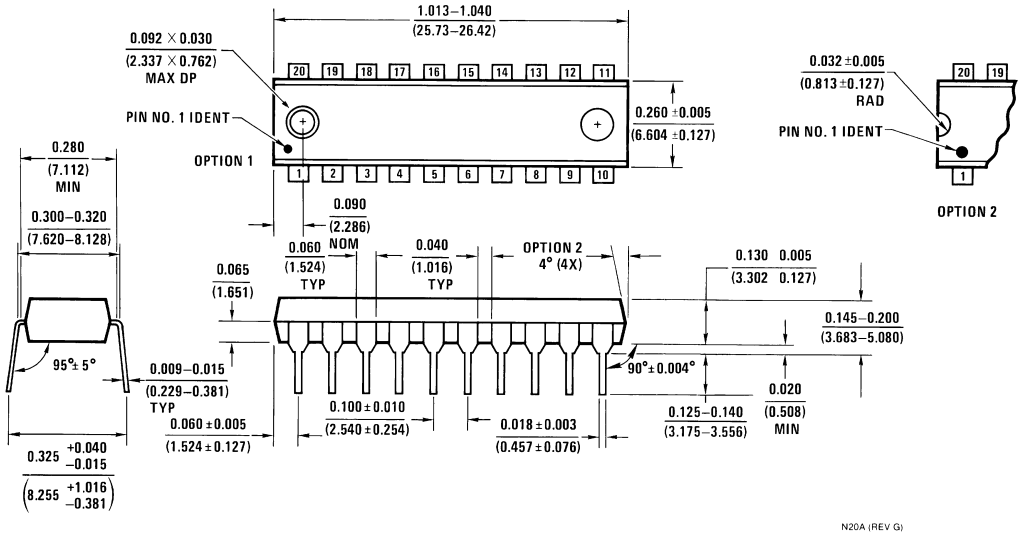
20-Lead Plastic EIAJ SOIC (SJ)
Package Number M20D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



20-Lead Plastic JEDEC TSSOP Type I (MTC)
Package Number MTC20

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



20-Lead (0.300" Wide) Molded Dual-in-Line Package
Package Number N20A

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