



3.3V CMOS 18-BIT UNIVERSAL BUS TRANS- CEIVER WITH 3-STATE OUTPUTS AND BUS-HOLD

IDT74ALVCH16501

FEATURES:

- 0.5 MICRON CMOS Technology
- Typical $t_{SK(0)}$ (Output Skew) < 250ps
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- 0.635mm pitch SSOP, 0.50mm pitch TSSOP, and 0.40mm pitch TVSOP packages
- Extended commercial range of - 40°C to + 85°C
- $V_{CC} = 3.3V \pm 0.3V$, Normal Range
- $V_{CC} = 2.7V$ to $3.6V$, Extended Range
- $V_{CC} = 2.5V \pm 0.2V$
- CMOS power levels (0.4μW typ. static)
- Rail-to-Rail output swing for increased noise margin

Drive Features for ALVCH16501:

- High Output Drivers: ±24mA
- Suitable for heavy loads

APPLICATIONS:

- 3.3V High Speed Systems
- 3.3V and lower voltage computing systems

DESCRIPTION:

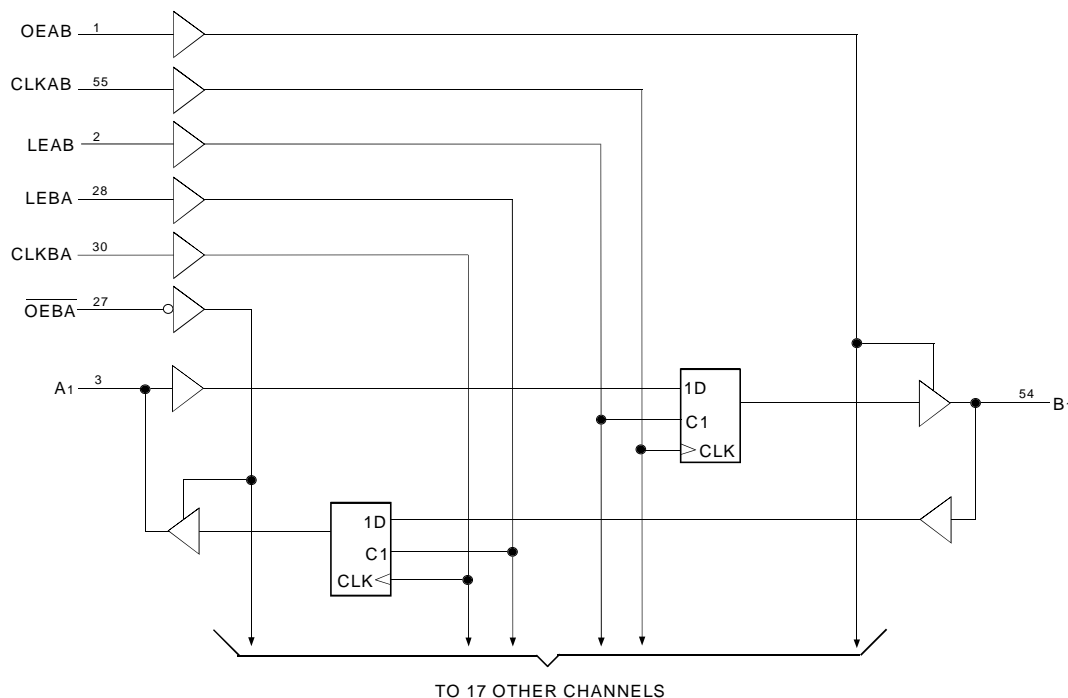
This 18-bit universal bus transceiver is built using advanced dual metal CMOS technology. Data flow in each direction is controlled by output-enable (OEAB and \overline{OEBA}), latch enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if CLKAB is held at a high or low logic level. If LEAB is low, the A data is stored in the latch/flip-flop on the low-to-high transition of CLKAB. When OEAB is high, the outputs are active. When OEAB is low, the outputs are in the high-impedance state.

Data flow for B to A is similar to that of A to B but uses \overline{OEBA} , LEBA, and CLKBA. The output enables are complementary (OEAB is active high and \overline{OEBA} is active low).

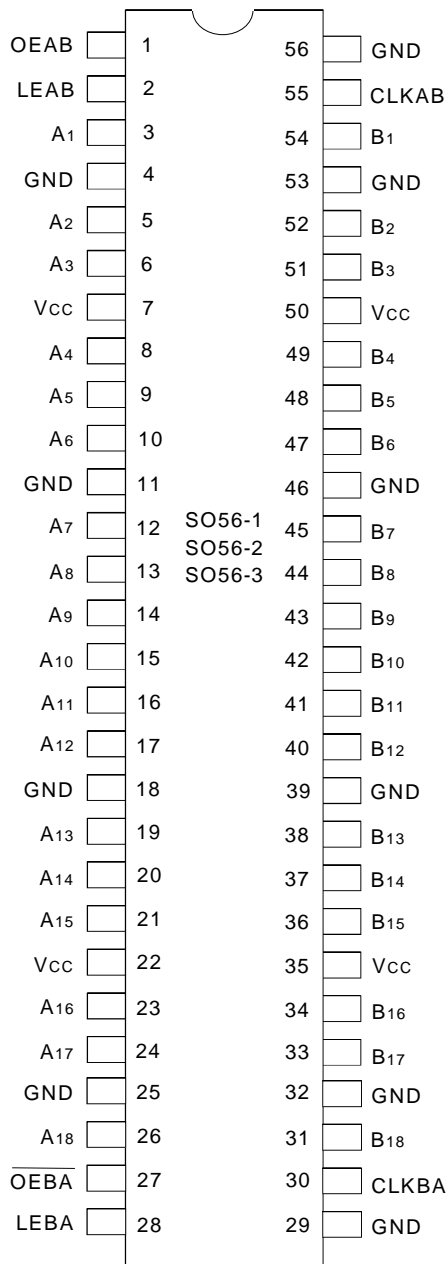
The ALVCH16501 has been designed with a ±24mA output driver. This driver is capable of driving a moderate to heavy load while maintaining speed performance.

The ALVCH16501 has "bus-hold" which retains the inputs' last state whenever the input bus goes to a high impedance. This prevents floating inputs and eliminates the need for pull-up/down resistors.

Functional Block Diagram



PIN CONFIGURATION



SSOP/TSSOP/TVSOP
TOP VIEW

CAPACITANCE ($T_A = +25^\circ\text{C}$, $f = 1.0\text{MHz}$)

| Symbol | Parameter ⁽¹⁾ | Conditions | Typ. | Max. | Unit |
|------------------|--------------------------|-----------------------|------|------|------|
| C _{IN} | Input Capacitance | V _{IN} = 0V | 5 | 7 | pF |
| C _{OUT} | Output Capacitance | V _{OUT} = 0V | 7 | 9 | pF |
| C _{I/O} | I/O Port Capacitance | V _{IN} = 0V | 7 | 9 | pF |

NOTE:

1. As applicable to the device type.

ABSOLUTE MAXIMUM RATING (1)

| Symbol | Description | Max. | Unit |
|----------------------------------|--|--------------------------------|------|
| V _{TERM} ⁽²⁾ | Terminal Voltage with Respect to GND | - 0.5 to + 4.6 | V |
| V _{TERM} ⁽³⁾ | Terminal Voltage with Respect to GND | - 0.5 to V _{CC} + 0.5 | V |
| T _{STG} | Storage Temperature | - 65 to + 150 | °C |
| I _{OUT} | DC Output Current | - 50 to + 50 | mA |
| I _{IK} | Continuous Clamp Current, V _I < 0 or V _I > V _{CC} | ± 50 | mA |
| I _{OK} | Continuous Clamp Current, V _O < 0 | - 50 | mA |
| I _{CC} | Continuous Current through each V _{CC} or GND | ± 100 | mA |

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NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{CC} terminals.
3. All terminals except V_{CC}.

PIN DESCRIPTION

| Pin Names | Description |
|--------------------------|---|
| OEAB | A-to-B Output Enable Input |
| $\overline{\text{OEBA}}$ | B-to-A Output Enable Input (Active LOW) |
| LEAB | A-to-B Latch Enable Input |
| LEBA | B-to-A Latch Enable Input |
| CLKAB | A-to-B Clock Input |
| CLKBA | B-to-A Clock Input |
| A _x | A-to-B Data Inputs or B-to-A 3-State Outputs ⁽¹⁾ |
| B _x | B-to-A Data Inputs or A-to-B 3-State Outputs ⁽¹⁾ |

NOTE:

1. These pins have "Bus-Hold." All other pins are standard inputs, outputs, or I/Os.

FUNCTION TABLE (1, 2)

| Inputs | | | | Output |
|--------|------|--------|----|-------------------|
| OEAB | LEAB | CLKAB | Ax | Bx |
| L | X | X | X | Z |
| H | H | X | L | L |
| H | H | X | H | H |
| H | L | ↑ | L | L |
| H | L | ↑ | H | H |
| H | L | L or H | X | Bo ⁽³⁾ |

NOTES:

1. A-to-B data flow is shown. B-to-A data flow is similar but uses \overline{OEBA} , \overline{LEBA} , and \overline{CLKBA} .
2. H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High-Impedance
↑ = LOW-to-HIGH Transition
3. Output level before the indicated steady-state input conditions were established.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Condition: TA = - 40°C to +85°C

| Symbol | Parameter | Test Conditions | | Min. | Typ. ⁽¹⁾ | Max. | Unit |
|--|--|--|----------------------------------|------|---------------------|-------|------|
| V _{IH} | Input HIGH Voltage Level | V _{CC} = 2.3V to 2.7V | | 1.7 | — | — | V |
| | | V _{CC} = 2.7V to 3.6V | | 2 | — | — | |
| V _{IL} | Input LOW Voltage Level | V _{CC} = 2.3V to 2.7V | | — | — | 0.7 | V |
| | | V _{CC} = 2.7V to 3.6V | | — | — | 0.8 | |
| I _{IH} | Input HIGH Current | V _{CC} = 3.6V | V _I = V _{CC} | — | — | ± 5 | μA |
| I _{IL} | Input LOW Current | V _{CC} = 3.6V | V _I = GND | — | — | ± 5 | |
| I _{OZH} | High Impedance Output Current (3-State Output pins) | V _{CC} = 3.6V | V _O = V _{CC} | — | — | ± 10 | μA |
| I _{OZL} | | | V _O = GND | — | — | ± 10 | μA |
| V _{IK} | Clamp Diode Voltage | V _{CC} = 2.3V, I _{IN} = - 18mA | | — | - 0.7 | - 1.2 | V |
| V _H | Input Hysteresis | V _{CC} = 3.3V | | — | 100 | — | mV |
| I _{CC1} I _{CC2} I _{CC3} | Quiescent Power Supply Current | V _{CC} = 3.6V | | — | 0.1 | 40 | μA |
| | | V _{IN} = GND or V _{CC} | | | | | |
| ΔI _{CC} | Quiescent Power Supply Current Variation | One input at V _{CC} - 0.6V, other inputs at V _{CC} or GND | | — | — | 750 | μA |

NOTE:

1. Typical values are at V_{CC} = 3.3V, +25°C ambient.

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BUS-HOLD CHARACTERISTICS

| Symbol | Parameter ⁽¹⁾ | Test Conditions | | Min. | Typ. ⁽²⁾ | Max. | Unit |
|----------------|----------------------------------|------------------------|----------------------------|------|---------------------|-------|------|
| IBHH IBHL | Bus-Hold Input Sustain Current | V _{CC} = 3.0V | V _I = 2.0V | - 75 | — | — | μA |
| | | | V _I = 0.8V | 75 | — | — | |
| IBHH IBHL | Bus-Hold Input Sustain Current | V _{CC} = 2.3V | V _I = 1.7V | - 45 | — | — | μA |
| | | | V _I = 0.7V | 45 | — | — | |
| IBHHO IBHLO | Bus-Hold Input Overdrive Current | V _{CC} = 3.6V | V _I = 0 to 3.6V | — | — | ± 500 | μA |

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NOTES:

1. Pins with Bus-hold are identified in the pin description.
2. Typical values are at V_{CC} = 3.3V, +25°C ambient.

OUTPUT DRIVE CHARACTERISTICS

| Symbol | Parameter | Test Conditions ⁽¹⁾ | | Min. | Max. | Unit |
|-----------------|---------------------|--------------------------------|---------------------------|--------------------------|------|------|
| V _{OH} | Output HIGH Voltage | V _{CC} = 2.3V to 3.6V | I _{OH} = - 0.1mA | V _{CC} - 0.2 | — | V |
| | | V _{CC} = 2.3V | I _{OH} = - 6mA | 2 | — | |
| | | V _{CC} = 2.3V | I _{OH} = - 12mA | 1.7 | — | |
| | | V _{CC} = 2.7V | | 2.2 | — | |
| | | V _{CC} = 3.0V | | 2.4 | — | |
| | | | V _{CC} = 3.0V | I _{OH} = - 24mA | 2 | |
| V _{OL} | Output LOW Voltage | V _{CC} = 2.3V to 3.6V | I _{OL} = 0.1mA | — | 0.2 | V |
| | | V _{CC} = 2.3V | I _{OL} = 6mA | — | 0.4 | |
| | | | I _{OL} = 12mA | — | 0.7 | |
| | | V _{CC} = 2.7V | I _{OL} = 12mA | — | 0.4 | |
| | | V _{CC} = 3.0V | I _{OL} = 24mA | — | 0.55 | |

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NOTE:

1. V_{IH} and V_{IL} must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate V_{CC} range. T_A = - 40°C to + 85°C.

OPERATING CHARACTERISTICS, $T_A = 25^\circ\text{C}$

| Symbol | Parameter | Test Conditions | $V_{CC} = 2.5V \pm 0.2V$ | $V_{CC} = 3.3V \pm 0.3V$ | Unit |
|--------|---|---|--------------------------|--------------------------|------|
| | | | Typical | Typical | |
| CPD | Power Dissipation Capacitance Outputs enabled | $C_L = 0\text{pF}$, $f = 10\text{MHz}$ | 44 | 54 | pF |
| CPD | Power Dissipation Capacitance Outputs disabled | | 6 | 6 | pF |

SWITCHING CHARACTERISTICS ⁽¹⁾

| Symbol | Parameter | $V_{CC} = 2.5V \pm 0.2V$ | | $V_{CC} = 2.7V$ | | $V_{CC} = 3.3V \pm 0.3V$ | | Unit | |
|------------------------|---|--------------------------|------|-----------------|------|--------------------------|------|------|----|
| | | Min. | Max. | Min. | Max. | Min. | Max. | | |
| f_{MAX} | | 150 | — | 150 | — | 150 | — | MHz | |
| t_{PLH} t_{PHL} | Propagation Delay Ax to Bx or Bx to Ax | 1 | 4.8 | — | 4.5 | 1 | 3.9 | ns | |
| t_{PLH} t_{PHL} | Propagation Delay LE to Ax or Bx | 1.1 | 5.7 | — | 5.3 | 1.3 | 4.6 | ns | |
| t_{PLH} t_{PHL} | Propagation Delay CLK to Ax or Bx | 1.2 | 6.1 | — | 5.6 | 1.4 | 4.9 | ns | |
| t_{PZH} t_{PZL} | Output Enable Time OEBA to Ax | 1.3 | 6.3 | — | 6 | 1.1 | 5 | ns | |
| t_{PZH} t_{PZL} | Output Enable Time OEAB to Bx | 1 | 5.8 | — | 5.3 | 1 | 4.6 | ns | |
| t_{PHZ} t_{PLZ} | Output Disable Time OEBA to Ax | 1.3 | 5.3 | — | 4.6 | 1.3 | 4.2 | ns | |
| t_{PHZ} t_{PLZ} | Output Disable Time OEAB to Bx | 1.5 | 6.2 | — | 5.7 | 1.4 | 5 | ns | |
| t_{SU} | Setup Time, data before $\text{CLK}\uparrow$ | 2.2 | — | 2.1 | — | 1.7 | — | ns | |
| t_H | Hold Time, data after $\text{CLK}\uparrow$ | 0.6 | — | 0.6 | — | 0.7 | — | ns | |
| t_{SU} | Setup Time, data before $\text{LE}\downarrow$ | CLK HIGH | 1.9 | — | 1.6 | — | 1.5 | — | ns |
| | | CLK LOW | 1.3 | — | 1.1 | — | 1 | — | ns |
| t_H | Hold Time, data after $\text{LE}\downarrow$, CLK HIGH or LOW | 1.4 | — | 1.7 | — | 1.4 | — | ns | |
| t_W | Pulse Width, LE HIGH | 3.3 | — | 3.3 | — | 3.3 | — | ns | |
| t_W | Pulse Width, CLK HIGH or LOW | 3.3 | — | 3.3 | — | 3.3 | — | ns | |
| $t_{SK(o)}$ | Output Skew ⁽²⁾ | — | — | — | — | — | 500 | ps | |

NOTES:

- See test circuits and waveforms. $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$.
- Skew between any two outputs of the same package and switching in the same direction.

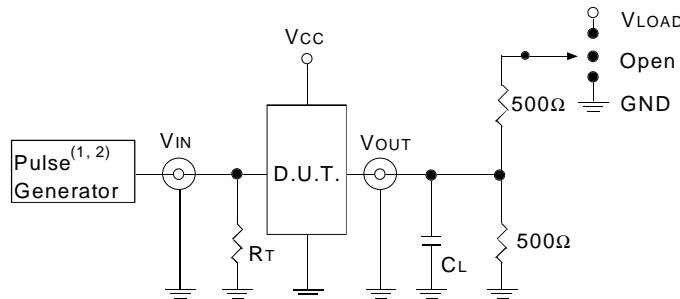
TEST CIRCUITS AND WAVEFORMS:

TEST CONDITIONS

| Symbol | V _{CC} (1)= 3.3V±0.3V | V _{CC} (1)= 2.7V | V _{CC} (2)= 2.5V±0.2V | Unit |
|-------------------|--------------------------------|---------------------------|--------------------------------|------|
| V _{LOAD} | 6 | 6 | 2 x V _{CC} | V |
| V _{IH} | 2.7 | 2.7 | V _{CC} | V |
| V _T | 1.5 | 1.5 | V _{CC} / 2 | V |
| V _{LZ} | 300 | 300 | 150 | mV |
| V _{HZ} | 300 | 300 | 150 | mV |
| C _L | 50 | 50 | 30 | pF |

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TEST CIRCUITS FOR ALL OUTPUTS



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DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

NOTES:

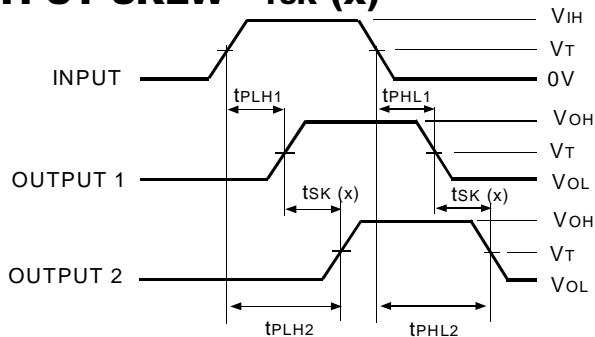
1. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns.
2. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_F ≤ 2ns; t_R ≤ 2ns.

SWITCH POSITION

| Test | Switch |
|---|-------------------|
| Open Drain Disable Low Enable Low | V _{LOAD} |
| Disable High Enable High | GND |
| All Other tests | Open |

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OUTPUT SKEW - TSK (x)



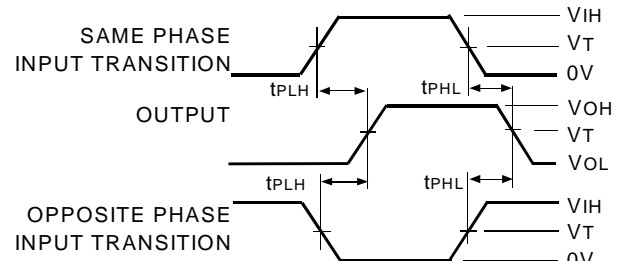
$$tsk(x) = |t_{PLH2} - t_{PLH1}| \text{ or } |t_{PHL2} - t_{PHL1}|$$

ALVC Link

NOTES:

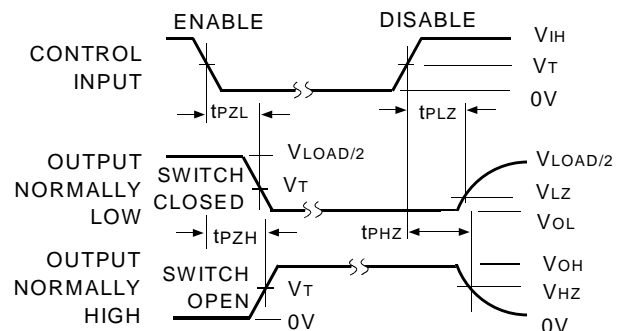
1. For tsk(o) OUTPUT1 and OUTPUT2 are any two outputs.
2. For tsk(b) OUTPUT1 and OUTPUT2 are in the same bank.

PROPAGATION DELAY



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ENABLE AND DISABLE TIMES

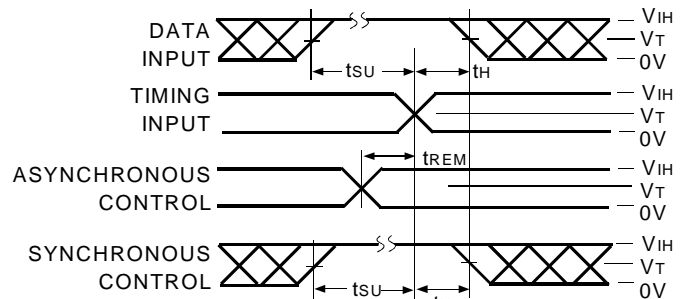


ALVC Link

NOTE:

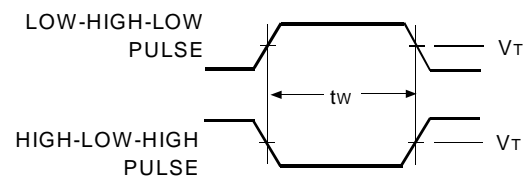
1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

SET-UP, HOLD, AND RELEASE TIMES



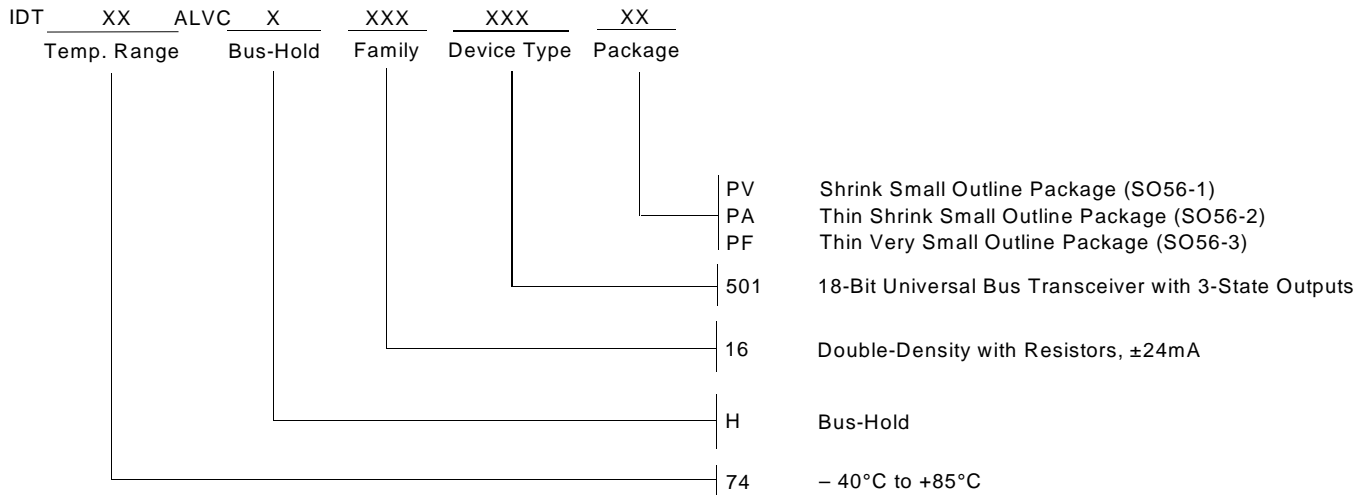
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PULSE WIDTH



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