Wireless Communication



OVERVIEW

The OneC[™] GSM is a high-performance, 3rdgeneration single-chip solution that integrates more than 100 man years of GSM-specific system experience into a single device. The OneCGSM is based on VISI's ViA[™] Standard **Communication Platform approach providing** flexibility for efficient customization, and giving GSM terminal manufacturers the design freedom necessary to innovate and differentiate in the highly competitive GSM market. The platform approach is also the first step towards combining GSM technology with applications such as mobile computing, personal digital assistants (PDAs) and global positioning systems (GPS), as well as towards next generation wireless communication systems like UMTS and IMT2000.

FEATURES

- Full GSM Phase 2 speech coding support including enhanced full rate, full rate and half rate (EFR/FR/HR)
- Typical standby time >500 hrs
- Typical talk time >7 hrs (battery 1200 mAh/3.6V)

- Supply voltage:
- \cdot 3V +/- 10% with 5V IO capability
- Highly flexible radio interface compatible with all established RF solutions in the market
- Extensive DSP and ARM firmware library
- High power efficiency:
 - \cdot 32 KHz idle time clocking
 - 3rd generation power management system
 - Real single chip through mixed-signal technology
- Integrated on-chip data services
- T/NT data services 0.3-14.4 Kbit/s
- · GPRS package-oriented data service
- · HSCSD multi-slot data capability

AVAILABILITY

VWS22100 OneC GSM samples are available now, with production following in the second half of 1998.

TOOLS

A wide set of development tools is available to support customers including:

• Development boards for software and RF integration

- Real-time trace support for HP165xx series and Lauterbach Trace 32
- VISI Vector[™] Multicore Development System (MDS) tools including compilers, simulator, multicore development chip and real-time dual-core debug tools

KEY BLOCKS

Multicores

The Vector Multicore Development Chip VVS 3670 provides the processing power for the OneC GSM. The VVS 3670 includes an ARM7TDMI RISC engine and the OakDSPcore. While the ARM7TDMI engine principally executes control and protocol processing functions, the OakDSPcore provides the resources for all GSM-specific signal processing as well as for complementary DSP features.

ARM7TDMI Subsystem

The embedded 32-bit ARM7TDMI RISC processor core drives the peripheral interfaces, power management, all three layers of the GSM protocol stack, the MMI software and some data applications. The ARM core can be run at multiple speeds, 13 or 26 MHz.

ViA[™] Standard Communication Platform

- OneC GSM Single-Chip Platform -

System FSBs and DSP Firmware	VBAFE	7	PRAM PROM		OakDSPcore		DRAM DROM		FiFo	GM SK	Single-mode
	AFE	PCM							FiFo	RX ADC	OneC GSM OneC DECT OneC PHS
Analog Cells	PLL & Clock		IT & Timer		Viterbi Cipher & Audio		Mode & Conf Reg		AGC & RSSI		Multi-mode
Microcontroller ARM 7Thumb	DA	1	SDI		AA Exchang		e Exchange		AFC		GSM/DECT DECT/PHS
	JTAG ICE		E Breaker		Buffer		Controls		TXB		PHS/AMPS GSM/SAT.
DSP OAK	мми		IT & Timer Mode & Conf Reg		BOOT CSGEN		ARM7TDMI		SPW RFEN		Multi-application GSM/PDA GSM/GPS

DSP Subsystem

The OakDSPcore provides the necessary processing power for all GSM-specific signal processing, (voice coding, equalization and channel coding) as well as for complementary features like echo cancellation and noise suppression, voice recognition and data compression. The DSP operating speed is configurable (13/26/39/52 MHz) depending on the performance needed. The DSP subsystem is mapped into the external and internal ARM address space. In the internal ARM address space, static locations are reserved for DSP configuration, for DSP status and for information exchange with flow control. Through this mechanism, signaling/ traffic information and processing results can be exchanged between the ARM and the DSP. The DSP can access external memory through a DMA mechanism arbitrated by the ARM MMU. This allows the external DSP software to be downloaded into the internal DSP memory, as well as allowing use of

external memory as workspace extension.

SDI Debug Capability

The SDI Smart Debug Interface provides fullcontext access to the Multicore and the complete address space. The Multicore can be stepped at any stage through programmable breakpoints in the ARM and DSP Software. Once a breakpoint is reached, the system information is transferred through a serial JTAG interface to a host computer. VISI's embedded trigger logic allows combined breakpoints for the DSP and ARM code to be set which forms the foundation for effective

real-time multicore debugging.

Radio Interface VISI's advanced mixed-signal technology allows the RF analog front-end to be integrated directly on-chip providing an efficient interface with the radio part of a GSM terminal. The OneC GSM RF interface features:

- Programmable TX power ramp (10-bit DAC)
- Either analog or a digital interface for Automatic RX Gain Control (AGC)

- GMSK modulator with 10 bit I/Q DAC and low noise filter
- I/Q RX 10-bit ADC
- Multi-Band Automatic Frequency Control
- Multi-Band Synthesiser Control
- Dynamic DC offset correction
- Digital RX filtering (optional)

Audio Interface

VLSI's advanced mixed-signal technology allows the audio front-end to be integrated on-chip. The codec achieves G712 requirements and enables the direct connection of the audio transducers to the chip. The OneC GSM programmable Audio Front-End Control adjusts the amplitude of audio signals.

Peripheral Blocks

The OneC GSM brings together all necessary peripheral blocks on-chip, minimizing external components and reducing cost and size (required PCB area). The on-chip peripherals include:

- 32 KHz Real-Time Clock (RTC)
- Two UARTs with integrated flow control
- IRDA interface
- 3/5V SIM controller
- PWM interface
- 10-bit AUXADC, 5 multiplexed inputs
- Multiple GPIOs
- Keypad controller
- Two general-purpose serial bus interfaces
- Alerter
- LCD driver

DSP and ARM firmware Librar y VLSI's GSM DSP and ARM firmware library includes all GSM Phase 2 algorithms as well as a wide set of complementary DSP features/algorithms. The library consists of:

- Voice coding algorithms for FR, EFR, HR
- Equalizer algorithm
- Channel coder algorithm
- Data compression/coding for T/NT data, GPRS, HSCSD, V42bis
- Echo cancellation
- Noise suppression
- Voice recognition

• VISI L1 GSM protocol software modules to accelerate software integration

CUSTOMIZATION

In today's highly competitive GSM market, cost efficiency is just the basic entry qualification. Non-stop innovation and the ability to quickly differentiate products are the determining elements that quarantee success. The OneC GSM was developed using VLSI's unique building foundation, the ViA[™] Standard Communication Platform, a universal wireless development environment that can combine multiple standards and that forms the basis of current and future solutions. ViA[™] provides terminal manufactures high flexibility and room for innovation at market-leading cost and the performance of a real single-chip solution. The customization process is also supported by a RAM-based OneC GSM development chip allowing customers to implement their own DSP code set to complement VLSI's readily available DSP and ARM firmware library. This approach allows terminal manufacturers to customize the OneC GSM according to their requirements, or to complement their designs with OneC GSM system-blocks and DSP firmware.

PACKAGE

The OneC GSM standard package is a 180FPBGA (Fine Pitch Ball Gate Array) with a 12x12 mm footprint.

FUTURE

During 1998, the OneC GSM platform will be migrated to 0.25 process technology, reducing cost, lowering the supply voltage to 1.5-2.5V and greatly enhancing the performance. All VISI wireless products follow the same Standard Communication Platform approach. This provides the ideal base for future multimode, single-chip solutions combining GSM with DECT, PHS, AMPS or Satellite technology. It is a major step towards next generation mobile standards such as UMTS/IMT2000.

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