

100MHz, High Input Impedance, Very Wideband, Uncompensated Operational Amplifiers

HA-2620/2625 are bipolar operational amplifiers that feature very high input impedance (500M Ω , HA-2620) coupled with wideband AC performance. The high resistance of the input stage is complemented by low offset voltage (0.5mV, HA-2620) and low bias and offset current (1nA, HA-2620) to facilitate accurate signal processing. Input offset can be reduced further by means of an external nulling potentiometer. The 100MHz gain bandwidth product (HA-2620/2625 are stable for closed loop gains greater than 5), 35V/ μ s slew rate and 150kV/V open loop gain enables HA-2620/2625 to perform high gain amplification of very fast, wideband signals. These dynamic characteristics, coupled with fast settling times, make these amplifiers ideally suited to pulse amplification designs as well as high frequency (e.g., video) applications. The frequency response of the amplifier can be tailored to exact design requirements by means of an external bandwidth control capacitor connected from the Comp pin to GND.

In addition to its application in pulse and video amplifier designs, HA-2620/2625 is particularly suited to other high performance designs such as high-gain low distortion audio amplifiers, high-Q and wideband active filters and high-speed comparators. For more information, please refer to Application Notes AN509, AN519 and AN546.

Ordering Information

PART NUMBER (BRAND)	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HA2-2620-2	-55 to 125	8 Pin Metal Can	T8.C
HA2-2625-5	0 to 75	8 Pin Metal Can	T8.C
HA3-2625-5	0 to 75	8 Ld PDIP	E8.3
HA9P2625-9 (H26259)	-40 to 85	8 Ld SOIC	M8.15

Features

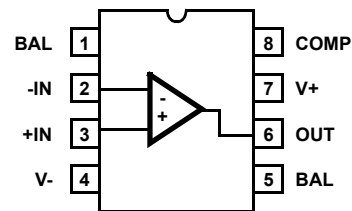
- Gain Bandwidth Product ($A_V \geq 5$) 100MHz
- High Input Impedance 500M Ω
- Low Input Bias Current. 1nA
- Low Input Offset Current 1nA
- Low Input Offset Voltage 0.5mV
- High Gain 150kV/V
- Slew Rate 35V/ μ s
- Output Short Circuit Protection
- Compensation Pin for Unity Gain Capability

Applications

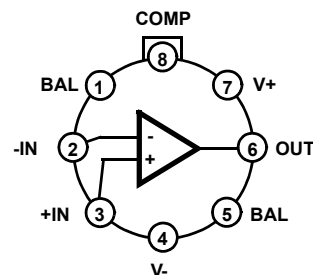
- Video and RF Amplifier
- Pulse Amplifier
- Audio Amplifiers and Filters
- High-Q Active Filters
- High Speed Comparators
- Low Distortion Oscillator

Pinouts

HA-2625 (PDIP, SOIC)
TOP VIEW



HA-2620, HA-2625 (METAL CAN)
TOP VIEW



HA-2620, HA-2625

Absolute Maximum Ratings

Supply Voltage (Between V+ and V- Terminals)	45V
Differential Input Voltage	12V
Peak Output Current	Full Short Circuit Protection

Operating Conditions

Temperature Range	
HA-2620-2	-55°C to 125°C
HA-2625-5	0°C to 75°C
HA-2625-9	-40°C to 85°C

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
PDIP Package	117	N/A
SOIC Package	165	N/A
Metal Can Package	165	80
Maximum Junction Temperature (Hermetic Package)	175°C	
Maximum Junction Temperature (Plastic Package)	150°C	
Maximum Storage Temperature Range	-65°C to 150°C	
Maximum Lead Temperature (Soldering 10s)	300°C	
(SOIC - Lead Tips Only)		

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

- θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications $V_{SUPPLY} = \pm 15V$, Unless Otherwise Specified

PARAMETER	TEMP. (°C)	HA-2620-2			HA-2625-5, -9			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS								
Offset Voltage (Note 3)	25	-	0.5	4	-	3	5	mV
	Full	-	2	6	-	-	7	mV
Average Offset Voltage Drift	Full	-	5	-	-	5	-	$\mu V/^\circ C$
Bias Current	25	-	1	15	-	5	25	nA
	Full	-	10	35	-	-	40	nA
Offset Current	25	-	1	15	-	5	25	nA
	Full	-	5	35	-	-	40	nA
Differential Input Resistance (Note 2)	25	65	500	-	40	300	-	M Ω
Input Noise Voltage Density (f = 1kHz)	25	-	11	-	-	11	-	nV/ \sqrt{Hz}
Input Noise Current Density (f = 1kHz)	25	-	0.16	-	-	0.16	-	pA/ \sqrt{Hz}
Common Mode Range	Full	± 11	± 12	-	± 11	± 12	-	V
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Notes 4, 5)	25	100	150	-	80	150	-	kV/V
	Full	70	-	-	70	-	-	kV/V
Common Mode Rejection Ratio (Note 6)	Full	80	100	-	74	100	-	dB
Minimum Stable Gain	25	5	-	-	5	-	-	V/V
Gain Bandwidth Product (Notes 4, 7, 8)	25	-	100	-	-	100	-	MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing (Note 4)	Full	± 10	± 12	-	± 10	± 12	-	V
Output Current (Note 5)	25	± 15	± 22	-	± 10	± 18	-	mA
Full Power Bandwidth (Notes 4, 5, 9, 13)	25	400	600	-	320	600	-	kHz
TRANSIENT RESPONSE (Note 8)								
Rise Time (Notes 4, 9, 10)	25	-	17	45	-	17	45	ns
Slew Rate (Notes 4, 9, 10, 12)	25	± 25	± 35	-	± 20	± 35	-	V/ μs

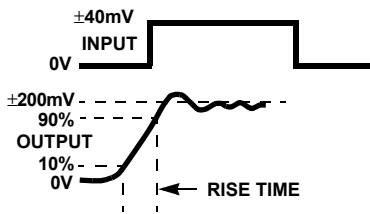
Electrical Specifications $V_{SUPPLY} = \pm 15V$, Unless Otherwise Specified (Continued)

PARAMETER	TEMP. (°C)	HA-2620-2			HA-2625-5, -9			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
POWER SUPPLY CHARACTERISTICS								
Supply Current	25	-	3	3.7	-	3	4	mA
Power Supply Rejection Ratio (Note 11)	Full	80	90	-	74	90	-	dB

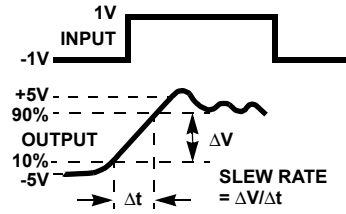
NOTES:

- This parameter value guaranteed by design calculations.
- Offset may be externally adjusted to zero.
- $R_L = 2k\Omega$.
- $V_{OUT} = \pm 10V$.
- $V_{CM} = \pm 10V$.
- $V_{OUT} < 90mV$.
- 40dB Gain.
- See Transient Response Test Circuits and Waveforms.
- $A_V = 5$ (The HA-2620 family is not stable at unity gain without external compensation).
- $\Delta V_S = \pm 5V$.
- $V_{OUT} = \pm 5V$.
- Full Power Bandwidth guaranteed by slew rate measurement: $FPBW = \frac{Slew\ Rate}{2\pi V_{PEAK}}$.

Test Circuits and Waveforms

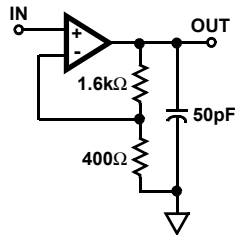


TRANSIENT RESPONSE

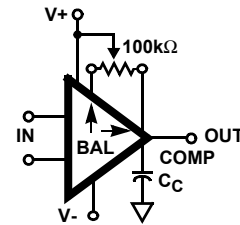


SLEW RATE

NOTE: Measured on both positive and negative transitions from 0V to +200mV and 0V to -200mV at output.



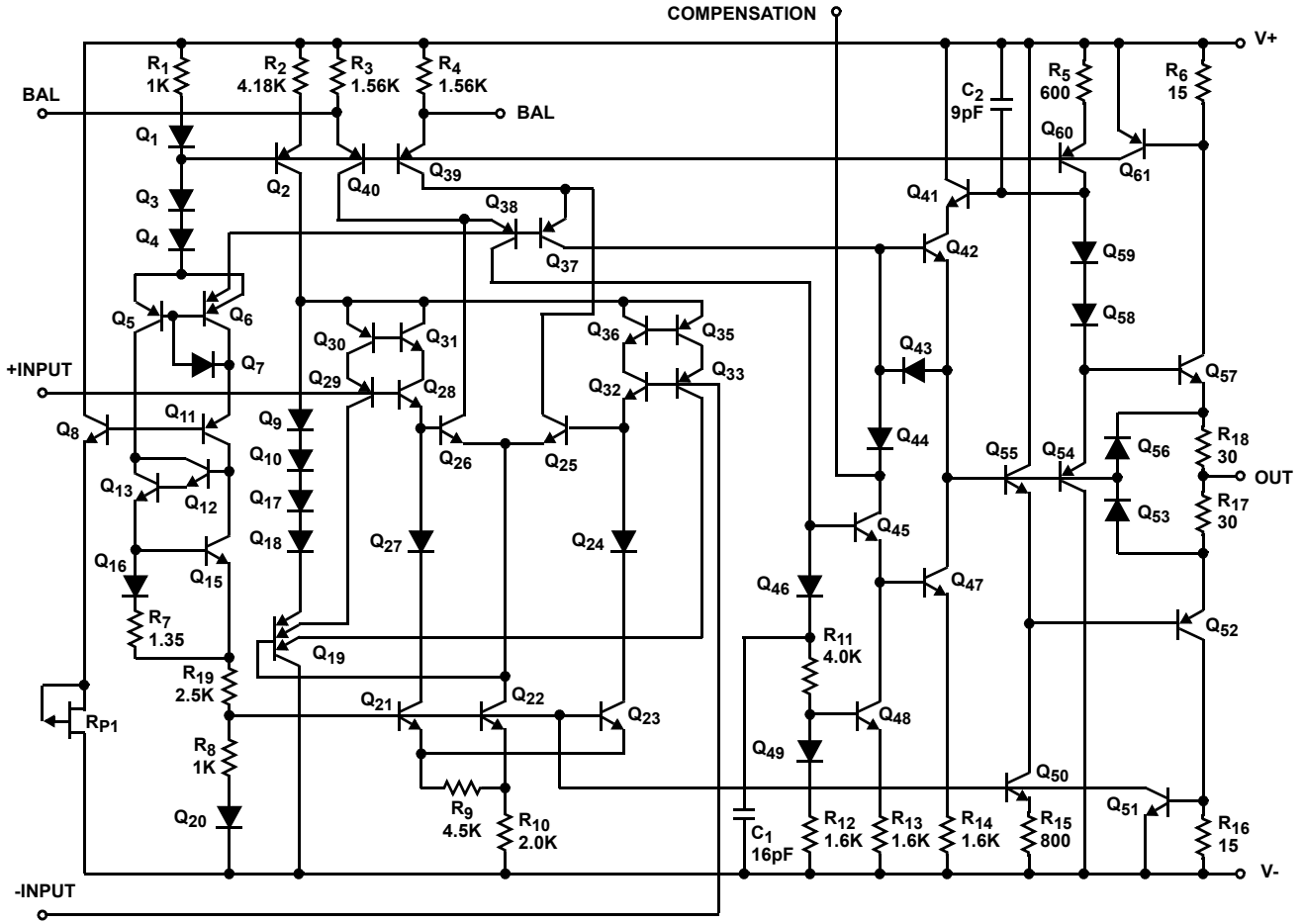
SLEW RATE AND TRANSIENT RESPONSE



NOTE: Tested Offset Adjustment is $|V_{OS} + 1mV|$ minimum referred to output. Typical range is $\pm 10mV$ with $R_T = 100k\Omega$.

SUGGESTED V_{OS} ADJUSTMENT AND COMPENSATION HOOK-UP

Schematic Diagram



Typical Applications

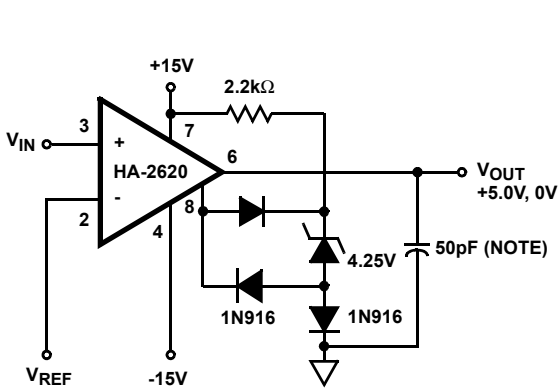


FIGURE 1. HIGH INPUT IMPEDANCE COMPARATOR

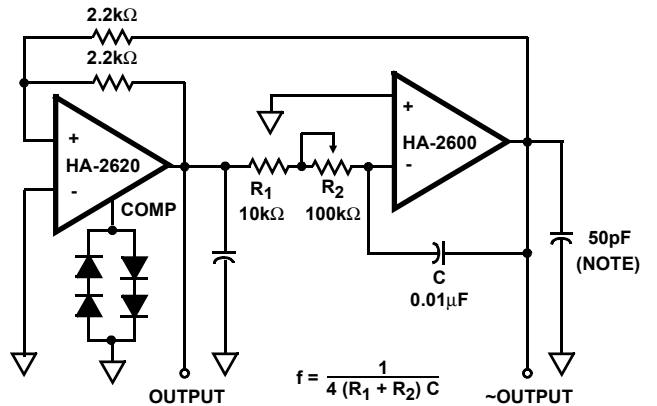
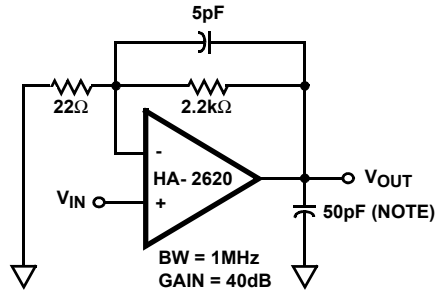


FIGURE 2. FUNCTION GENERATOR

Typical Applications (Continued)



NOTE: A small load capacitance of at least 30pF (including stray capacitance) is recommended to prevent possible high frequency oscillations.

FIGURE 3. VIDEO AMPLIFIER

Typical Performance Curves $V_S = \pm 15V, T_A = 25^\circ C$, Unless Otherwise Specified

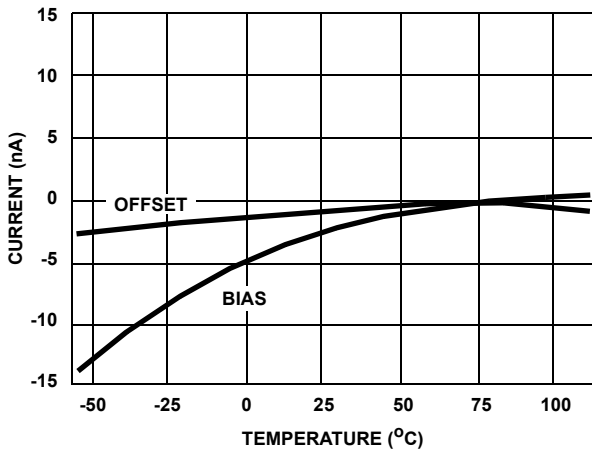


FIGURE 4. INPUT BIAS CURRENT AND OFFSET CURRENT vs TEMPERATURE

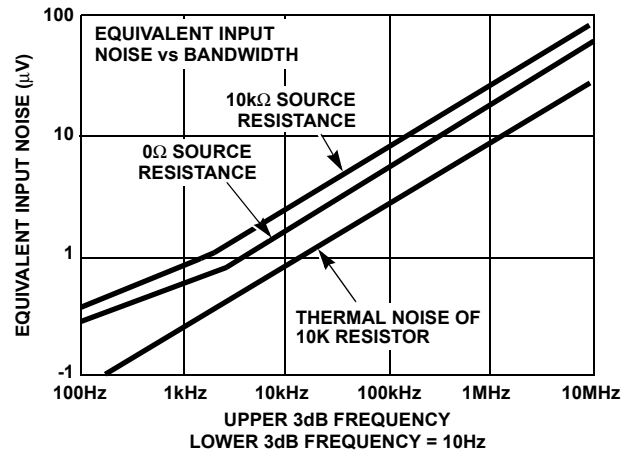


FIGURE 5. BROADBAND NOISE CHARACTERISTICS

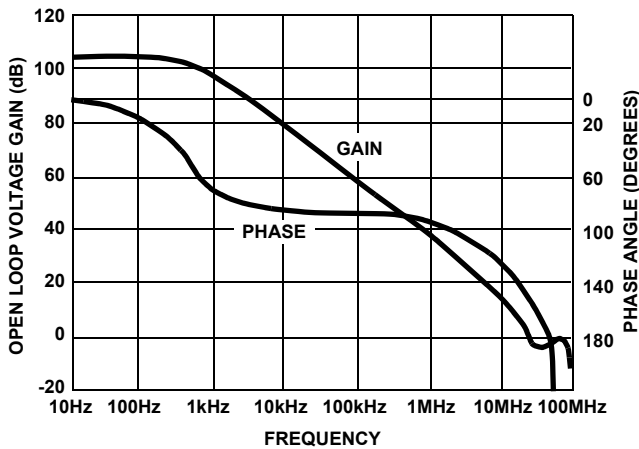


FIGURE 6. OPEN LOOP FREQUENCY RESPONSE

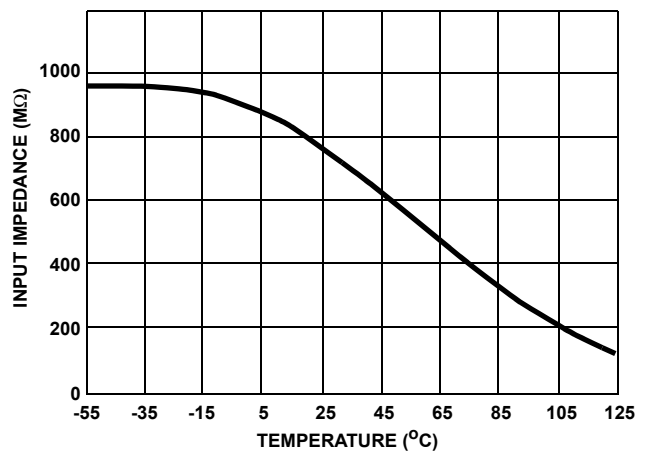


FIGURE 7. INPUT IMPEDANCE vs TEMPERATURE, 100Hz

Typical Performance Curves $V_S = \pm 15V, T_A = 25^\circ C$, Unless Otherwise Specified (Continued)

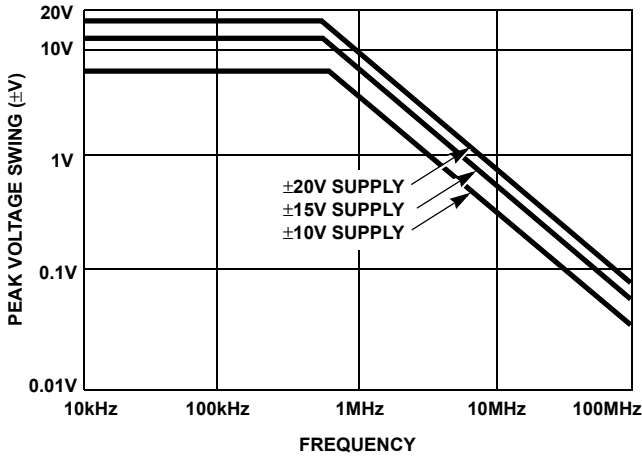
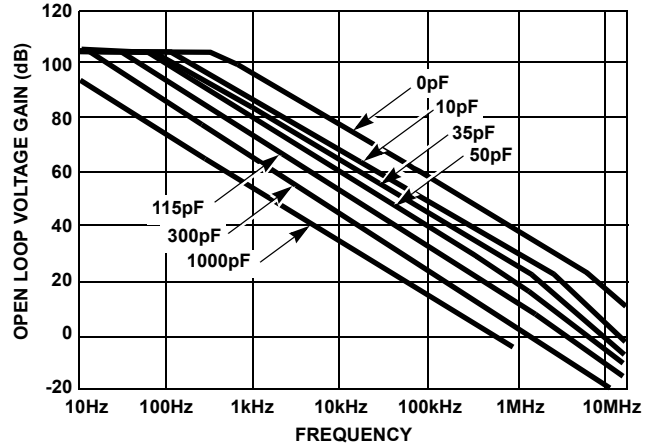


FIGURE 8. OUTPUT VOLTAGE SWING vs FREQUENCY



NOTE: External Compensation is required for closed loop gain < 5. If external compensation is used, also connect 100pF capacitor from output to ground.

FIGURE 9. OPEN LOOP FREQUENCY RESPONSE FOR VARIOUS VALUES OF CAPACITORS FROM COMP. PIN TO GND

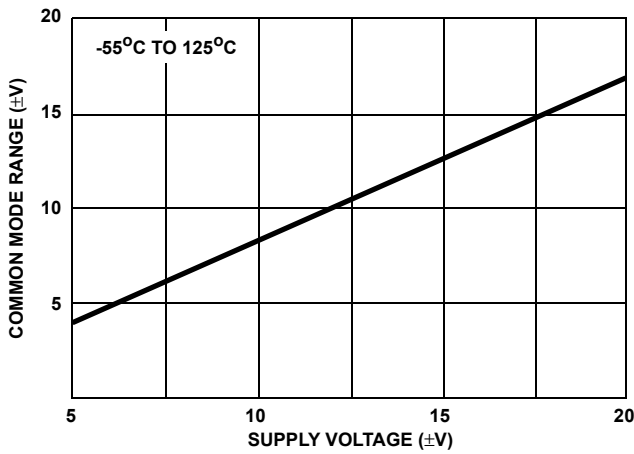


FIGURE 10. COMMON MODE VOLTAGE RANGE vs SUPPLY VOLTAGE

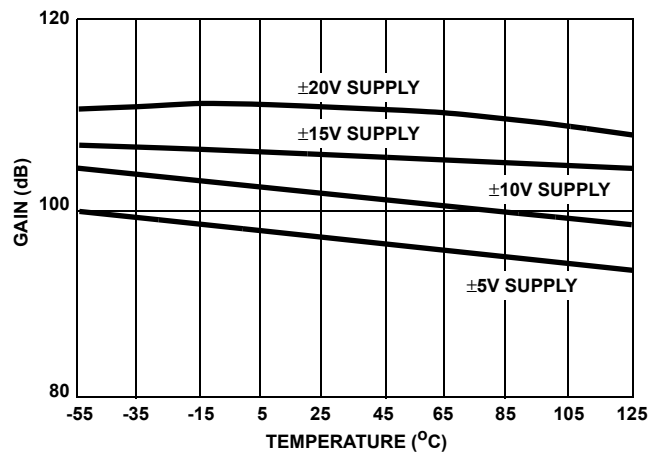


FIGURE 11. OPEN LOOP VOLTAGE GAIN vs TEMPERATURE

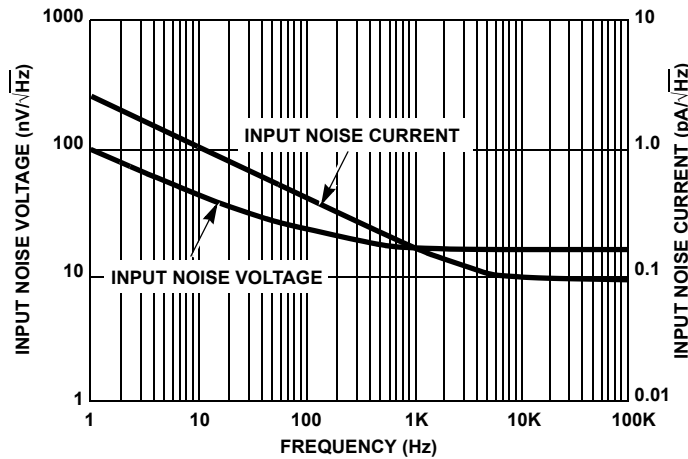


FIGURE 12. NOISE DENSITY vs FREQUENCY

Die Characteristics

DIE DIMENSIONS:

69 mils x 56 mils x 19 mils
1750 μ m x 1420 μ m x 483 μ m

METALLIZATION:

Type: Al, 1% Cu
Thickness: 16k \AA \pm 2k \AA

SUBSTRATE POTENTIAL (POWERED UP):

Unbiased

PASSIVATION:

Type: Nitride (Si_3N_4) over Silox (SiO_2 , 5% Phos.)
Silox Thickness: 12k \AA \pm 2k \AA
Nitride Thickness: 3.5k \AA \pm 1.5k \AA

TRANSISTOR COUNT:

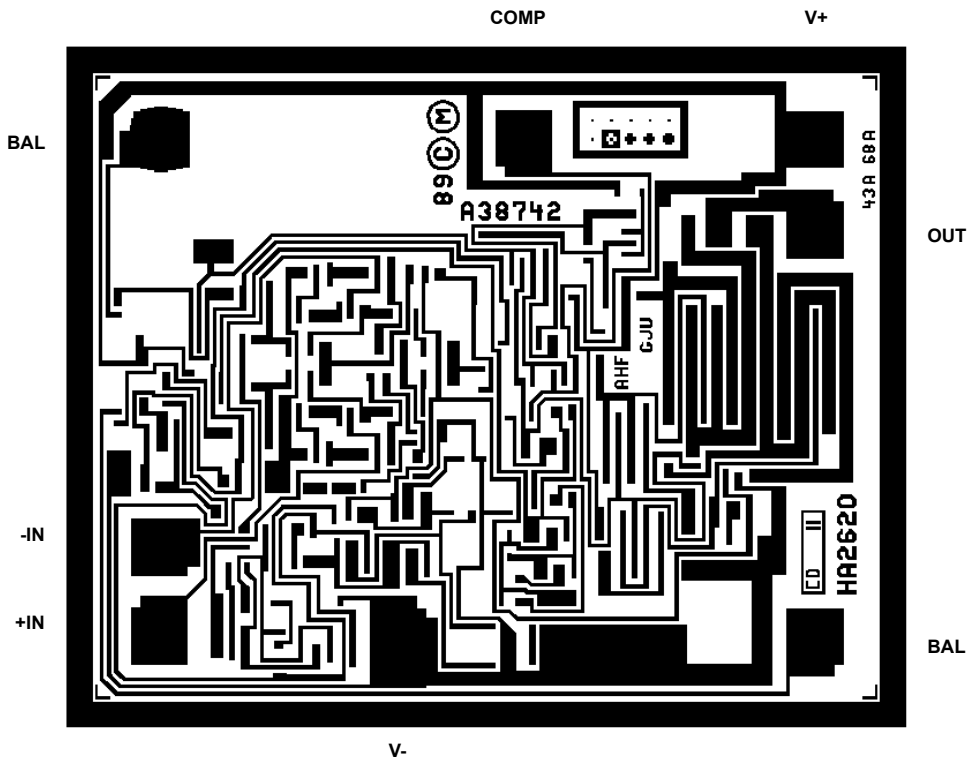
140

PROCESS:

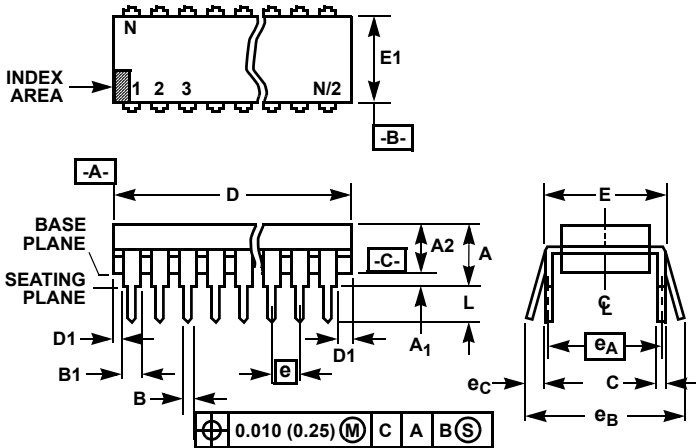
Bipolar Dielectric Isolation

Metallization Mask Layout

HA-2620, HA-2625



Dual-In-Line Plastic Packages (PDIP)



NOTES:

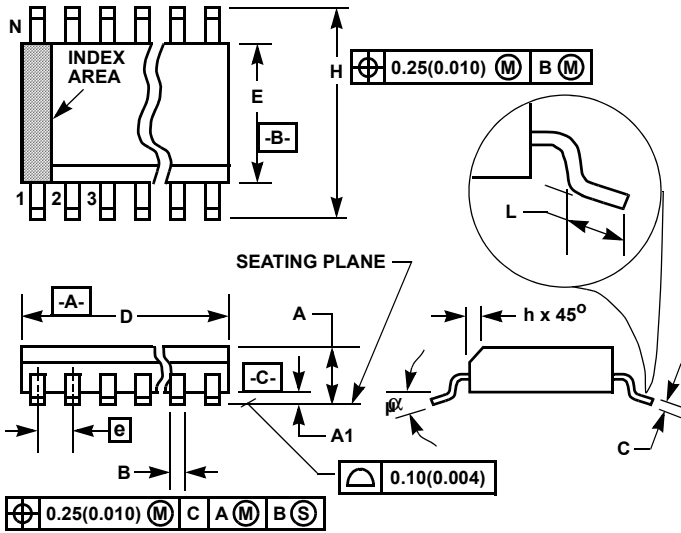
1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E8.3 (JEDEC MS-001-BA ISSUE D)
8 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8, 10
C	0.008	0.014	0.204	0.355	-
D	0.355	0.400	9.01	10.16	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e _A	0.300 BSC		7.62 BSC		6
e _B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	8		8		9

Rev. 0 12/93

Small Outline Plastic Packages (SOIC)



M8.15 (JEDEC MS-012-AA ISSUE C)
8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

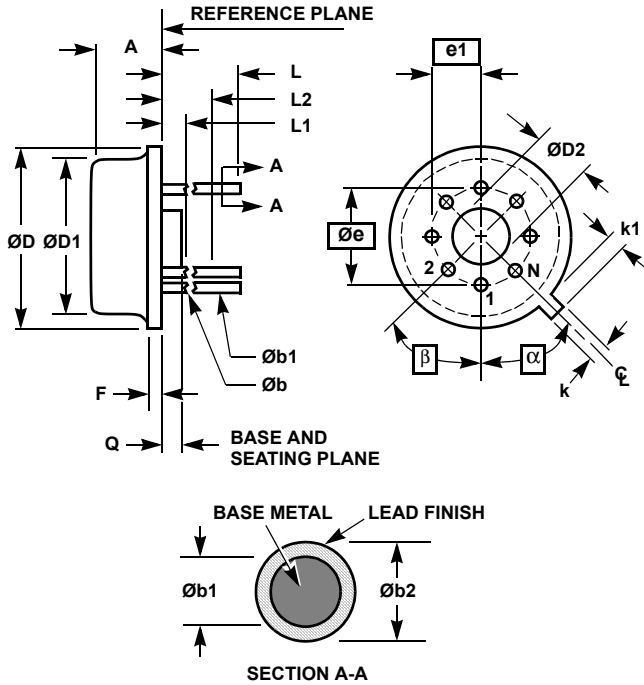
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.1890	0.1968	4.80	5.00	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	8		8		7
α	0°	8°	0°	8°	-

NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

Rev. 0 12/93

Metal Can Packages (Can)



**T8.C MIL-STD-1835 MACY1-X8 (A1)
8 LEAD METAL CAN PACKAGE**

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.165	0.185	4.19	4.70	-
$\varnothing b$	0.016	0.019	0.41	0.48	1
$\varnothing b1$	0.016	0.021	0.41	0.53	1
$\varnothing b2$	0.016	0.024	0.41	0.61	-
$\varnothing D$	0.335	0.375	8.51	9.40	-
$\varnothing D1$	0.305	0.335	7.75	8.51	-
$\varnothing D2$	0.110	0.160	2.79	4.06	-
e	0.200 BSC		5.08 BSC		-
e1	0.100 BSC		2.54 BSC		-
F	-	0.040	-	1.02	-
k	0.027	0.034	0.69	0.86	-
k1	0.027	0.045	0.69	1.14	2
L	0.500	0.750	12.70	19.05	1
L1	-	0.050	-	1.27	1
L2	0.250	-	6.35	-	1
Q	0.010	0.045	0.25	1.14	-
α	45° BSC		45° BSC		3
β	45° BSC		45° BSC		3
N	8		8		4

Rev. 0 5/18/94

NOTES:

1. (All leads) $\varnothing b$ applies between L1 and L2. $\varnothing b1$ applies between L2 and 0.500 from the reference plane. Diameter is uncontrolled in L1 and beyond 0.500 from the reference plane.
2. Measured from maximum diameter of the product.
3. α is the basic spacing from the centerline of the tab to terminal 1 and β is the basic spacing of each lead or lead position (N - 1 places) from α , looking at the bottom of the package.
4. N is the maximum number of terminal positions.
5. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
6. Controlling dimension: INCH.

All Intersil semiconductor products are manufactured, assembled and tested under **ISO9000** quality systems certification.

Intersil semiconductor products are sold by description only. Intersil Corporation reserves the right to make changes in circuit design and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.

For information regarding Intersil Corporation and its products, see web site www.intersil.com