Document Title

8M x 8 Bit NAND Flash Memory

Revision History

Revision No.	History	Draft Date	Remark
0.0	Initial issue.	Jul. 24 . 2001	Advance
0.1	1. I_{OL}(R/$\overline{B}$) of 1.8V device is changed. -min. Value: 7mA -->3mA -typ. Value: 8mA -->4mA 2. Package part number is modified. K9F6408U0C-Y ---> K9F6408U0C_T 3. AC parameter is changed. tRP(min.) : 30ns --> 25ns	Nov. 5 . 2001	Preliminary
0.2	1. TBGA package is changed. - 9mmX11mm 63ball TBGA ---> 6mmX8.5mm 48ball TBGA 2. Part number(TBGA package part number) is changed - K9F6408Q0C-D ----> K9F6408Q0C-B - K9F6408U0C-D -----> K9F6408U0C-B 3. K9F6408U0C-BCB0,BIB0 products are added	Nov. 12 . 2001	
0.3	1. WSOP1 package is added. - Part number : K9F6408U0C_VCB0,VIBO	Mar. 13 . 2002	
0.4	1. Add the Rp vs tr ,tf & Rp vs ibusy graph for 1.8V device (Page 28) 2. Add the data protection Vcc guidence for 1.8V device - below about 1.1V. (Page 29)	Nov, 21th 2002	
0.5	The min. Vcc value 1.8V devices is changed. K9F64XXQ0C : Vcc 1.65V~1.95V --> 1.70V~1.95V	Mar. 5th 2003	
0.6	Pb-free Package is added. K9F6408U0C-QCB0,QIB0 K9F6408U0C-HCB0,HIB0 K9F6408Q0C-HCB0,HIB0 K9F6408U0C-FCB0,FIB0	Mar. 13 . 2003	
0.7	Note is added. (VIL can undershoot to -0.4V and VIH can overshoot to VCC +0.4V for durations of 20 ns or less.)	Jul. 4th. 2003	

Note : For more detailed features and specifications including FAQ, please refer to Samsung' s Flash web site.
http://www.samsung.com/Products/Semiconductor/Flash/TechnicalInfo/datasheets.htm

8M x 8 Bit Bit NAND Flash Memory

PRODUCT LIST

Part Number	Vcc Range	Organization	PKG Type
K9F6408Q0C-B,H	1.70 ~ 1.95V	X8	TBGA
K9F6408U0C-B,H	2.7 ~ 3.6V		
K9F6408U0C-T,Q			TSOP II
K9F6408U0C-V,F			WSOP I

FEATURES

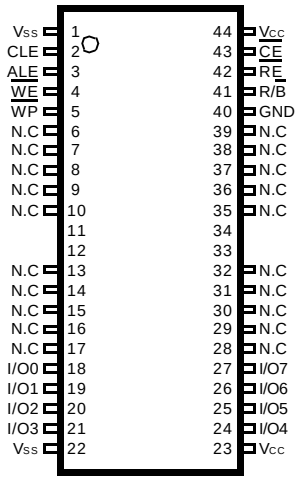
- Voltage Supply
  - 1.8V device(K9F6408Q0C) : 1.70~1.95V
  - 3.3V device(K9F6408U0C) : 2.7 ~ 3.6 V
- Organization
  - Memory Cell Array : (8M + 256K)bit x 8bit
  - Data Register : (512 + 16)bit x8bit
- Automatic Program and Erase
  - Page Program : (512 + 16)Byte
  - Block Erase : (8K + 256)Byte
- 528-Byte Page Read Operation
  - Random Access : 10μs(Max.)
  - Serial Page Access
    - 1.8V device(K9F6408Q0C) : 50ns
    - 3.3V device(K9F6408U0C) : 50ns
- Fast Write Cycle Time
  - Program Time
    - 1.8V device(K9F6408Q0C) : 200μs(Typ.)
    - 3.3V device(K9F6408U0C) : 200μs(Typ.)
  - Block Erase Time : 2ms(Typ.)
- Command/Address/Data Multiplexed I/O Port
- Hardware Data Protection
  - Program/Erase Lockout During Power Transitions
- Reliable CMOS Floating-Gate Technology
  - Endurance : 100K Program/Erase Cycles
  - Data Retention : 10 Years
- Command Register Operation
- Package
  - K9F6408U0C-TCB0/TIB0 :
    44(40) - Lead TSOP Type II (400mil / 0.8 mm pitch)
  - K9F6408Q0C-BCB0/BIB0
    48- Ball TBGA (6 x 8.5 /0.8mm pitch , Width 1.0 mm)
  - K9F6408U0C-VCB0/VIB0
    48 - Pin WSOP I (12X17X0.7mm)
  - K9F6408U0C-QCB0/QIB0 : Pb-free Package
    44(40) - Lead TSOP Type II (400mil / 0.8 mm pitch)
  - K9F6408Q0C-HCB0/HIB0 : Pb-free Package
    48- Ball TBGA (6 x 8.5 /0.8mm pitch , Width 1.0 mm)
  - K9F6408U0C-FCB0/FIB0 : Pb-free Package
    48 - Pin WSOP I (12X17X0.7mm)
    * K9F6408U0C-V,F(WSOPI) is the same device as K9F6408U0C-T,Q(TSOPII) except package type.

GENERAL DESCRIPTION

The K9F6408X0C is a 8M(8,388,608)x8bit NAND Flash Memory with a spare 256K(262,144)x8bit. The device is offered in 1.8V or 3.3V Vcc. Its NAND cell provides the most cost-effective solution for the solid state mass storage market. A program operation programs the 528-byte page in typical 200μs and an erase operation can be performed in typical 2ms on an 8K-byte block. Data in the page can be read out at 50ns cycle time per byte. The I/O pins serve as the ports for address and data input/output as well as command inputs. The on-chip write controller automates all program and erase functions including pulse repetition, where required, and internal verification and margining of data. Even the write-intensive systems can take advantage of the K9F6408X0C′s extended reliability of 100K program/erase cycles by providing ECC(Error Correcting Code) with real time mapping-out algorithm. These algorithms have been implemented in many mass storage applications and also the spare 16 bytes of a page combined with the other 512 bytes can be utilized by system-level ECC. The K9F6408X0C is an optimum solution for large nonvolatile storage applications such as solid state file storage, digital voice recorder, digital still camera and other portable applications requiring non-volatility.

PIN CONFIGURATION (TSOP II)

K9F6408U0C-TCB0,QCB0/TIB0,QIB0

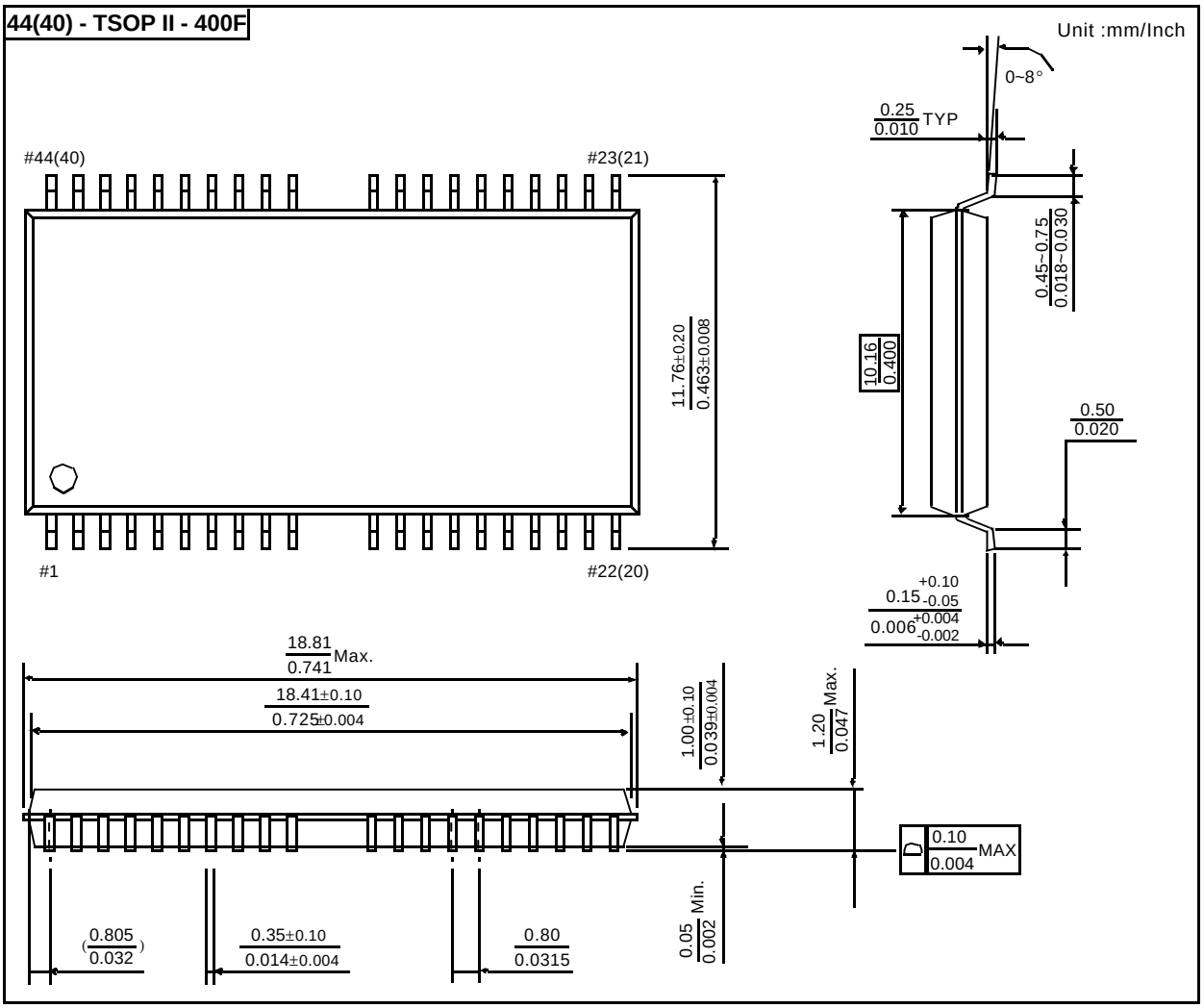


PACKAGE DIMENSIONS

44(40) LEAD/LEAD FREE PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE(II)

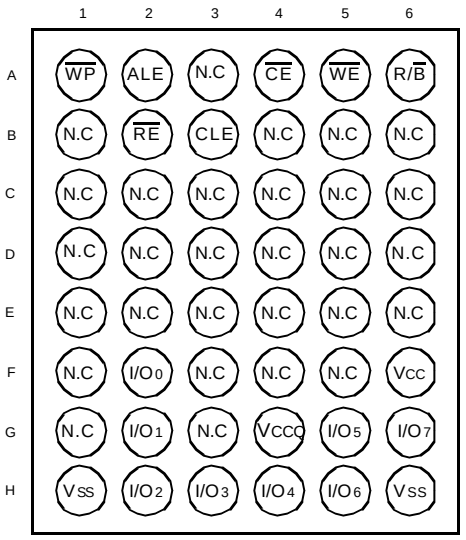
44(40) - TSOP II - 400F

Unit :mm/Inch



PIN CONFIGURATION (TBGA)

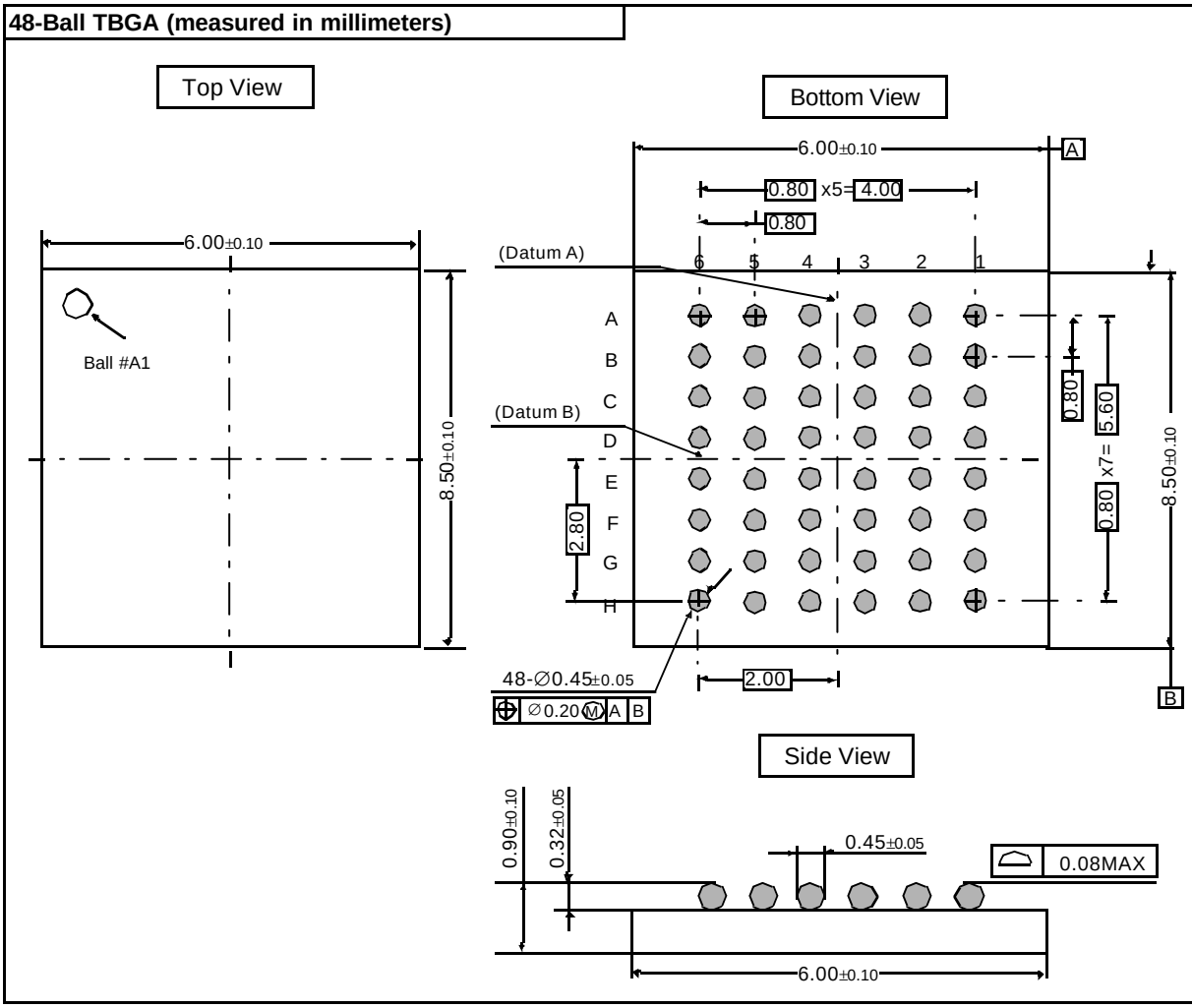
K9F6408X0C-BCB0,HCB0/BIB0,HIB0



(Top View)

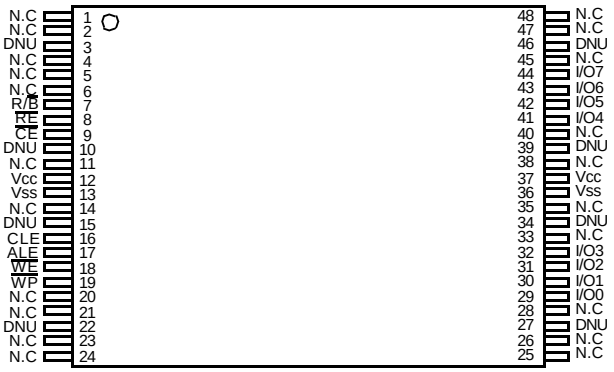
PACKAGE DIMENSIONS

48-Ball TBGA (measured in millimeters)



PIN CONFIGURATION (WSOP1)

K9F6408U0C-VCB0,FCB0/VIB0,FIB0

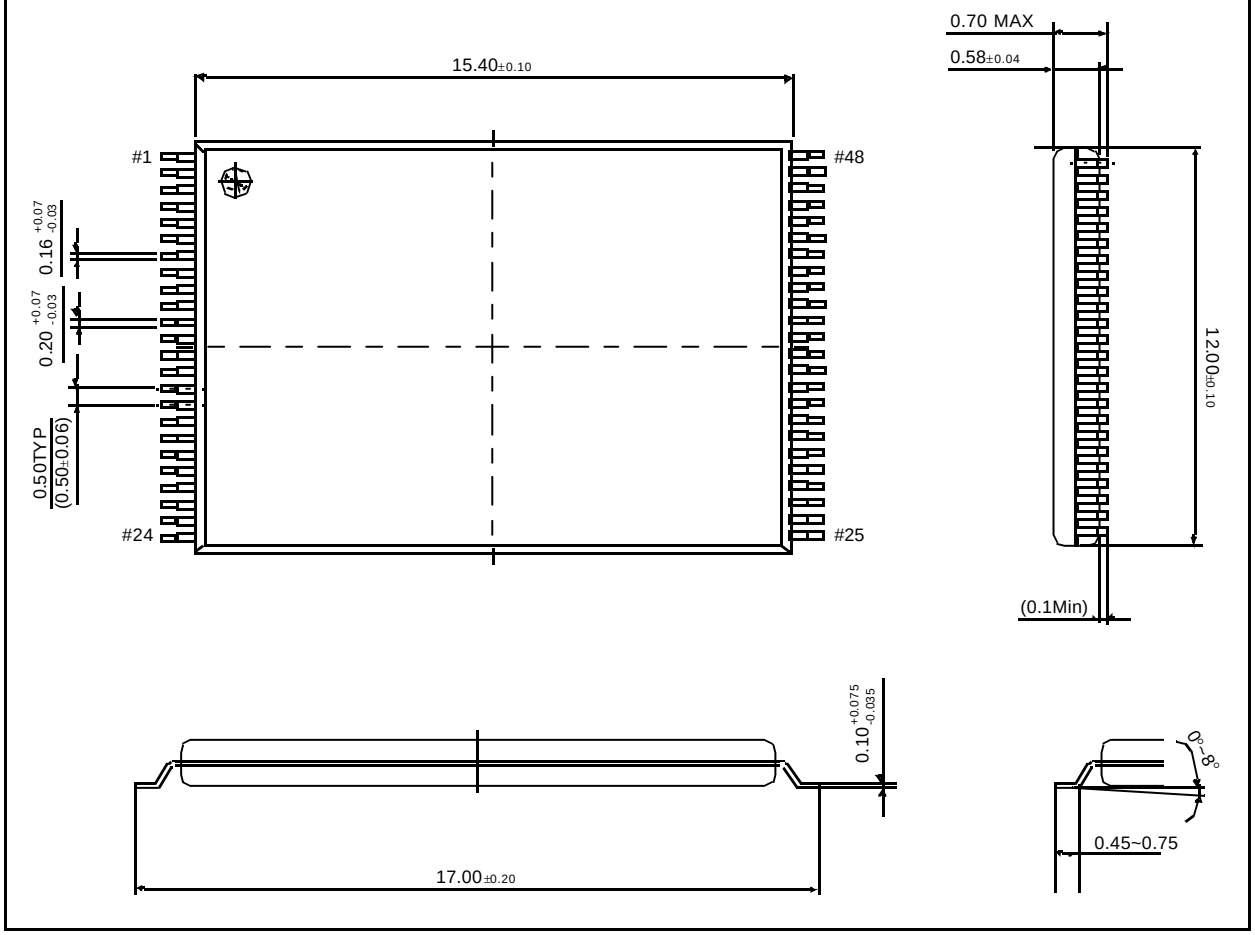


PACKAGE DIMENSIONS

48-PIN LEAD/LEAD FREE PLASTIC VERY VERY THIN SMALL OUT-LINE PACKAGE TYPE (I)

48 - WSOP1 - 1217F

Unit :mm



PIN DESCRIPTION

Pin Name	Pin Function
$I/O_0 \sim I/O_7$	**DATA INPUTS/OUTPUTS** The I/O pins are used to input command, address and data, and to output data during read operations. The I/O pins float to high-z when the chip is deselected or when the outputs are disabled.
CLE	**COMMAND LATCH ENABLE** The CLE input controls the activating path for commands sent to the command register. When active high, commands are latched into the command register through the I/O ports on the rising edge of the $\overline{WE}$ signal.
ALE	**ADDRESS LATCH ENABLE** The ALE input controls the activating path for address to the internal address registers. Addresses are latched on the rising edge of $\overline{WE}$ with ALE high.
$\overline{CE}$	**CHIP ENABLE** The $\overline{CE}$ input is the device selection control. When the device is in the Busy state, $\overline{CE}$ high is ignored, and the device does not return to standby mode in program or erase operation. Regarding $\overline{CE}$ control during read operation, refer to ' Page read' section of Device operation .
$\overline{RE}$	**READ ENABLE** The $\overline{RE}$ input is the serial data-out control, and when active drives the data onto the I/O bus. Data is valid tREA after the falling edge of $\overline{RE}$ which also increments the internal column address counter by one.
$\overline{WE}$	**WRITE ENABLE** The $\overline{WE}$ input controls writes to the I/O port. Commands, address and data are latched on the rising edge of the $\overline{WE}$ pulse.
$\overline{WP}$	**WRITE PROTECT** The $\overline{WP}$ pin provides inadvertent write/erase protection during power transitions. The internal high voltage generator is reset when the $\overline{WP}$ pin is active low.
$R/\overline{B}$	**READY/BUSY OUTPUT** The $R/\overline{B}$ output indicates the status of the device operation. When low, it indicates that a program, erase or random read operation is in process and returns to high state upon completion. It is an open drain output and does not float to high-z condition when the chip is deselected or when outputs are disabled.
V_{CCQ}	**OUTPUT BUFFER POWER** V_{CCQ} is the power supply for Output Buffer. V_{CCQ} is internally connected to Vcc, thus should be biased to Vcc.
Vcc	**POWER** V_{CC} is the power supply for device.
Vss	**GROUND**
N.C	**NO CONNECTION** Lead is not internally connected.
GND	**GND INPUT FOR ENABLING SPARE AREA** To do sequential read mode including spare area , connect this input pin to Vss or set to static low state or to do sequential read mode excluding spare area , connect this input pin to Vcc or set to static high state .
DNU	**DO NOT USE** Leave it disconnected.

NOTE : Connect all V_{CC} and V_{SS} pins of each device to common power supply outputs.

Do not leave V_{CC} or V_{SS} disconnected.

Figure 1. FUNCTIONAL BLOCK DIAGRAM

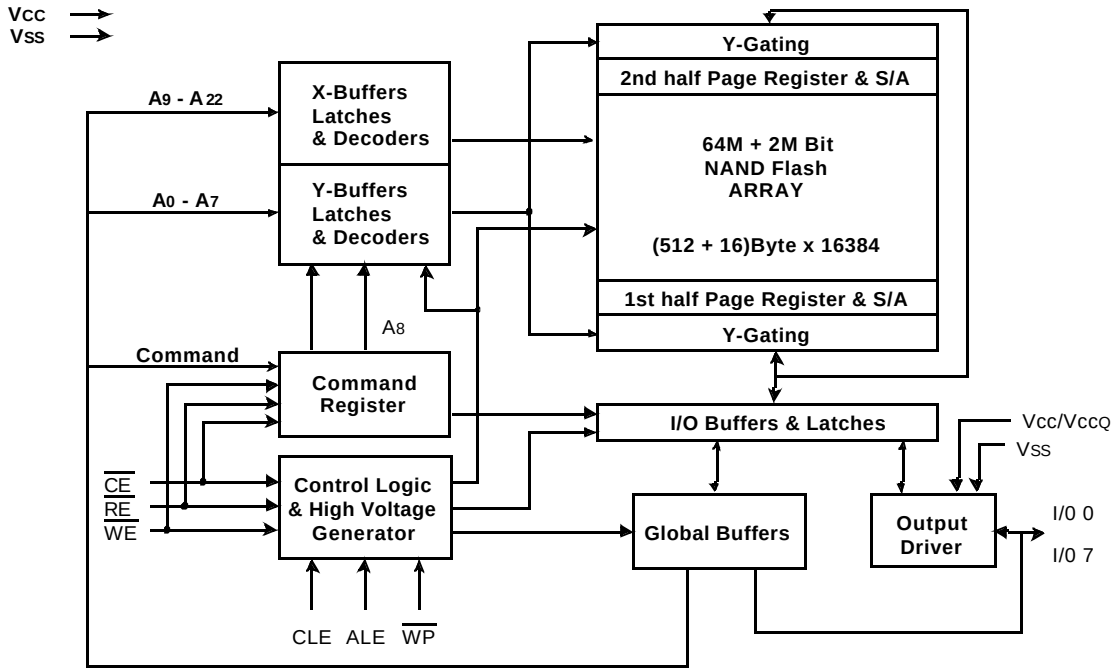
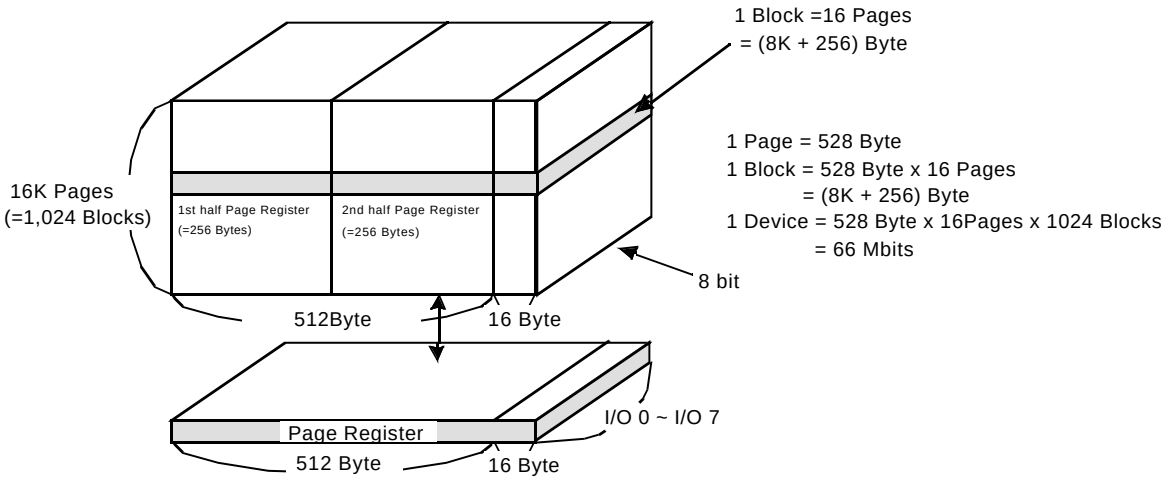


Figure 2. ARRAY ORGANIZATION



	I/O 0	I/O 1	I/O 2	I/O 3	I/O 4	I/O 5	I/O 6	I/O 7	
1st Cycle	A0	A1	A2	A3	A4	A5	A6	A7	Column Address
2nd Cycle	A9	A10	A11	A12	A13	A14	A15	A16	Row Address
3rd Cycle	A17	A18	A19	A20	A21	A22	*L	*L	(Page Address)

NOTE : Column Address : Starting Address of the Register.

00h Command(Read) : Defines the starting address of the 1st half of the register.

01h Command(Read) : Defines the starting address of the 2nd half of the register.

* A8 is set to "Low" or "High" by the 00h or 01h Command.

* L must be set to "Low".

* The device ignores any additional input of address cycles than reguired.

PRODUCT INTRODUCTION

The K9F6408X0C is a 66Mbit(69,206,016 bit) memory organized as 16,384 rows(pages) by 528 columns. Spare sixteen columns are located from column address of 512 to 527. A 528-byte data register is connected to memory cell arrays accommodating data transfer between the I/O buffers and memory during page read and page program operations. The memory array is made up of 16 cells that are serially connected to form a NAND structure. Each of the 16 cells resides in a different page. A block consists of two NAND structured strings. A NAND structure consists of 16 cells. Total 135168 NAND cells reside in a block. The array organization is shown in Figure 2. The program and read operations are executed on a page basis, while the erase operation is executed on a block basis. The memory array consists of 1024 separately erasable 8K-byte blocks. It indicates that the bit by bit erase operation is prohibited on the K9F6408X0C.

The K9F6408X0C has addresses multiplexed into 8 I/O′s. This scheme dramatically reduces pin counts and allows systems upgrades to future densities by maintaining consistency in system board design. Command, address and data are all written through I/O′s by bringing $\overline{WE}$ to low while $\overline{CE}$ is low. Data is latched on the rising edge of $\overline{WE}$. Command Latch Enable(CLE) and Address Latch Enable(ALE) are used to multiplex command and address respectively, via the I/O pins. All commands require one bus cycle except for Block Erase command which requires two cycles: one cycle for erase-setup and another for erase-execution after block address loading. The 8M byte physical space requires 23 addresses, thereby requiring three cycles for byte-level addressing: column address, low row address and high row address, in that order. Page Read and Page Program need the same three address cycles following the required command input. In Block Erase operation, however, only the two row address cycles are used.
Device operations are selected by writing specific commands into the command register. Table 1 defines the specific commands of the K9F6408X0C.

Table 1. COMMAND SETS

Function	1st. Cycle	2nd. Cycle	Acceptable Command during Busy
Read 1	00h/01h(1)	-	
Read 2	50h(2)	-	
Read ID	90h	-	
Reset	FFh	-	O
Page Program	80h	10h	
Block Erase	60h	D0h	
Read Status	70h	-	O

NOTE : 1. The 00h command defines starting address of the 1st half of registers.
The 01h command defines starting address of the 2nd half of registers.
After data access on the 2nd half of register by the 01h command, the status pointer is automatically moved to the 1st half register(00h) on the next cycle.
2. The 50h command is valid only when the GND input(pin #40) is low level.

Caution : Any undefined command inputs are prohibited except for above command set of Table 1.

ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Rating		Unit
			K9F6408Q0C(1.8V)	K9F6408U0C(3.3V)	
Voltage on any pin relative to V_{SS}		$V_{IN/OUT}$	-0.6 to + 2.45	-0.6 to + 4.6	V
		V_{CC}	-0.2 to + 2.45	-0.6 to + 4.6	V
		V_{CCQ}	-0.2 to + 2.45	-0.6 to + 4.6	V
Temperature Under Bias	K9F6408X0C-XCB0	T_{BIAS}	-10 to + 125		°C
	K9F6408X0C-XIB0		-40 to + 125		
Storage Temperature		T_{STG}	-65 to + 150		°C

NOTE :

1. Minimum DC voltage is -0.6V on input/output pins and -0.2V on Vcc and V_{CCQ} pins. During transitions, this level may undershoot to -2.0V for periods <20ns. Maximum DC voltage on input/output pins is V_{CCQ}+0.3V which, during transitions, may overshoot to V_{CC}+2.0V for periods <20ns.
2. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS

(Voltage reference to GND, K9F6408X0C-XCB0:TA=0 to 70°C, K9F6408X0C-XIB0:TA=-40 to 85°C)

Parameter	Symbol	K9F6408Q0C(1.8V)			K9F6408U0C(3.3V)			Unit
		Min	Typ.	Max	Min	Typ.	Max	
Supply Voltage	V_{CC}	1.70	1.8	1.95	2.7	3.3	3.6	V
Supply Voltage	V_{CCQ}	1.70	1.8	1.95	2.7	3.3	3.6	V
Supply Voltage	V_{SS}	0	0	0	0	0	0	V

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions otherwise noted.)

Parameter		Symbol	Test Conditions	K9F6408Q0C(1.8V)			K9F6408U0C(3.3V)			Unit
				Min	Typ	Max	Min	Typ	Max	
Operating Current	Sequential Read	I_{CC1}	$\overline{CE}$=V_{IL}, I_{OUT}=0mA tRC=50ns	-	5	10	-	10	20	mA
	Program	I_{CC2}	-	-	8	15	-	10	20	
	Erase	I_{CC3}	-	-	8	15	-	10	20	
Stand-by Current(TTL)		I_{SB1}	$\overline{CE}$=V_{IH}, $\overline{WP}$=0V/Vcc	-	-	1	-	-	1	
Stand-by Current(CMOS)		I_{SB2}	$\overline{CE}$=Vcc-0.2, $\overline{WP}$=0V/Vcc	-	10	50	-	10	50	µA
Input Leakage Current		I_{LI}	V_{IN}=0 to Vcc(max)	-	-	±10	-	-	±10	
Output Leakage Current		I_{LO}	V_{OUT}=0 to Vcc(max)	-	-	±10	-	-	±10	
Input High Voltage		V_{IH}*	I/O pins	V_{CCQ}-0.4		V_{CCQ} +0.3	2.0	-	V_{CCQ}+0.3	V
			Except I/O pins	V_{CC}-0.4	-	VCC +0.3	2.0	-	V_{CC}+0.3	
Input Low Voltage, All inputs		V_{IL}*	-	-0.3	-	0.4	-0.3	-	0.8	
Output High Voltage Level		V_{OH}	K9F6408Q0C :I_{OH}=-100µA K9F6408U0C :I_{OH}=-400µA	V_{CCQ}-0.1	-	-	2.4	-	-	
Output Low Voltage Level		V_{OL}	K9F6408Q0C :I_{OL}=100uA K9F6408U0C :I_{OL}=2.1mA	-	-	0.1	-	-	0.4	
Output Low Current(R/$\overline{B}$)		I_{OL}(R/$\overline{B}$)	K9F6408Q0C :V_{OL}=0.1V K9F6408U0C :V_{OL}=0.4V	3	4	-	8	10	-	mA

NOTE : V_{IL} can undershoot to -0.4V and V_{IH} can overshoot to V_{CC} +0.4V for durations of 20 ns or less.

VALID BLOCK

Parameter	Symbol	Min	Typ.	Max	Unit
Valid Block Number	N_{VB}	1014	1020	1024	Blocks

NOTE :

1. The device may include invalid blocks when first shipped. Additional invalid blocks may develop while being used. The number of valid blocks is presented with both cases of invalid blocks considered. Invalid blocks are defined as blocks that contain one or more bad bits. Do not erase or program factory-marked bad blocks. Refer to the attached technical notes for a appropriate management of invalid blocks.
2. The 1st block, which is placed on 00h block address, is guaranteed to be a valid block, does not require Error Correction up to 1K program/erase cycles.

AC TEST CONDITION

(K9F6408X0C-XCB0:TA=0 to 70°C, K9F6408X0C-XIB0:TA=-40 to 85°C

K9F6408Q0C: Vcc=1.70V~1.95V , K9F6408U0C: Vcc=2.7V~3.6V unless otherwise noted)

Parameter	K9F6408Q0C	K9F6408U0C
Input Pulse Levels	0V to V_{CCQ}	0.4V to 2.4V
Input Rise and Fall Times	5ns	5ns
Input and Output Timing Levels	V_{CCQ}/2	1.5V
K9F6408Q0C:Output Load (V_{CCQ}:1.8V +/-10%) K9F6408U0C:Output Load (V_{CCQ}:3.0V +/-10%)	1 TTL GATE and CL=30pF	1 TTL GATE and CL=50pF
K9F6408U0C:Output Load (V_{CCQ}:3.3V +/-10%)	-	1 TTL GATE and CL=100pF

CAPACITANCE(T_A=25°C, V_{CC}=1.8V/3.3V, f=1.0MHz)

Item	Symbol	Test Condition	Min	Max	Unit
Input/Output Capacitance	$C_{I/O}$	V_{IL}=0V	-	10	pF
Input Capacitance	C_{IN}	V_{IN}=0V	-	10	pF

NOTE : Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

CLE	ALE	$\overline{CE}$	$\overline{WE}$	$\overline{RE}$	$\overline{WP}$	Mode	
H	L	L	⎍	H	X	Read Mode	Command Input
L	H	L	⎍	H	X		Address Input(3clock)
H	L	L	⎍	H	H	Write Mode	Command Input
L	H	L	⎍	H	H		Address Input(3clock)
L	L	L	⎍	H	H	Data Input	
L	L	L	H	⎍	X	Data Output	
L	L	L	H	H	X	During Read(Busy) on K9F6408U0C_T,Q or K9F6408U0C_V,F	
X	X	X	X	H	X	During Read(Busy) on the devices except K9F6408U0C_T,Q and K9F6408U0C_V,F	
X	X	X	X	X	H	During Program(Busy)	
X	X	X	X	X	H	During Erase(Busy)	
X	X(1)	X	X	X	L	Write Protect	
X	X	H	X	X	0V/V_{CC}(2)	Stand-by	

NOTE : 1. X can be V_{IL} or V_{IH}.
2. $\overline{WP}$ should be biased to CMOS high or CMOS low for standby.

Program/Erase Characteristics

Parameter		Symbol	Min	Typ	Max	Unit
Program Time		t_{PROG}	-	200	500	µs
Number of Partial Program Cycles in the Same Page	Main Array	Nop	-	-	2	cycles
	Spare Array		-	-	3	cycles
Block Erase Time		t_{BERS}	-	2	3	ms

AC Timing Characteristics for Command / Address / Data Input

Parameter	Symbol	K9F6408Q0C		K9F6408U0C		Unit
		Min	Max	Min	Max	
CLE Set-up Time	t_{CLS}	0	-	0	-	ns
CLE Hold Time	t_{CLH}	10	-	10	-	ns
$\overline{CE}$ Setup Time	t_{CS}	0	-	0	-	ns
$\overline{CE}$ Hold Time	t_{CH}	10	-	10	-	ns
$\overline{WE}$ Pulse Width	t_{WP}	25(1)	-	25(1)	-	ns
ALE Setup Time	t_{ALS}	0	-	0	-	ns
ALE Hold Time	t_{ALH}	10	-	10	-	ns
Data Setup Time	t_{DS}	20	-	20	-	ns
Data Hold Time	t_{DH}	10	-	10	-	ns
Write Cycle Time	t_{WC}	50	-	50	-	ns
$\overline{WE}$ High Hold Time	t_{WH}	15	-	15	-	ns

NOTE : 1. If tCS is set less than 10ns, tWP must be minimum 35ns, otherwise, tWP may be minimum 25ns.

AC Characteristics for Operation

Parameter		Symbol	K9F6408Q0C		K9F6408U0C		Unit
			Min	Max	Min	Max	
Data Transfer from Cell to Register		t_R	-	10	-	10	µs
ALE to $\overline{RE}$ Delay(ID read)		t_{AR1}	20	-	20	-	ns
ALE to $\overline{RE}$ Delay(Read cycle)		t_{AR2}	50	-	50	-	ns
CLE to $\overline{RE}$ Delay		t_{CLR}	50	-	50	-	ns
Ready to $\overline{RE}$ Low		t_{RR}	20	-	20	-	ns
$\overline{RE}$ Pulse Width		t_{RP}	25	-	25	-	ns
$\overline{WE}$ High to Busy		t_{WB}	-	100	-	100	ns
Read Cycle Time		t_{RC}	50	-	50	-	ns
$\overline{CE}$ Access Time		t_{CEA}	-	45	-	45	ns
$\overline{RE}$ Access Time		t_{REA}	-	35	-	35	ns
$\overline{RE}$ High to Output Hi-Z		t_{RHZ}	-	30	-	30	ns
$\overline{CE}$ High to Output Hi-Z		t_{CHZ}	-	20	-	20	ns
$\overline{RE}$ or $\overline{CE}$ High to Output hold		t_{OH}	15	-	15	-	ns
$\overline{RE}$ High Hold Time		t_{REH}	15	-	15	-	ns
Output Hi-Z to $\overline{RE}$ Low		t_{IR}	0	-	0	-	ns
$\overline{WE}$ High to $\overline{RE}$ Low		t_{WHR}	60	-	60	-	ns
Device Resetting Time(Read/Program/Erase)		t_{RST}	-	5/10/500(1)	-	5/10/500(1)	µs
K9F6408U0C-T,Q,V,F only	Last RE High to Busy (at sequential read)	t_{RB}	-	100	-	100	ns
	$\overline{CE}$ High to Ready(in case of interception by $\overline{CE}$ at read)	t_{CRY}	-	50 +tr(R/$\overline{B}$)(3)	-	50 +tr(R/$\overline{B}$)(3)	ns
	$\overline{CE}$ High Hold Time(at the last serial read)(2)	t_{CEH}	100	-	100	-	ns

NOTE : 1. If reset command(FFh) is written at Ready state, the device goes into Busy for maximum 5us.
2. To break the sequential read cycle, $\overline{CE}$ must be held high for longer time than tCEH.
3. The time to Ready depends on the value of the pull-up resistor tied R/$\overline{B}$ pin.

NAND Flash Technical Notes

Invalid Block(s)

Invalid blocks are defined as blocks that contain one or more invalid bits whose reliability is not guaranteed by Samsung. The information regarding the invalid block(s) is so called as the invalid block information. Devices with invalid block(s) have the same quality level or as devices with all valid blocks and have the same AC and DC characteristics. An invalid block(s) does not affect the performance of valid block(s) because it is isolated from the bit line and the common source line by a select transistor. The system design must be able to mask out the invalid block(s) via address mapping. The 1st block of the NAND Flash, however, is guaranteed to be a valid block up to 1K program/erase cycles.

Identifying Invalid Block(s)

All device locations are erased(FFh) except locations where the invalid block(s) information is written prior to shipping. The invalid block(s) status is defined by the 6th byte in the spare area. Samsung makes sure that either the 1st or 2nd page of every invalid block has non-FFh data at the column address of 517. Since the invalid block information is also erasable in most cases, it is impossible to recover the information once it has been erased. Therefore, the system must be able to recognize the invalid block(s) based on the original invalid block information and create the invalid block table via the following suggested flow chart(Figure 1). Any intentional erasure of the original invalid block information is prohibited.

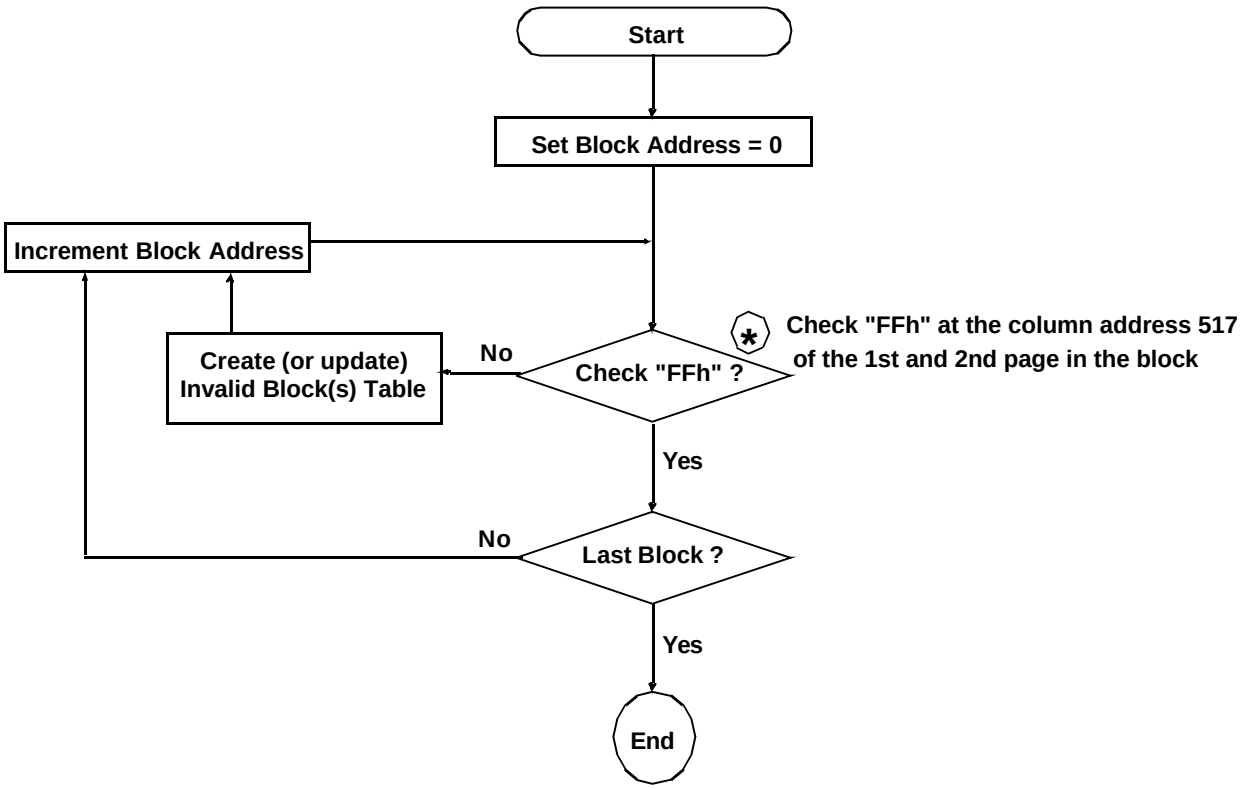


Figure 1. Flow chart to create invalid block table.

NAND Flash Technical Notes *(Continued)*

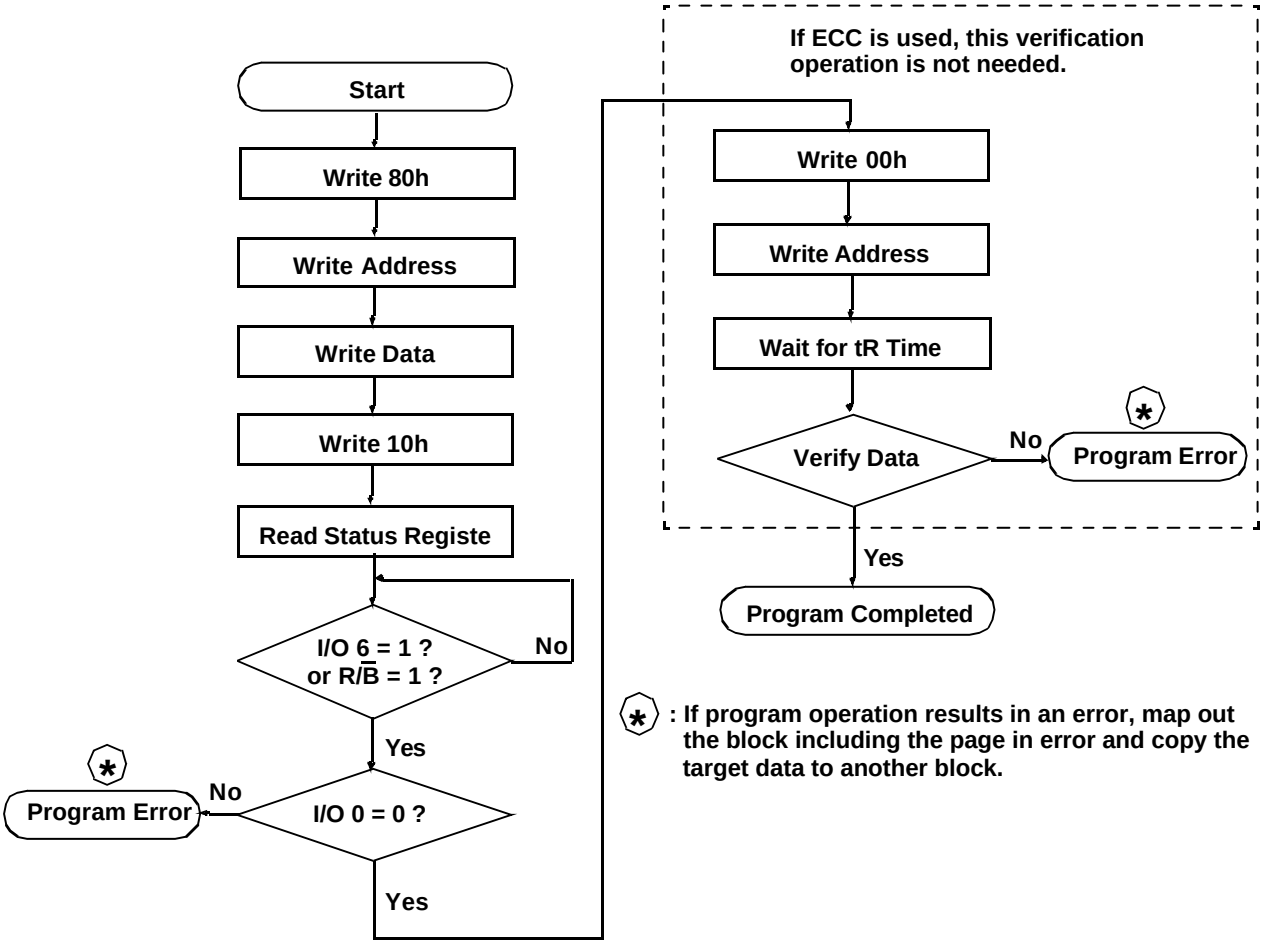
Error in write or read operation

Within its life time, the additional invalid blocks may develop with NAND Flash memory. Refer to the qualification report for the actual data.The following possible failure modes should be considered to implement a highly reliable system. In the case of status read failure after erase or program, block replacement should be done. To improve the efficiency of memory space, it is recommended that the read or verification failure due to single bit error be reclaimed by ECC without any block replacement. The said additional block failure rate does not include those reclaimed blocks.

Failure Mode		Detection and Countermeasure sequence
Write	Erase Failure	Status Read after Erase --> Block Replacement
	Program Failure	Status Read after Program --> Block Replacement Read back (Verify after Program) --> Block Replacement or ECC Correction
Read	Single Bit Failure	Verify ECC -> ECC Correction

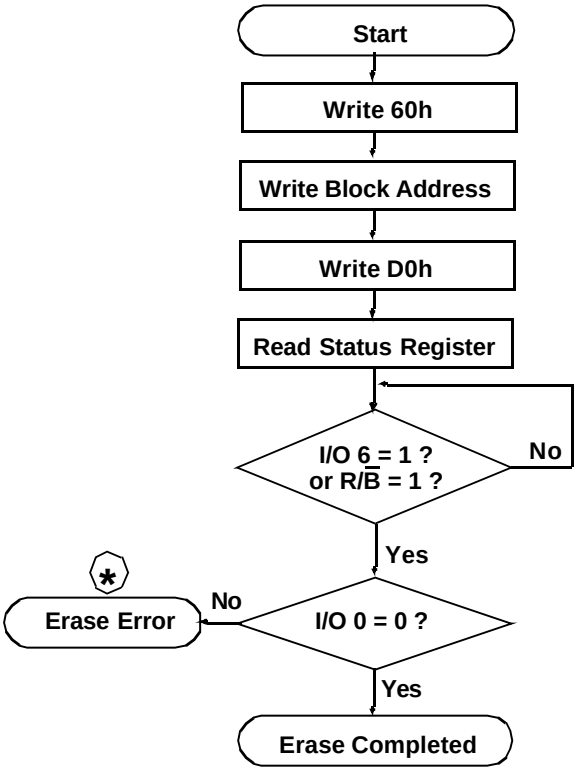
ECC : Error Correcting Code --> Hamming Code etc.
Example) 1bit correction & 2bit detection

Program Flow Chart

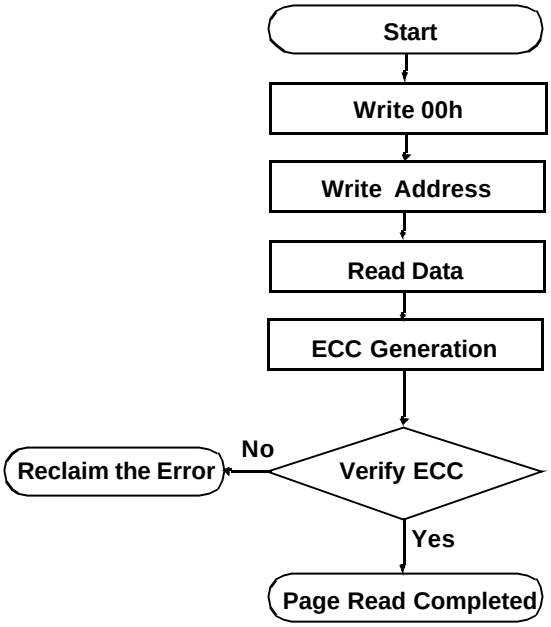


NAND Flash Technical Notes *(Continued)*

Erase Flow Chart

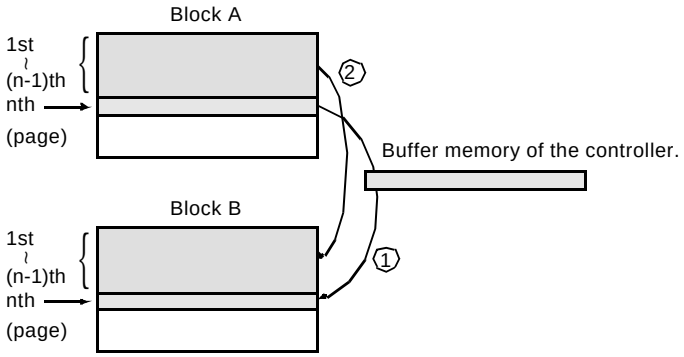


Read Flow Chart



(*) : If erase operation results in an error, map out the failing block and replace it with another block.

Block Replacement



* Step1
When an error happens in the nth page of the Block ' A' during erase or program operation.
* Step2
Copy the nth page data of the Block ' A' in the buffer memory to the nth page of another free block. (Block ' B')
* Step3
Then, Copy the 1st ~ (n-1)th data to the same location of the Block ' B' .
* Step4
Do not further erase Block ' A' by creating a ' invalid Block' table or other appropriate scheme.

Pointer Operation of K9F6408U0C

Samsung NAND Flash has three address pointer commands as a substitute for the two most significant column addresses. ' 00h' command sets the pointer to ' A' area(0~255byte), ' 01h' command sets the pointer to ' B' area(256~511byte), and ' 50h' command sets the pointer to ' C' area(512~527byte). With these commands, the starting column address can be set to any of a whole page(0~527byte). ' 00h' or ' 50h' is sustained until another address pointer command is inputted. ' 01h' command, however, is effective only for one operation. After any operation of Read, Program, Erase, Reset, Power_Up is executed once with ' 01h' command, the address pointer returns to ' A' area by itself. To program data starting from ' A' or ' C' area, ' 00h' or ' 50h' command must be inputted before ' 80h' command is written. A complete read operation prior to ' 80h' command is not necessary. To program data starting from ' B' area, ' 01h' command must be inputted right before ' 80h' command is written.

Table 1. Destination of the pointer

Command	Pointer position	Area
00h	0 ~ 255 byte	1st half array(A)
01h	256 ~ 511 byte	2nd half array(B)
50h	512 ~ 527 byte	spare array(C)

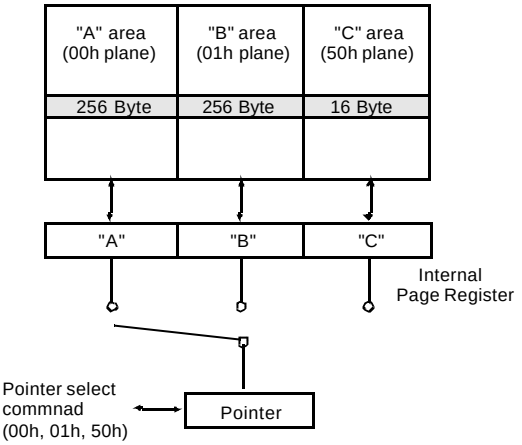
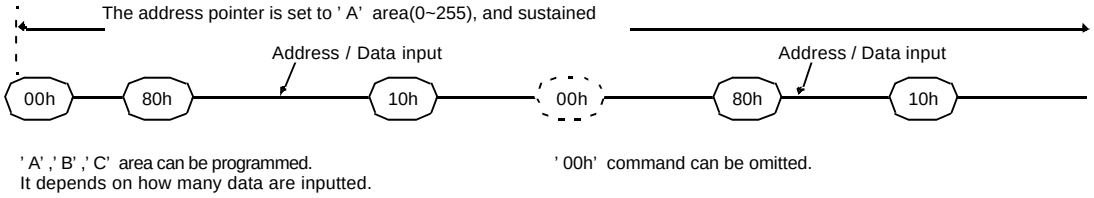


Figure 2. Block Diagram of Pointer Operation

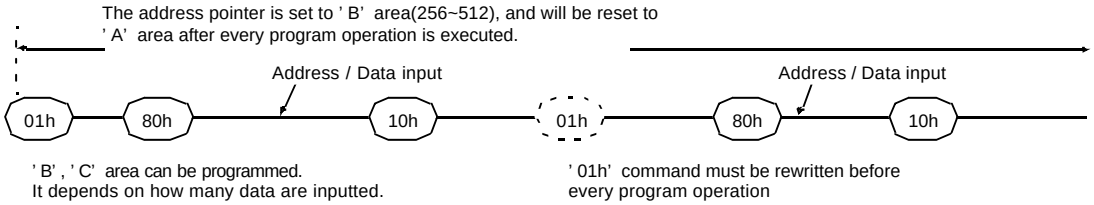
(1) Command input sequence for programming ' A' area



' A' ,' B' ,' C' area can be programmed.
It depends on how many data are inputted.

' 00h' command can be omitted.

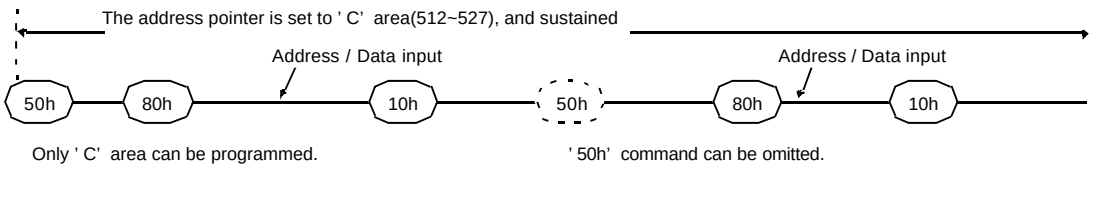
(2) Command input sequence for programming ' B' area



' B' , ' C' area can be programmed.
It depends on how many data are inputted.

' 01h' command must be rewritten before every program operation

(3) Command input sequence for programming ' C' area



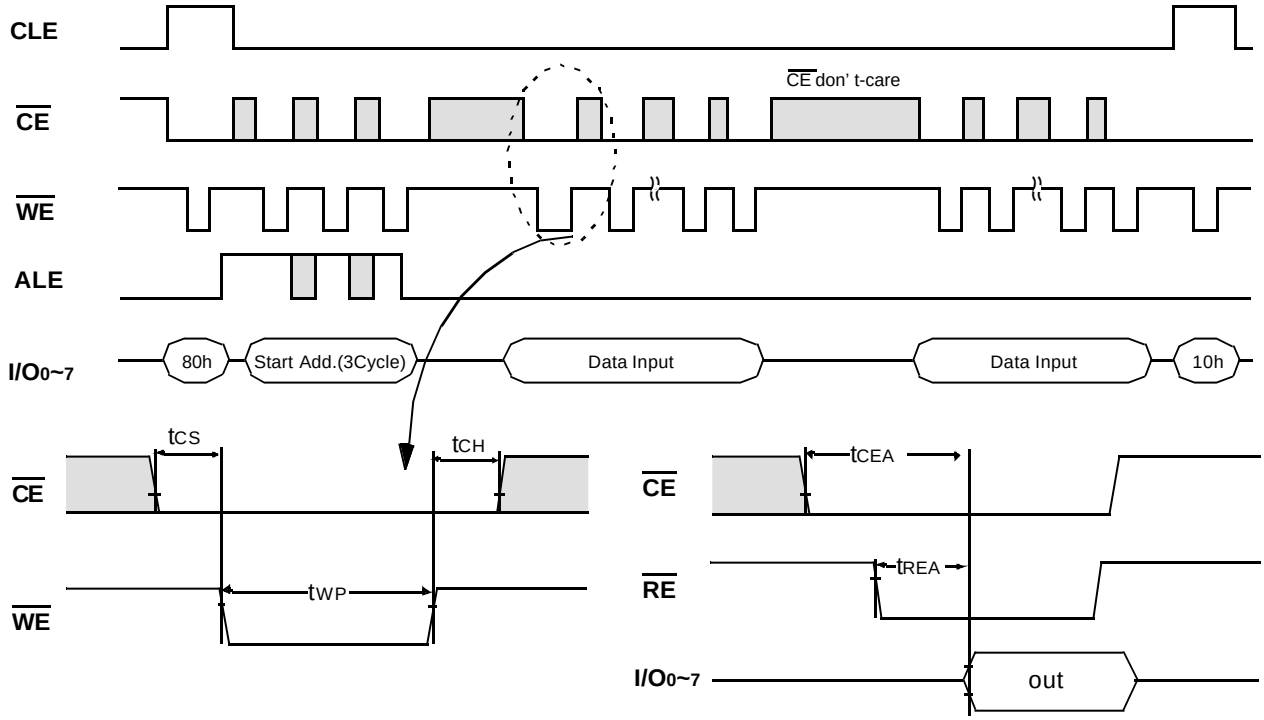
Only ' C' area can be programmed.

' 50h' command can be omitted.

System Interface Using $\overline{CE}$ don' t-care.

For an easier system interface, $\overline{CE}$ may be inactive during the data-loading or sequential data-reading as shown below. The internal 528byte page registers are utilized as seperate buffers for this operation and the system design gets more flexible. In addition, for voice or audio applications which use slow cycle time on the order of u-seconds, de-activating $\overline{CE}$ during the data-loading and reading would provide significant savings in power consumption.

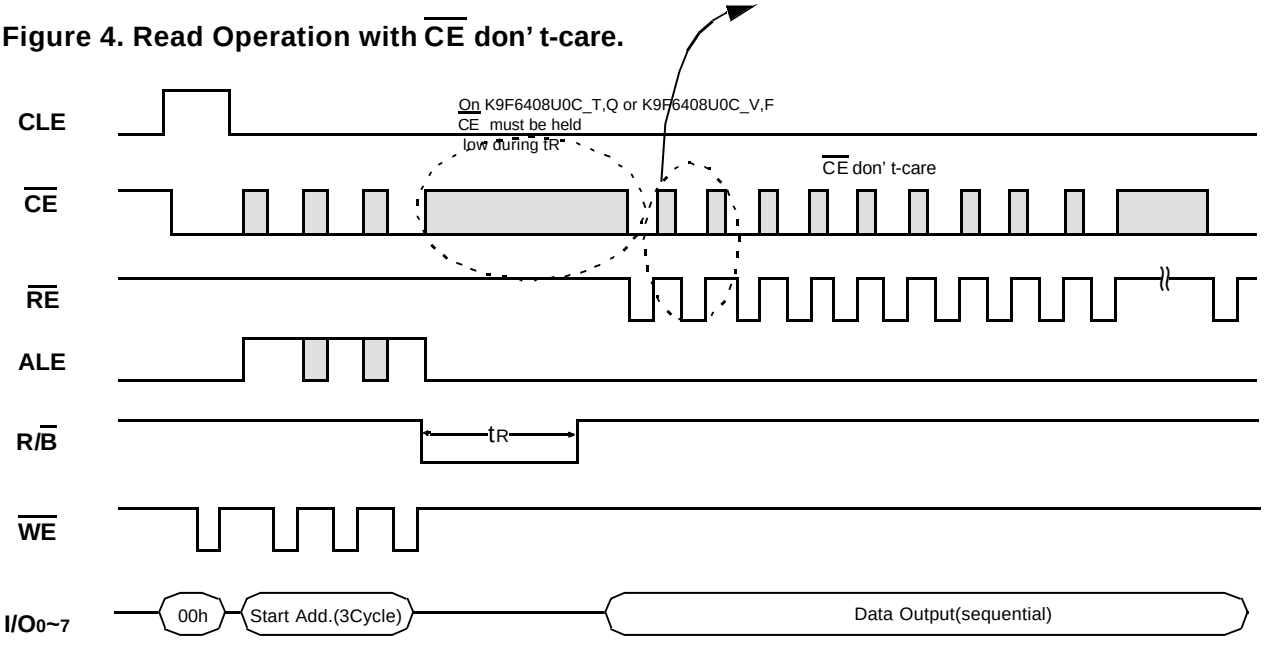
Figure 3. Program Operation with $\overline{CE}$ don' t-care.



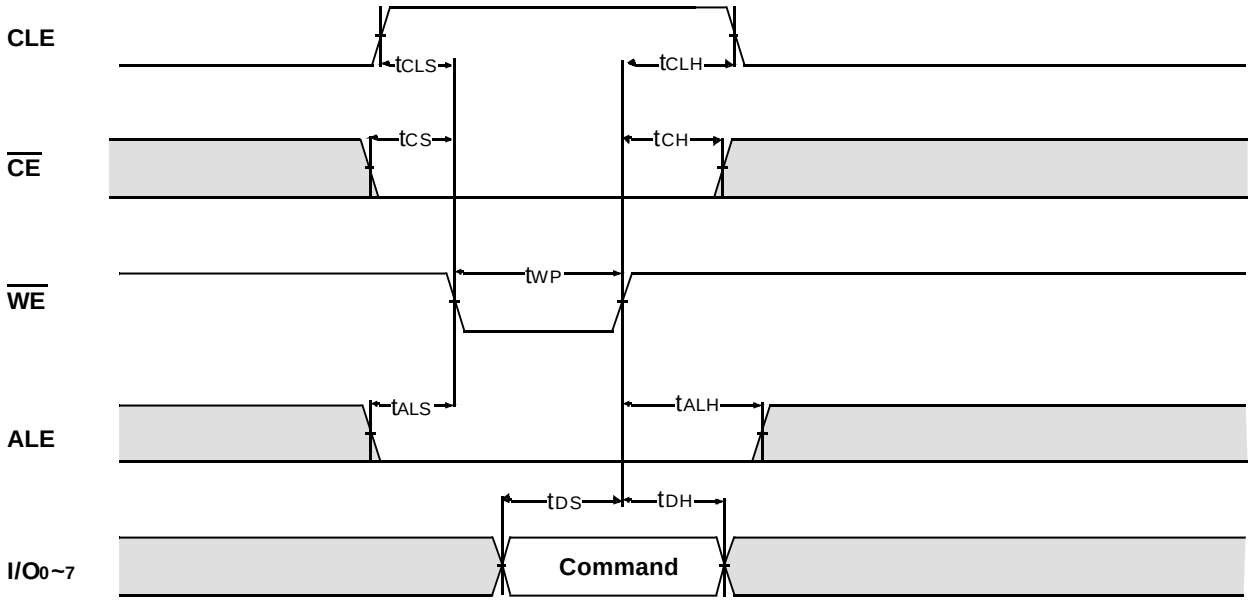
Timing requirements : If $\overline{CE}$ is is exerted high during data-loading, tCS must be minimum 10ns and tWC must be increased accordingly.

Timing requirements : If $\overline{CE}$ is exerted high during sequential data-reading, the falling edge of $\overline{CE}$ to valid data(tCEA) must be kept greater than 45ns.

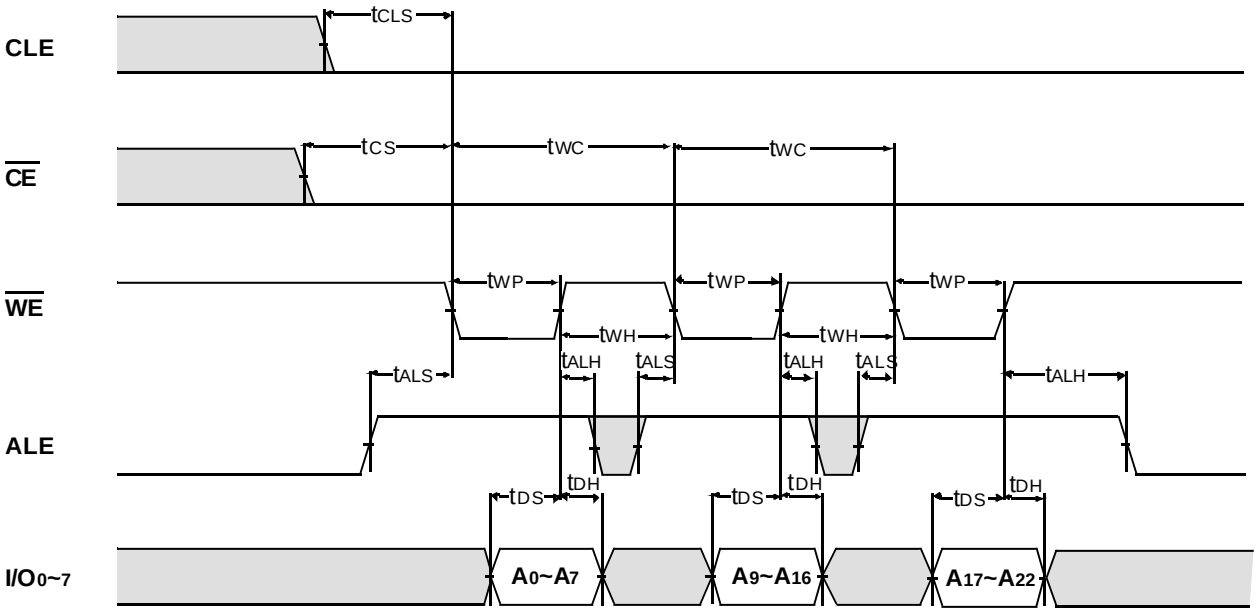
Figure 4. Read Operation with $\overline{CE}$ don' t-care.



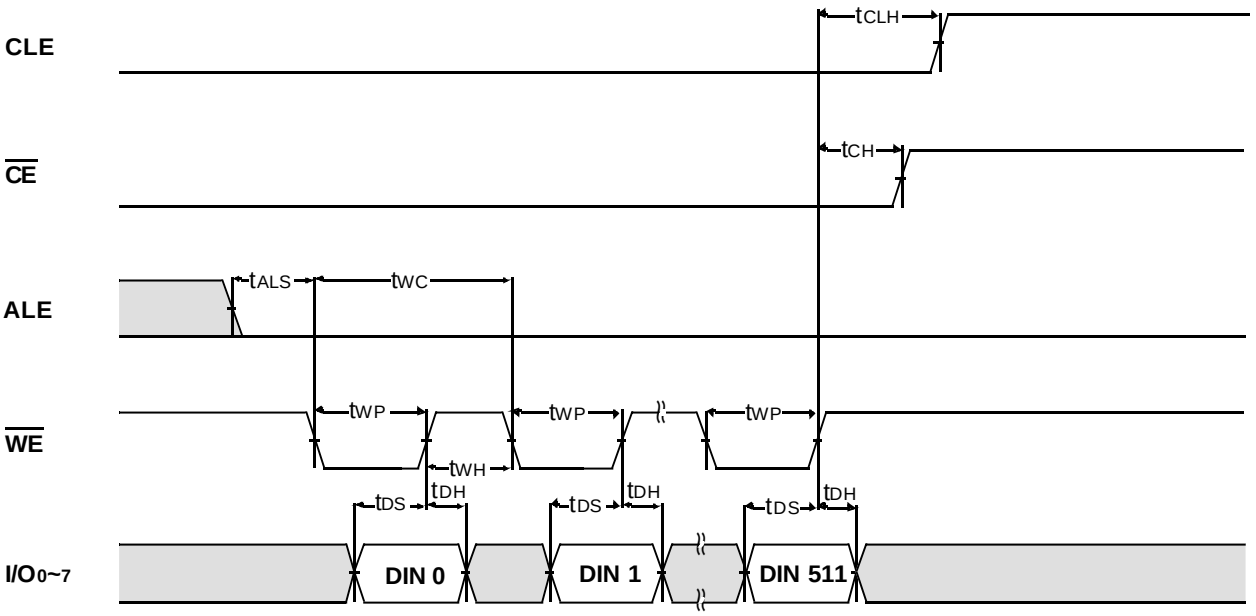
Command Latch Cycle



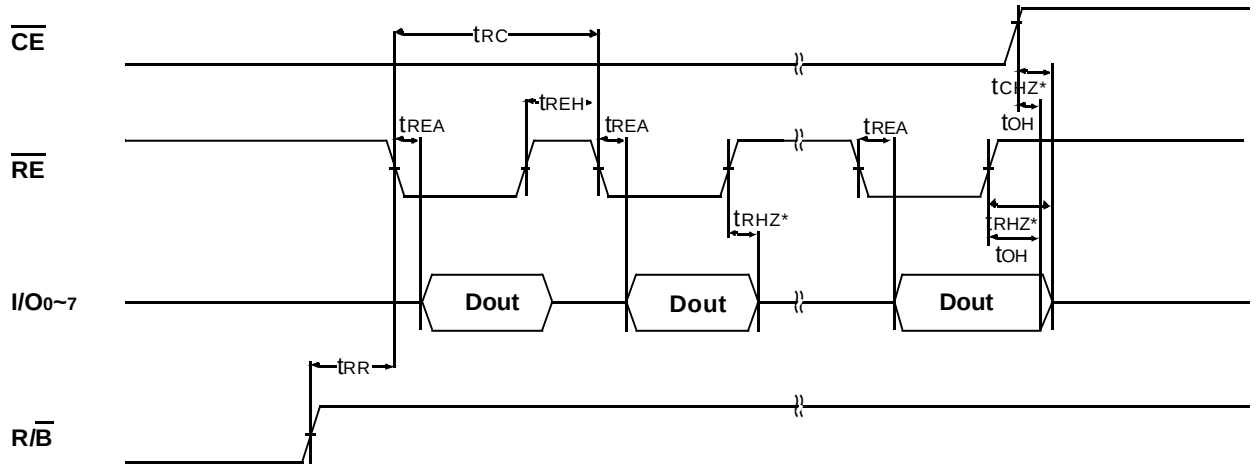
Address Latch Cycle



Input Data Latch Cycle

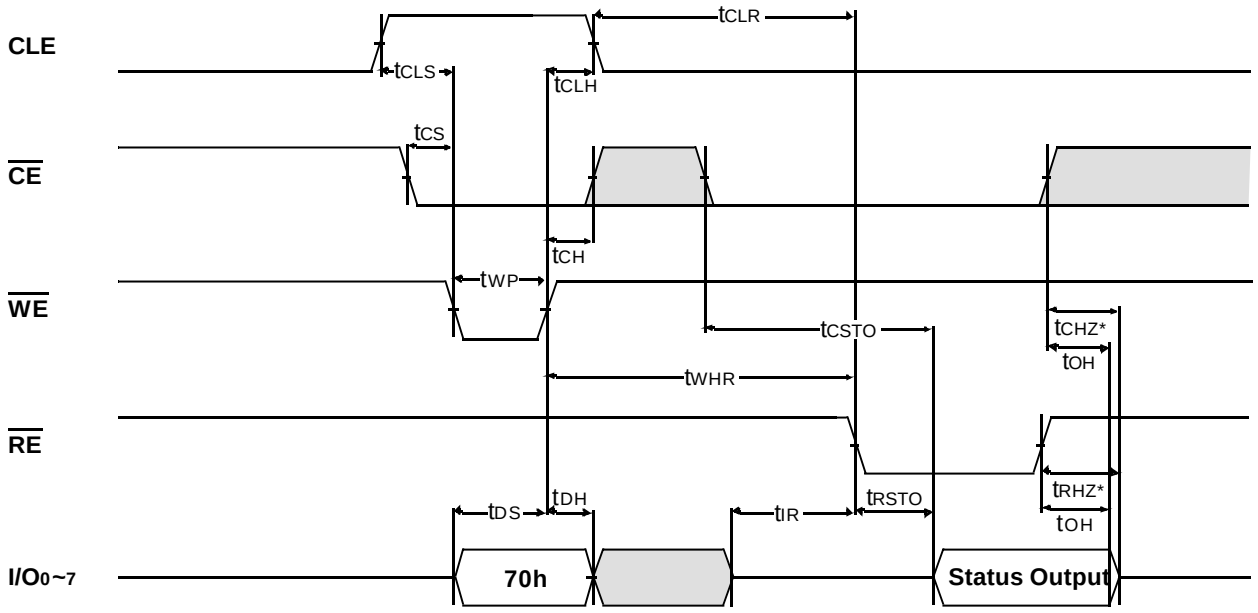


Serial access Cycle after Read (CLE=L, $\overline{WE}$=H, ALE=L)

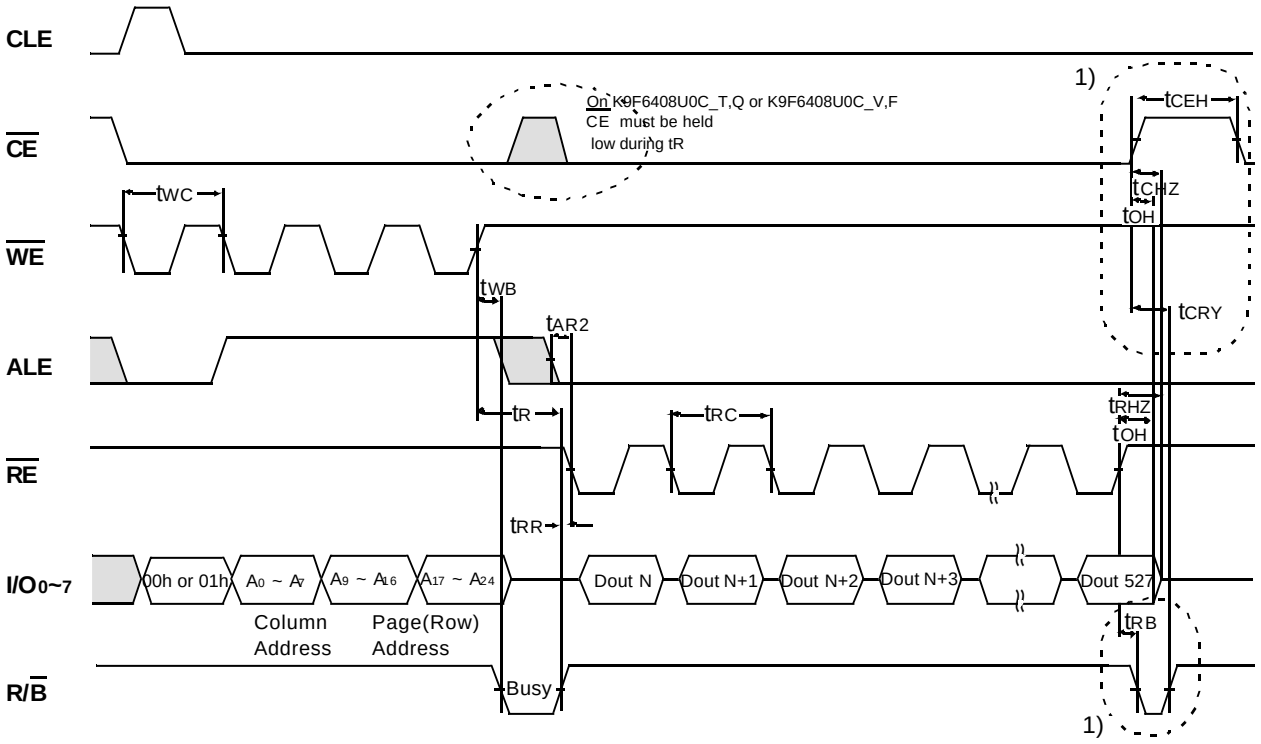


NOTES : Transition is measured ±200mV from steady state voltage with load.
This parameter is sampled and not 100% tested.

Status Read Cycle

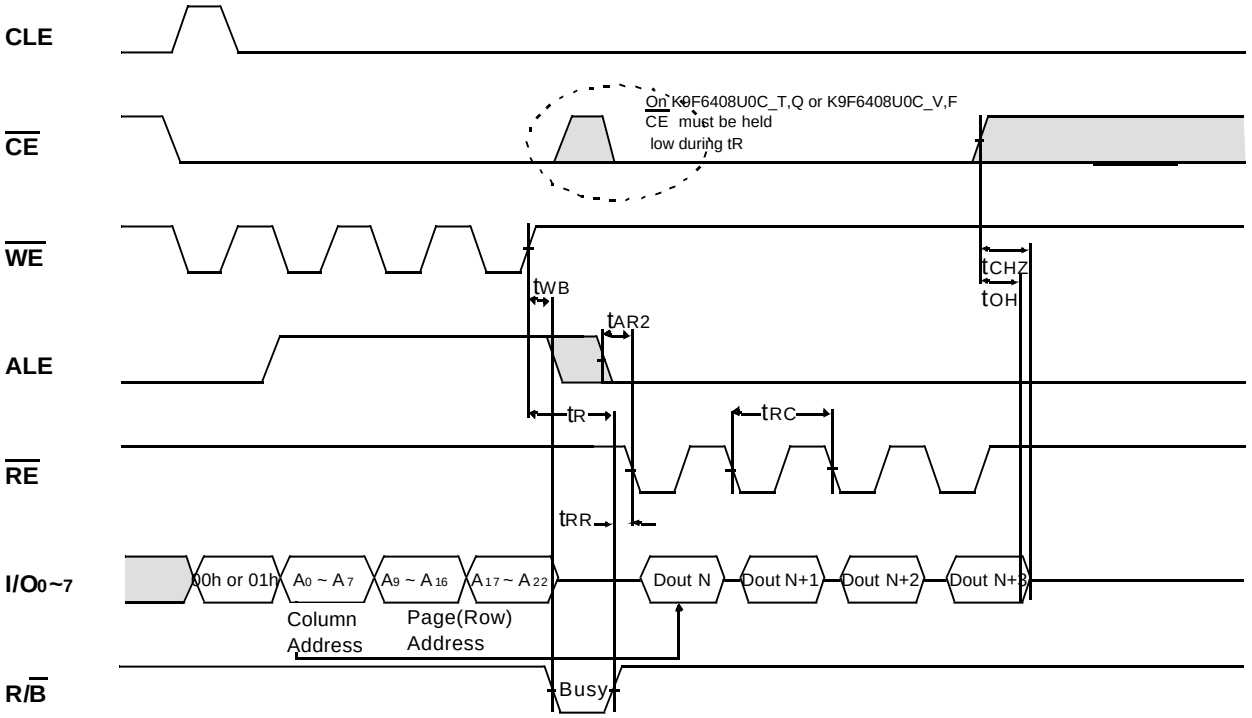


READ1 OPERATION (READ ONE PAGE)

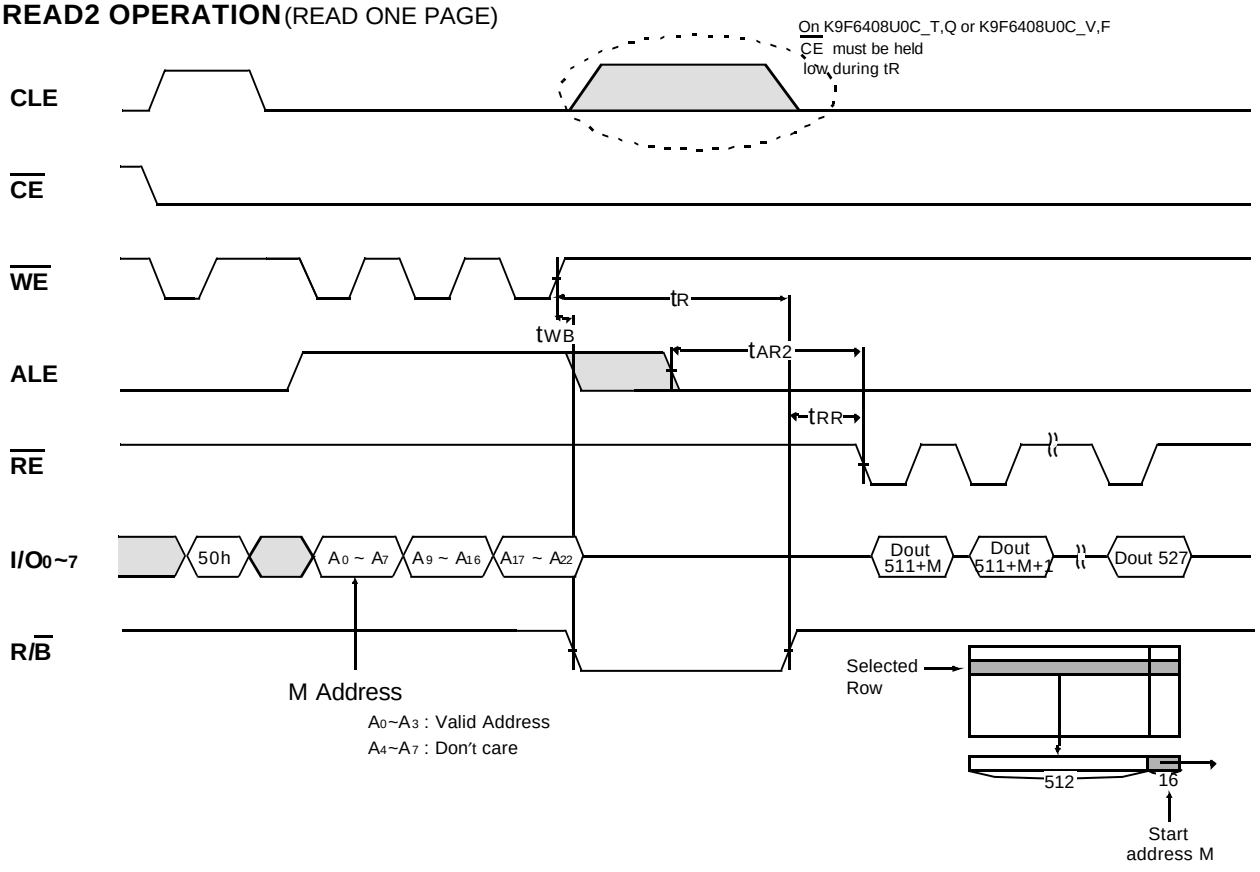


NOTES : 1) is only valid on K9F6408U0C_T,Q or K9F6408U0C_V,F

READ1 OPERATION (INTERCEPTED BY $\overline{CE}$)

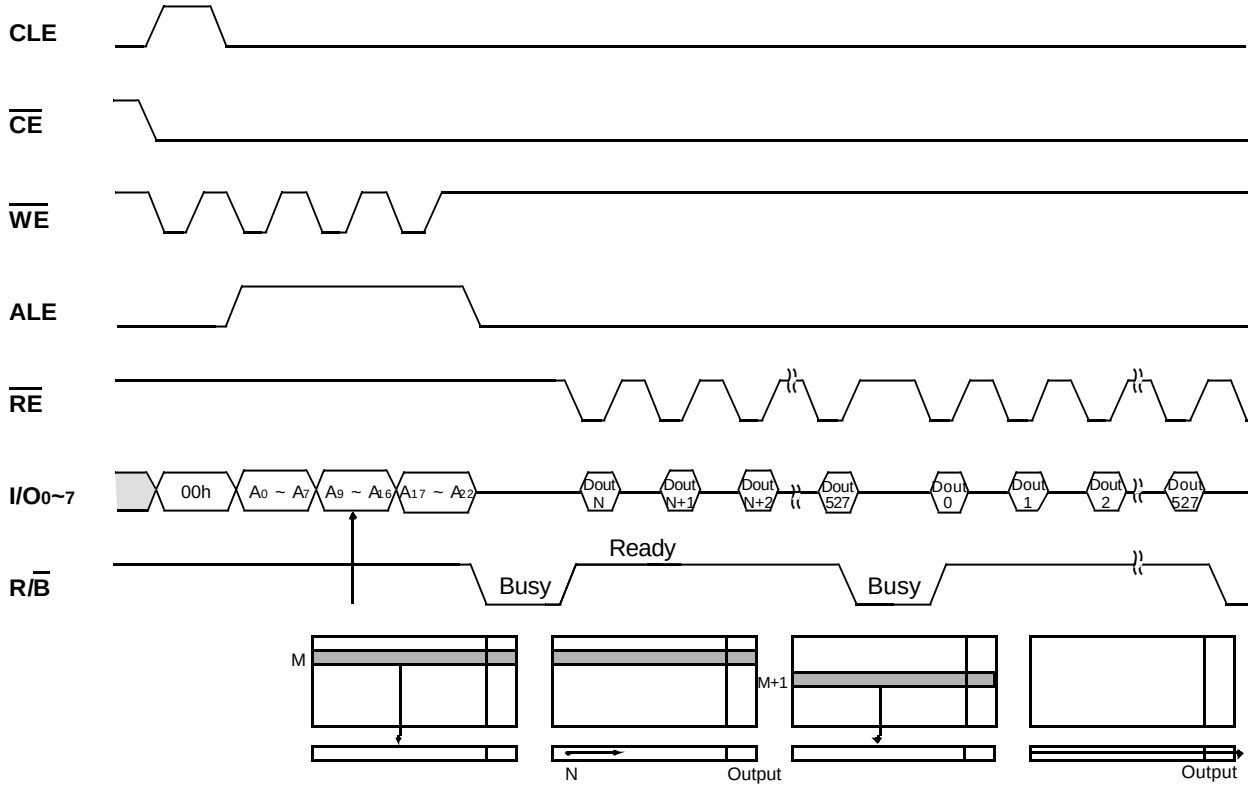


READ2 OPERATION (READ ONE PAGE)

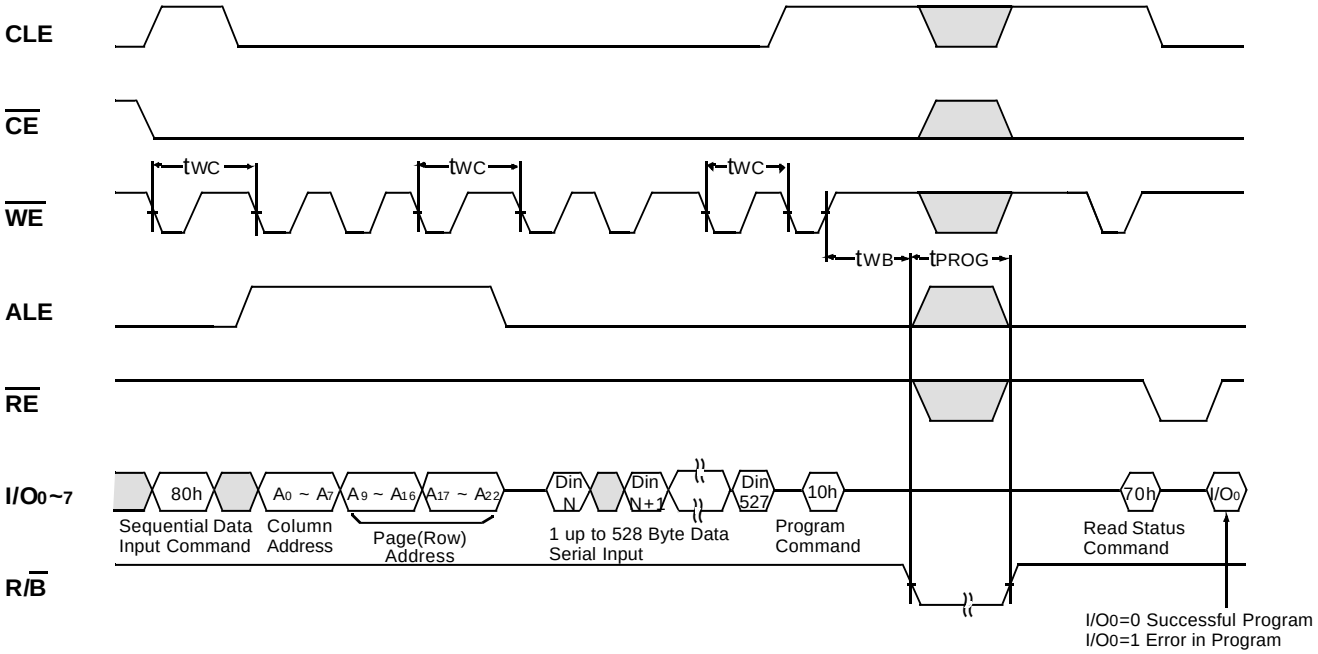


SEQUENTIAL ROW READ OPERATION

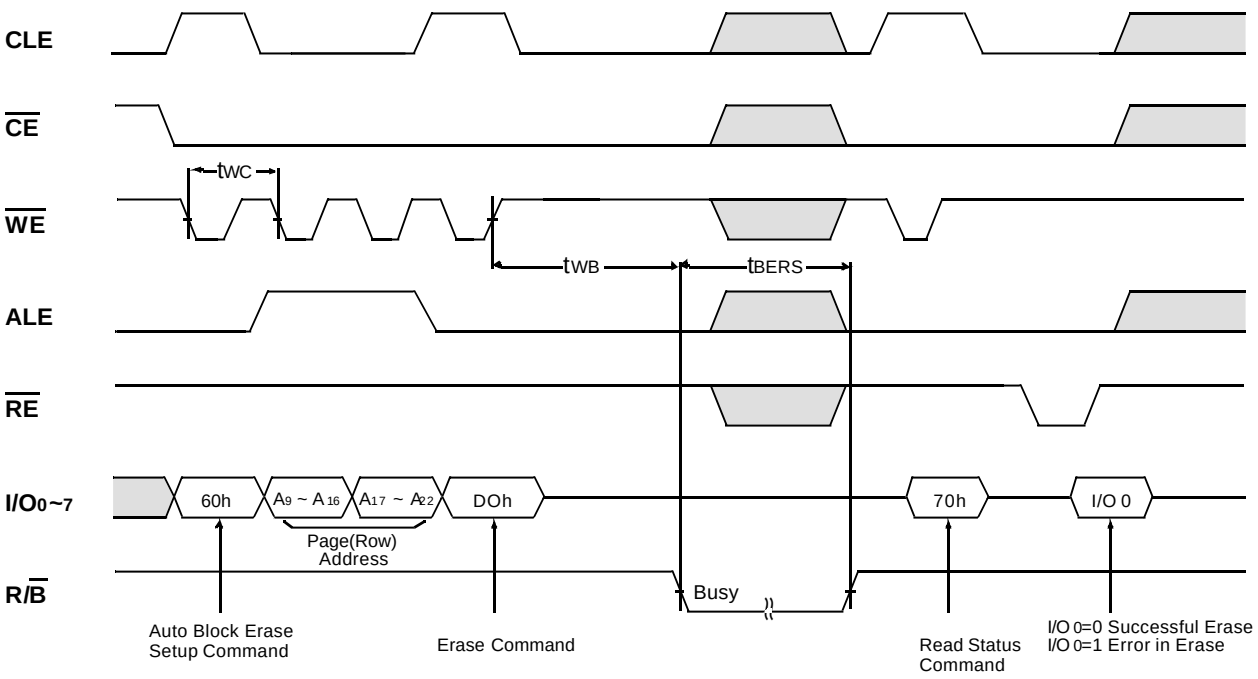
(only for K9F6408U0C-T,Q and K9F6408U0C-V,F valid within a block)



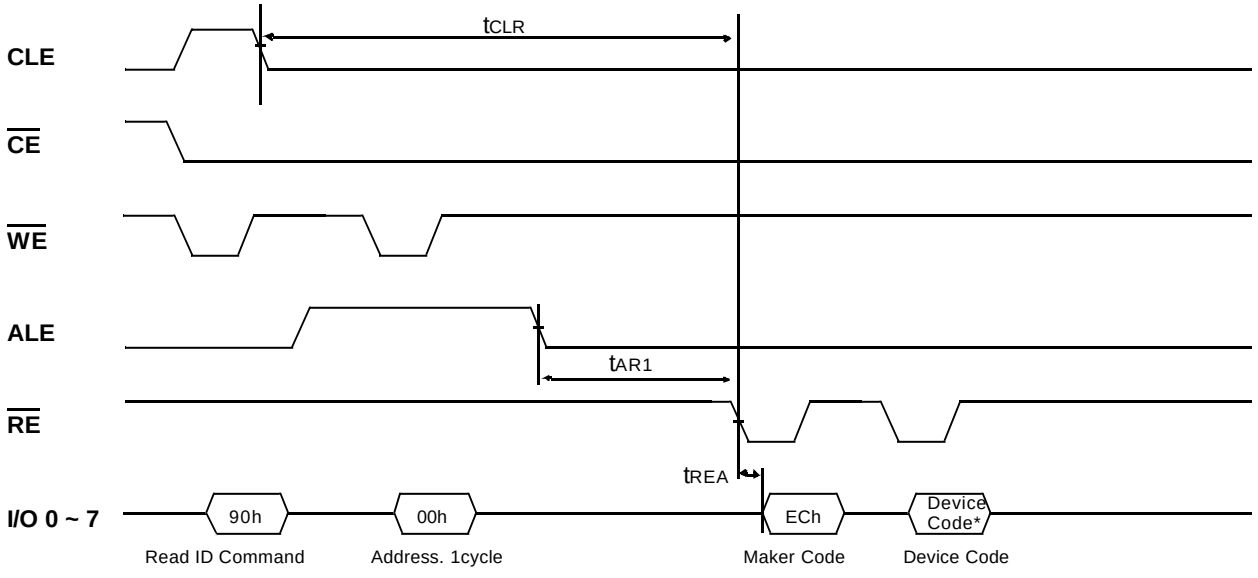
PAGE PROGRAM OPERATION



BLOCK ERASE OPERATION (ERASE ONE BLOCK)



MANUFACTURE & DEVICE ID READ OPERATION



Device	Device Code*
K9F6408Q0C	39h
K9F6408U0C	E6h

DEVICE OPERATION

PAGE READ

Upon initial device power up, the device defaults to Read1 mode. This operation is also initiated by writing 00h to the command register along with three address cycles. Once the command is latched, it does not need to be written for the following page read operation. Three types of operations are available : random read, serial page read and sequential row read.

The random read mode is enabled when the page address is changed. The 528 bytes of data within the selected page are transferred to the data registers in less than 10μs(tR). The CPU can detect the completion of this data transfer(tR) by analyzing the output of R/$\overline{B}$ pin. Once the data in a page is loaded into the registers, they may be read out in 50ns cycle time by sequentially pulsing $\overline{RE}$. High to low transitions of the $\overline{RE}$ clock output the data stating from the selected column address up to the last column address(column 511 or 527 depending on the state of GND input pin).

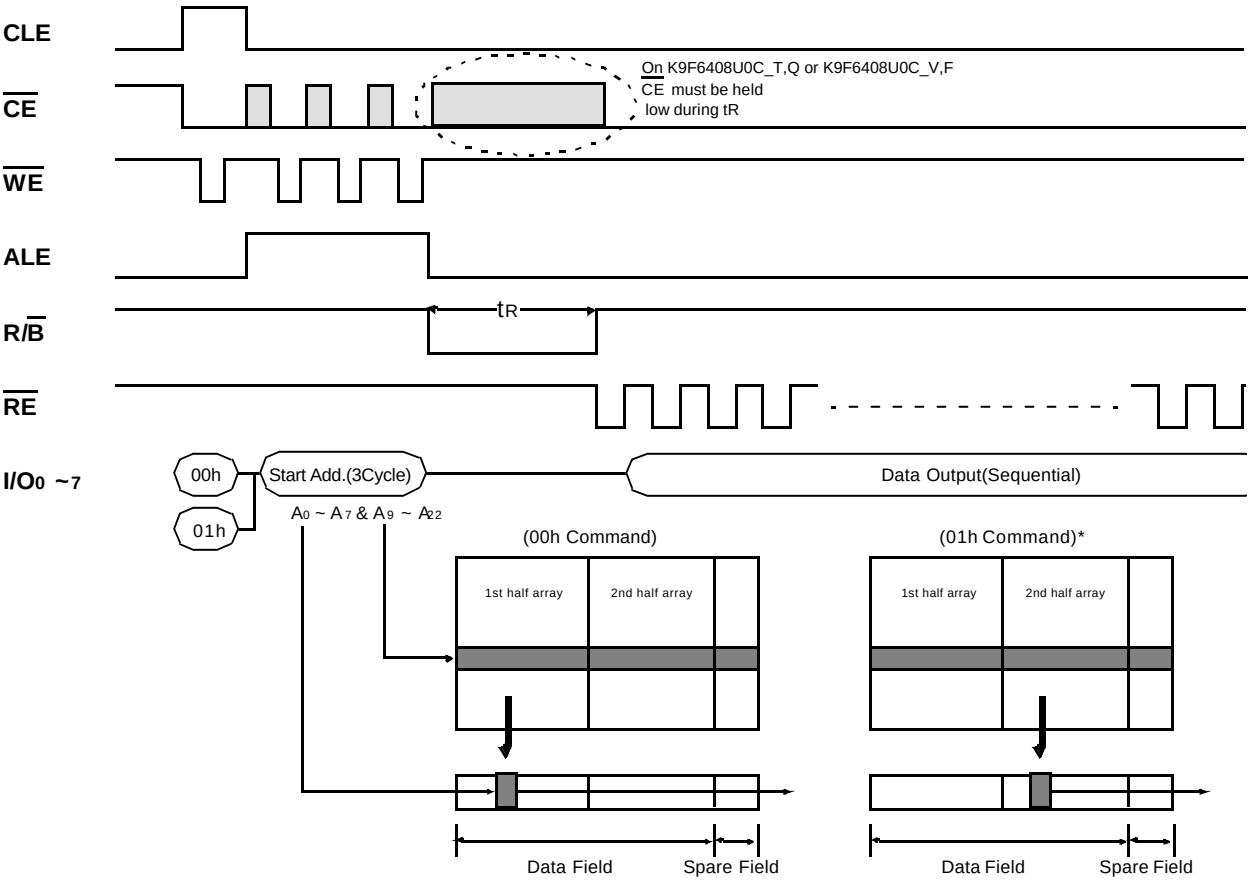
After the data of last column address is clocked out, the next page is automatically selected for sequential row read.

Waiting 10μs again allows reading the selected page.The sequential row read operation is terminated by bringing $\overline{CE}$ high. The way the Read1 and Read2 commands work is like a pointer set to either the main area or the spare area. The spare area of bytes 512 to 527 may be selectively accessed by writing the Read2 command with GND input pin low. Addresses A_0 to A_3 set the starting address of the spare area while addresses A_4 to A_7 are ignored. Unless the operation is aborted, the page address is automatically incremented for sequential row read as in Read1 operation and spare sixteen bytes of each page may be sequentially read. The Read1 command(00h/01h) is needed to move the pointer back to the main area. Figures 3 through 6 show typical sequence and timings for each read operation.

Sequential Row Read is available only on K9F6408U0C_T,Q or K9F6408U0C_V,F :

After the data of last column address is clocked out, the next page is automatically selected for sequential row read. Waiting 10μs again allows reading the selected page. The sequential row read operation is terminated by bringing $\overline{CE}$ high. Unless the operation is aborted, the page address is automatically incremented for sequential row read as in Read1 operation and spare sixteen bytes of each page may be sequentially read. The Sequential Read 1 and 2 operation is allowed only within a block and after the last page of a block is readout, the sequential read operation must be terminated by bringing $\overline{CE}$ high. When the page address moves onto the next block, read command and address must be given. Figures 5, 6 show typical sequence and timings for sequential row read operation.

Figure 3. Read1 Operation



* After data access on 2nd half array by 01H command, the start pointer is automatically moved to 1st half array (00h) at next cycle.

Figure 4. Read2 Operation

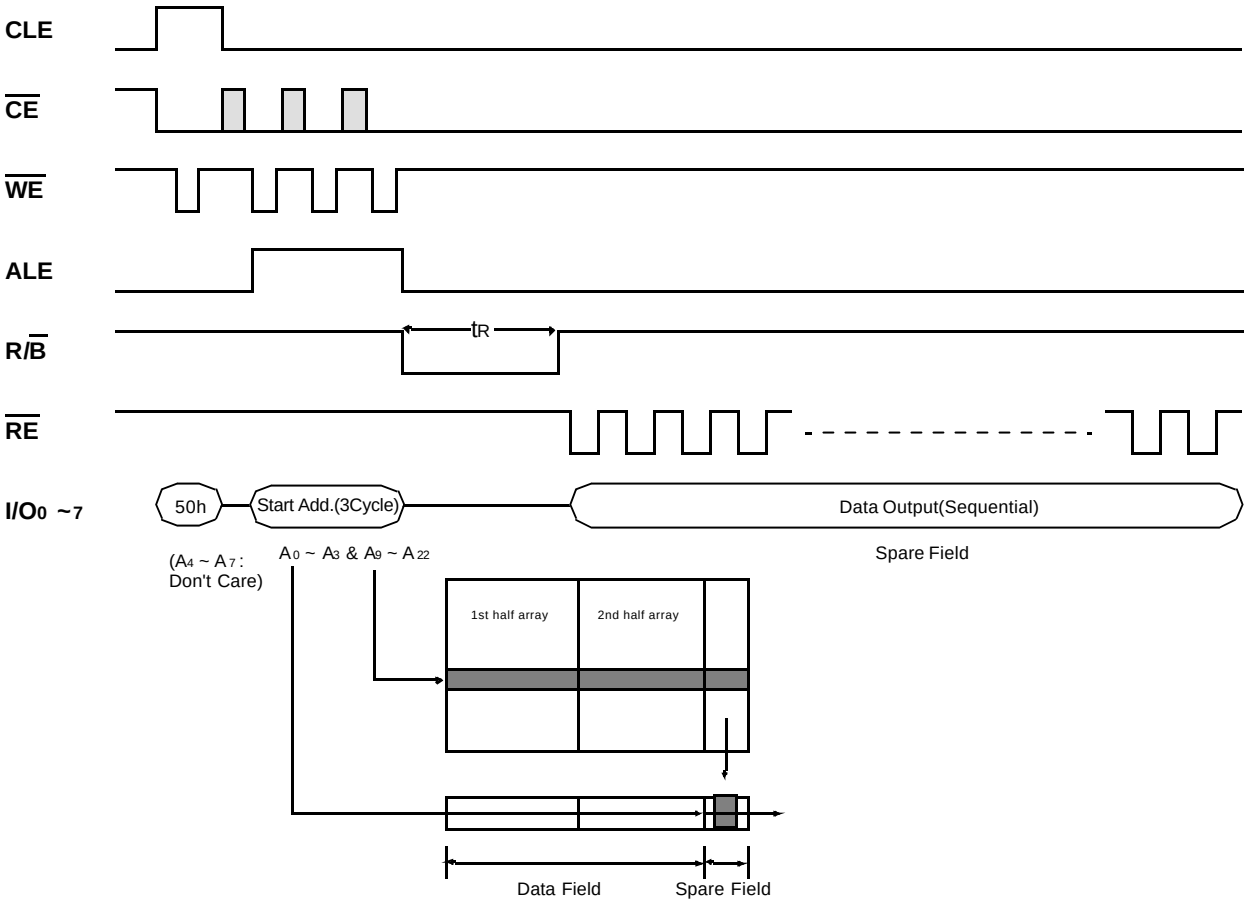


Figure 5. Sequential Row Read1 Operation
(only for K9F6408U0C-T,Q and K9F6408U0C-V,F valid within a block)

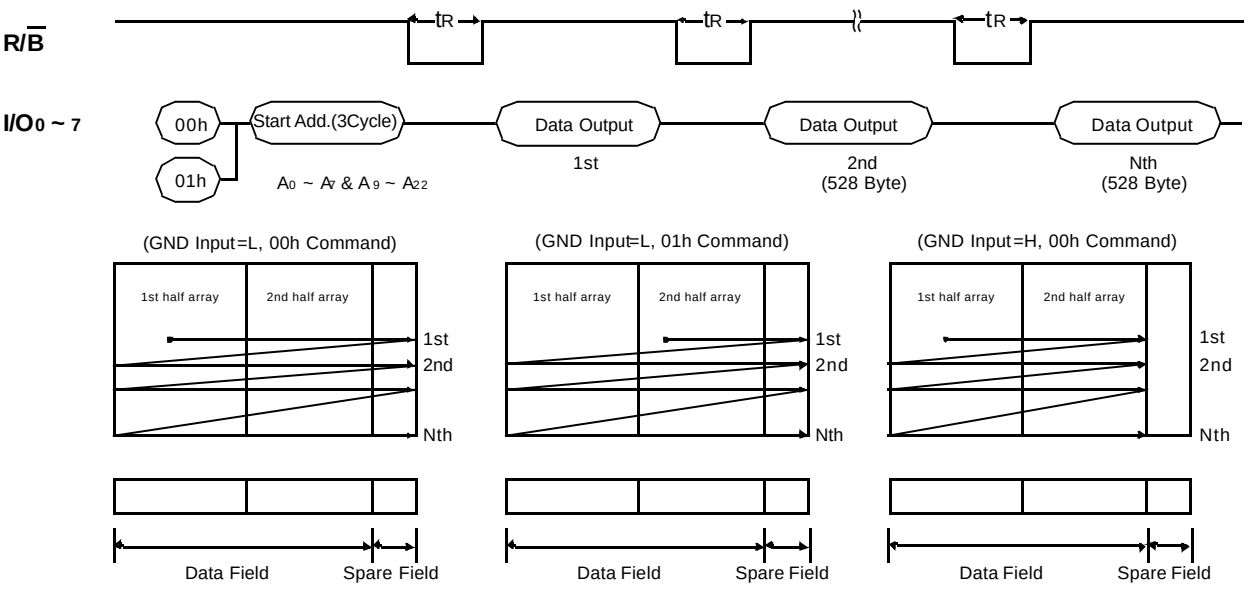
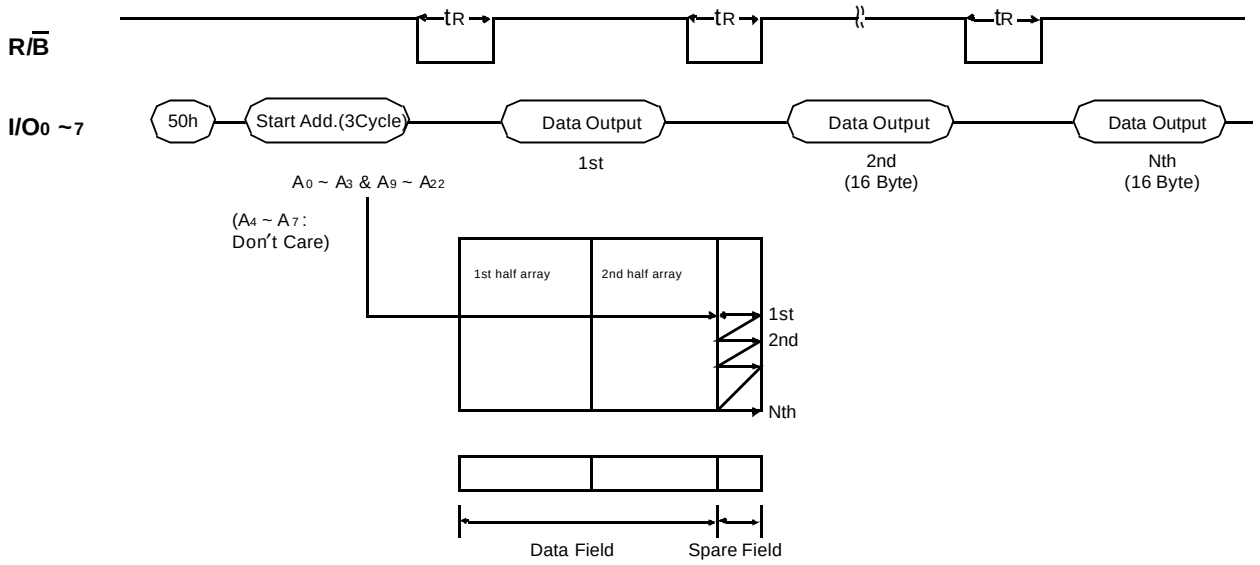


Figure 6. Sequential Row Read2 Operation (GND Input=Fixed Low)

(only for K9F6408U0C-T,Q and K9F6408U0C-V,F valid within a block)

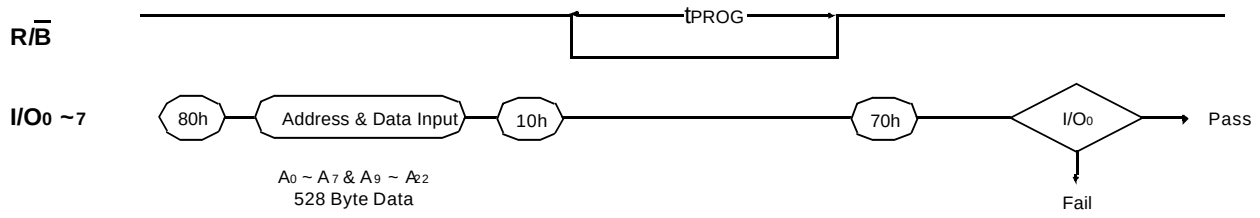


PAGE PROGRAM

The device is programmed basically on a page basis, but it does allow multiple partial page programming of a byte or consecutive bytes up to 528, in a single page program cycle. The number of consecutive partial page programming operation within the same page without an intervening erase operation should not exceed 2 for main array and 3 for spare array. The addressing may be done in any random order in a block. A page program cycle consists of a serial data loading period in which up to 528 bytes of data may be loaded into the page register, followed by a non-volatile programming period where the loaded data is programmed into the appropriate cell. Serial data loading can be started from 2nd half array by moving pointer. About the pointer operation, please refer to the attached technical notes.

The serial data loading period begins by inputting the Serial Data Input command(80h), followed by the three cycle address input and then serial data loading. The bytes other than those to be programmed do not need to be loaded.The Page Program confirm command(10h) initiates the programming process. Writing 10h alone without previously entering the serial data will not initiate the programming process. The internal write controller automatically executes the algorithms and timings necessary for program and verify, thereby freeing the CPU for other tasks. Once the program process starts, the Read Status Register command may be entered, with $\overline{RE}$ and $\overline{CE}$ low, to read the status register. The CPU can detect the completion of a program cycle by monitoring the R/$\overline{B}$ output, or the Status bit(I/O 6) of the Status Register. Only the Read Status command and Reset command are valid while programming is in progress. When the Page Program is complete, the Write Status Bit(I/O 0) may be checked(Figure 7). The internal write verify detects only errors for "1"s that are not successfully programmed to "0"s. The command register remains in Read Status command mode until another valid command is written to the command register.

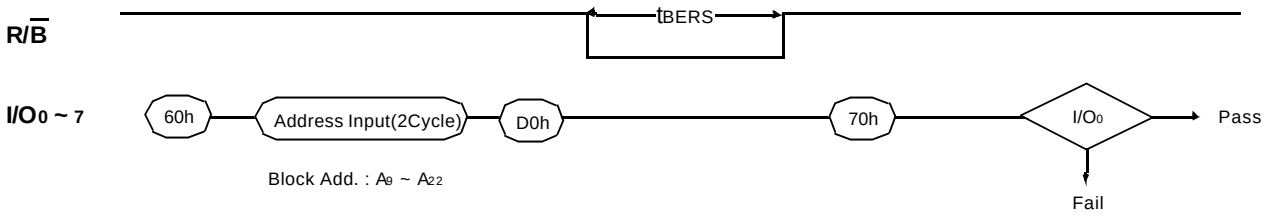
Figure 7. Program & Read Status Operation



BLOCK ERASE

The Erase operation is done on a block(8K Byte) basis. Block address loading is accomplished in two cycles initiated by an Erase Setup command(60h). Only address A_{13} to A_{22} is valid while A_9 to A_{12} is ignored. The Erase Confirm command(D0h) following the block address loading initiates the internal erasing process. This two-step sequence of setup followed by execution command ensures that memory contents are not accidentally erased due to external noise conditions.
At the rising edge of WE after the erase confirm command input, the internal write controller handles erase and erase-verify. When the erase operation is completed, the Write Status Bit(I/O 0) may be checked.
Figure 8 details the sequence.

Figure 8. Block Erase Operation



READ STATUS

The device contains a Status Register which may be read to find out whether program or erase operation is completed, and whether the program or erase operation is completed successfully. After writing 70h command to the command register, a read cycle outputs the content of the Status Register to the I/O pins on the falling edge of $\overline{CE}$ or $\overline{RE}$, whichever occurs last. This two line control allows the system to poll the progress of each device in multiple memory connections even when R/$\overline{B}$ pins are common-wired. $\overline{RE}$ or $\overline{CE}$ does not need to be toggled for updated status. Refer to table 2 for specific Status Register definitions. The command register remains in Status Read mode until further commands are issued to it. Therefore, if the status register is read during a random read cycle, a read command(00h or 50h) should be given before sequential page read cycle.

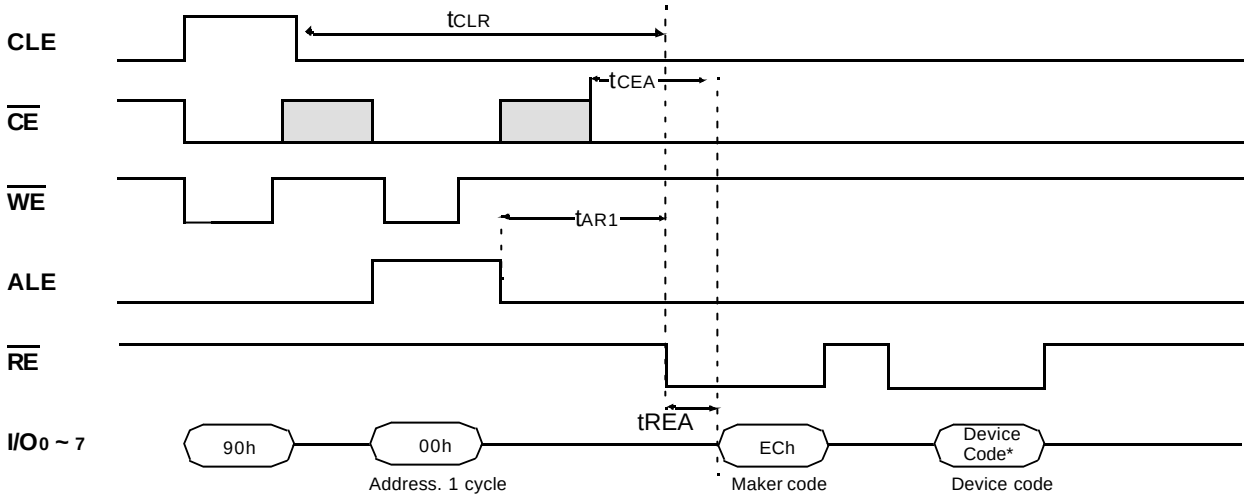
Table2. Read Status Register Definition

I/O #	Status	Definition
I/O_0	Program / Erase	"0" : Successful Program / Erase
		"1" : Error in Program / Erase
I/O_1	Reserved for Future Use	"0"
I/O_2		"0"
I/O_3		"0"
I/O_4		"0"
I/O_5		"0"
I/O_6	Device Operation	"0" : Busy "1" : Ready
I/O_7	Write Protect	"0" : Protected "1" : Not Protected

READ ID

The device contains a product identification mode, initiated by writing 90h to the command register, followed by an address input of 00h. Two read cycles sequentially output the manufacture code(ECh), and the device code respectively. The command register remains in Read ID mode until further commands are issued to it. Figure 9 shows the operation sequence.

Figure 9. Read ID Operation



Device	Device Code*
K9F6408Q0C	39h
K9F6408U0C	E6h

RESET

The device offers a reset feature, executed by writing FFh to the command register. When the device is in Busy state during random read, program or erase modes, the reset operation will abort these operation. The contents of memory cells being altered are no longer valid, as the data will be partially programmed or erased. Internal address registers are cleared to "0"s and data registers to "1"s. The command register is cleared to wait for the next command, and the Status Register is cleared to value C0h when $\overline{WP}$ is high. Refer to table 3 for device status after reset operation. If the device is already in reset state a new reset command will not be accepted to by the command register. The R/$\overline{B}$ pin transitions to low for t_{RST} after the Reset command is written. Reset command is not necessary for normal operation. Refer to Figure 10 below.

Figure 10. RESET Operation

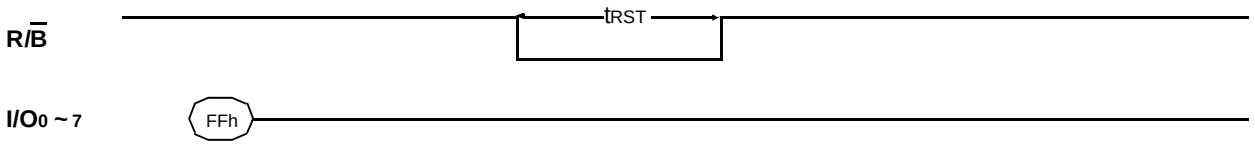


Table3. Device Status

	After Power-up	After Reset
Operation Mode	Read 1	Waiting for next command

READY/$\overline{BUSY}$

The device has a R/$\overline{B}$ output that provides a hardware method of indicating the completion of a page program, erase and random read completion. The R/$\overline{B}$ pin is normally high but transitions to low after program or erase command is written to the command register or random read is started after address loading. It returns to high when the internal controller has finished the operation. The pin is an open-drain driver thereby allowing two or more R/$\overline{B}$ outputs to be Or-tied. Because pull-up resistor value is related to tr(R/$\overline{B}$) and current drain during busy(ibusy) , an appropriate value can be obtained with the following reference chart(Fig 11). Its value can be determined by the following guidance.

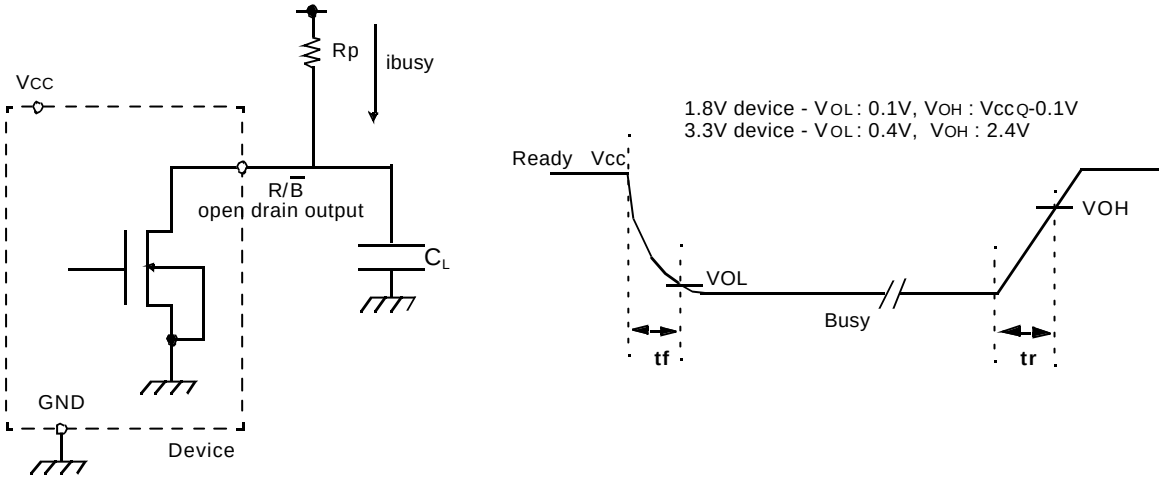
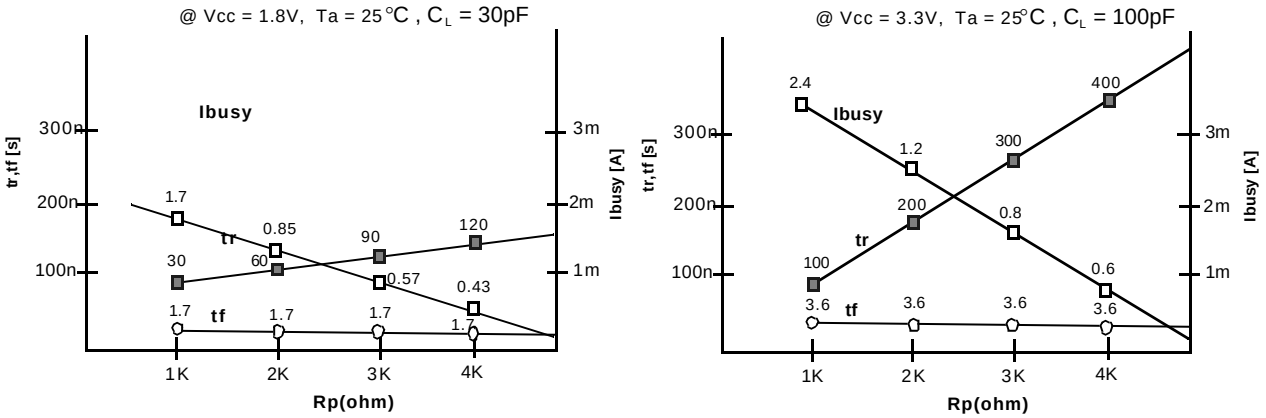


Figure 11. Rp vs tr ,tf & Rp vs ibusy



Rp value guidance

$$Rp(min, 1.8V\ part) = \frac{V_{CC}(Max.) - V_{OL}(Max.)}{I_{OL} + \Sigma I_L} = \frac{1.85V}{3mA + \Sigma I_L}$$

$$Rp(min, 3.3V\ part) = \frac{V_{CC}(Max.) - V_{OL}(Max.)}{I_{OL} + \Sigma I_L} = \frac{3.2V}{8mA + \Sigma I_L}$$

where I_L is the sum of the input currents of all devices tied to the R/$\overline{B}$ pin.

Rp(max) is determined by maximum permissible limit of tr

Data Protection & Powerup sequence

The device is designed to offer protection from any involuntary program/erase during power-transitions. An internal voltage detector disables all functions whenever Vcc is below about 1.1V/2V(K9F6408Q0C:1.1V, K9F6408U0C:2V). $\overline{WP}$ pin provides hardware protection and is recommended to be kept at V_{IL} during power-up and power-down and recovery time of minimum 10µs is required before internal circuit gets ready for any command sequences as shown in Figure 12. The two step command sequence for program/erase provides additional software protection.

Figure 12. AC Waveforms for Power Transition