



CAT5112

32-Tap Digitally Programmable Potentiometer (DPP™) with Buffered Wiper

FEATURES

- 32-position linear taper potentiometer
- Non-volatile NVRAM wiper storage; buffered wiper
- Low power CMOS technology
- Single supply operation: 2.5V-6.0V
- Increment up/down serial interface
- Resistance values: 10kΩ, 50kΩ and 100kΩ
- Available in PDIP, SOIC, TSSOP and MSOP packages

APPLICATIONS

- Automated product calibration
- Remote control adjustments
- Offset, gain and zero control
- Tamper-proof calibrations
- Contrast, brightness and volume controls
- Motor controls and feedback systems
- Programmable analog functions

DESCRIPTION

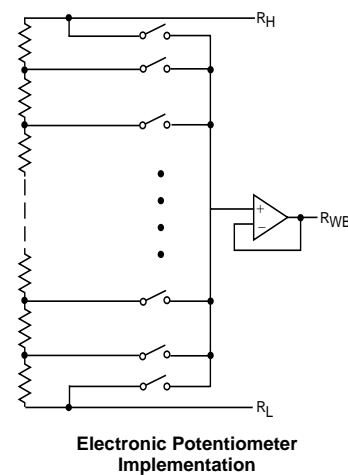
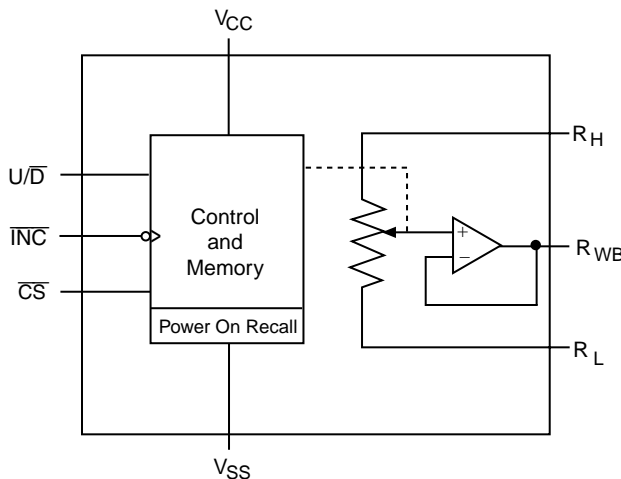
The CAT5112 is a single digitally programmable potentiometer (DPP™) designed as a electronic replacement for mechanical potentiometers and trim pots. Ideal for automated adjustments on high volume production lines, they are also well suited for applications where equipment requiring periodic adjustment is either difficult to access or located in a hazardous or remote environment.

The CAT5112 contains a 32-tap series resistor array connected between two terminals R_H and R_L . An up/down counter and decoder that are controlled by three input pins, determines which tap is connected to the wiper, R_{WB} . The CAT5112 wiper is buffered by an op amp that operates rail to rail. The wiper setting, stored in non-volatile NVRAM memory, is not lost when the device is powered down and is automatically recalled when power is returned. The wiper can be adjusted to test new

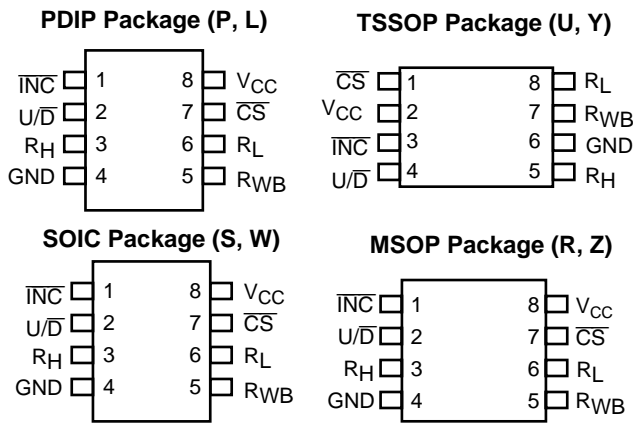
system values without effecting the stored setting. Wiper-control of the CAT5112 is accomplished with three input control pins, \overline{CS} , U/\overline{D} , and \overline{INC} . The \overline{INC} input increments the wiper in the direction which is determined by the logic state of the U/\overline{D} input. The \overline{CS} input is used to select the device and also store the wiper position prior to power down.

The digitally programmable potentiometer can be used as a buffered voltage divider. For applications where the potentiometer is used as a 2-terminal variable resistor, please refer to the CAT5114. The buffered wiper of the CAT5112 is not compatible with that application. DPPs bring variability and programmability to a broad range of applications and are used primarily to control, regulate or adjust a characteristic or parameter of an analog circuit.

FUNCTIONAL DIAGRAM



PIN CONFIGURATION



PIN FUNCTIONS

Pin Name	Function
\overline{INC}	Increment Control
U/\overline{D}	Up/Down Control
R _H	Potentiometer High Terminal
GND	Ground
R _{WB}	Buffered Wiper Terminal
R _L	Potentiometer Low Terminal
\overline{CS}	Chip Select
V _{CC}	Supply Voltage

PIN DESCRIPTIONS

\overline{INC} : Increment Control Input

The \overline{INC} input (on the falling edge) moves the wiper in the up or down direction determined by the condition of the U/\overline{D} input.

U/\overline{D} : Up/Down Control Input

The U/\overline{D} input controls the direction of the wiper movement. When in a high state and \overline{CS} is low, any high-to-low transition on \overline{INC} will cause the wiper to move one increment toward the R_H terminal. When in a low state and \overline{CS} is low, any high-to-low transition on \overline{INC} will cause the wiper to move one increment towards the R_L terminal.

R_H: High End Potentiometer Terminal

R_H is the high end terminal of the potentiometer. It is not required that this terminal be connected to a potential greater than the R_L terminal. Voltage applied to the R_H terminal cannot exceed the supply voltage, V_{CC} or go below ground, GND.

R_{WB}: Wiper Potentiometer Terminal (Buffered)

R_{WB} is the buffered wiper terminal of the potentiometer. Its position on the resistor array is controlled by the control inputs, \overline{INC} , U/\overline{D} and \overline{CS} .

R_L: Low End Potentiometer Terminal

R_L is the low end terminal of the potentiometer. It is not required that this terminal be connected to a potential less than the R_H terminal. Voltage applied to the R_L terminal cannot exceed the supply voltage, V_{CC} or go below ground, GND. R_L and R_H are electrically interchangeable.

\overline{CS} : Chip Select

The chip select input is used to activate the control input

of the CAT5112 and is active low. When in a high state, activity on the \overline{INC} and U/\overline{D} inputs will not affect or change the position of the wiper.

DEVICE OPERATION

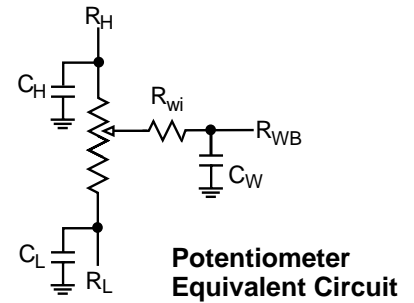
The CAT5112 operates like a digitally controlled potentiometer with R_H and R_L equivalent to the high and low terminals and R_{WB} equivalent to the mechanical potentiometer's wiper. There are 32 available tap positions including the resistor end points, R_H and R_L. There are 31 resistor elements connected in series between the R_H and R_L terminals. The wiper terminal is connected to one of the 32 taps and controlled by three inputs, \overline{INC} , U/\overline{D} and \overline{CS} . These inputs control a five-bit up/down counter whose output is decoded to select the wiper position. The selected wiper position can be stored in nonvolatile memory using the \overline{INC} and \overline{CS} inputs.

With \overline{CS} set LOW the CAT5112 is selected and will respond to the U/\overline{D} and \overline{INC} inputs. HIGH to LOW transitions on \overline{INC} will increment or decrement the wiper (depending on the state of the U/\overline{D} input and five-bit counter). The wiper, when at either fixed terminal, acts like its mechanical equivalent and does not move beyond the last position. The value of the counter is stored in nonvolatile memory whenever \overline{CS} transitions HIGH while the \overline{INC} input is also HIGH. When the CAT5112 is powered-down, the last stored wiper counter position is maintained in the nonvolatile memory. When power is restored, the contents of the memory are recalled and the counter is set to the value stored.

With \overline{INC} set low, the CAT5112 may be de-selected and powered down without storing the current wiper position in nonvolatile memory. This allows the system to always power up to a preset value stored in nonvolatile memory.

OPERATING MODES

\overline{INC}	\overline{CS}	U/\overline{D}	Operation
High to Low	Low	High	Wiper toward H
High to Low	Low	Low	Wiper toward L
High	Low to High	X	Store Wiper Position
Low	Low to High	X	No Store, Return to Standby
X	High	X	Standby



ABSOLUTE MAXIMUM RATINGS

Supply Voltage V_{CC} to GND	-0.5V to +7V
Inputs \overline{CS} to GND	-0.5V to $V_{CC} + 0.5V$
\overline{INC} to GND	-0.5V to $V_{CC} + 0.5V$
U/\overline{D} to GND	-0.5V to $V_{CC} + 0.5V$
R_H to GND	-0.5V to $V_{CC} + 0.5V$
R_L to GND	-0.5V to $V_{CC} + 0.5V$
R_{WB} to GND	-0.5V to $V_{CC} + 0.5V$

Operating Ambient Temperature

Commercial ('C' or Blank suffix)	0°C to +70°C
Industrial ('I' suffix)	-40°C to +85°C
Junction Temperature	+150°C
Storage Temperature	-65°C to +150°C
Lead Soldering (10 sec max)	+300°C

* Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. Absolute Maximum Ratings are limited values applied individually while other parameters are within specified operating conditions, and functional operation at any of these conditions is NOT implied. Device performance and reliability may be impaired by exposure to absolute rating conditions for extended periods of time.

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Test Method	Min	Typ	Max	Units
$V_{ZAP}^{(1)}$	ESD Susceptibility	MIL-STD-883, Test Method 3015	2000			Volts
$I_{LTH}^{(1)(2)}$	Latch-Up	JEDEC Standard 17	100			mA
T_{DR}	Data Retention	MIL-STD-883, Test Method 1008	100			Years
N_{END}	Endurance	MIL-STD-883, Test Method 1003	1,000,000			Stores

DC Electrical Characteristics: $V_{CC} = +2.5V$ to $+6.0V$ unless otherwise specified

Power Supply

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{CC}	Operating Voltage Range		2.5	—	6.0	V
I_{CC1}	Supply Current (Increment)	$V_{CC} = 6V, f = 1MHz, I_W=0$ $V_{CC} = 6V, f = 250kHz, I_W=0$	—	—	200 100	μA
I_{CC2}	Supply Current (Write)	Programming, $V_{CC} = 6V$ $V_{CC} = 3V$	—	—	1 500	mA μA
$ISB_1^{(2)}$	Supply Current (Standby)	$CS=V_{CC}-0.3V$ $U/D, INC=V_{CC}-0.3V$ or GND	—	75	150	μA

Logic Inputs

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{IH}	Input Leakage Current	$V_{IN} = V_{CC}$	—	—	10	μA
I_{IL}	Input Leakage Current	$V_{IN} = 0V$	—	—	-10	μA
V_{IH1}	TTL High Level Input Voltage	$4.5V \leq V_{CC} \leq 5.5V$	2	—	V_{CC}	V
V_{IL1}	TTL Low Level Input Voltage		0	—	0.8	V
V_{IH2}	CMOS High Level Input Voltage	$2.5V \leq V_{CC} \leq 6V$	$V_{CC} \times 0.7$	—	$V_{CC} + 0.3$	V
V_{IL2}	CMOS Low Level Input Voltage		-0.3	—	$V_{CC} \times 0.2$	V

- NOTES:**
- (1) This parameter is tested initially and after a design or process change that affects the parameter.
 - (2) Latch-up protection is provided for stresses up to 100mA on address and data pins from -1V to $V_{CC} + 1V$
 - (3) I_W =source or sink
 - (4) These parameters are periodically sampled and are not 100% tested.

Potentiometer Parameters

Symbol	Parameter	Conditions	Min	Typ	Max	Units
R _{POT}	Potentiometer Resistance	-10 Device		10		kΩ
		-50 Device		50		
		-00 Device		100		
	Pot Resistance Tolerance				±20	%
V _{RH}	Voltage on R _H pin		0		V _{CC}	V
V _{RL}	Voltage on R _L pin		0		V _{CC}	V
	Resolution			1		%
INL	Integral Linearity Error	I _W ≤ 2μA		0.5	1	LSB
DNL	Differential Linearity Error	I _W ≤ 2μA		0.25	0.5	LSB
R _{OUT}	Buffer Output Resistance	.05V _{CC} ≤ V _{WB} ≤ .95V _{CC} , V _{CC} =5V			1	Ω
I _{OUT}	Buffer Output Current	.05V _{CC} ≤ V _{WB} ≤ .95V _{CC} , V _{CC} =5V			3	mA
TC _{R_{POT}}	TC of Pot Resistance			300		ppm/°C
TC _{RATIO}	Ratiometric TC			TBD		ppm/°C
R _{ISO}	Isolation Resistance			TBD		Ω
C _{RH} /C _{R_L} /C _{R_W}	Potentiometer Capacitances			8/8/25		pF
f _c	Frequency Response	Passive Attenuator, 10kΩ		1.7		MHz
V _{WB(SWING)}	Output Voltage Range	I _{OUT} ≤ 100μA, V _{CC} =5V	0.01V _{CC}		.99V _{CC}	

AC CONDITIONS OF TEST

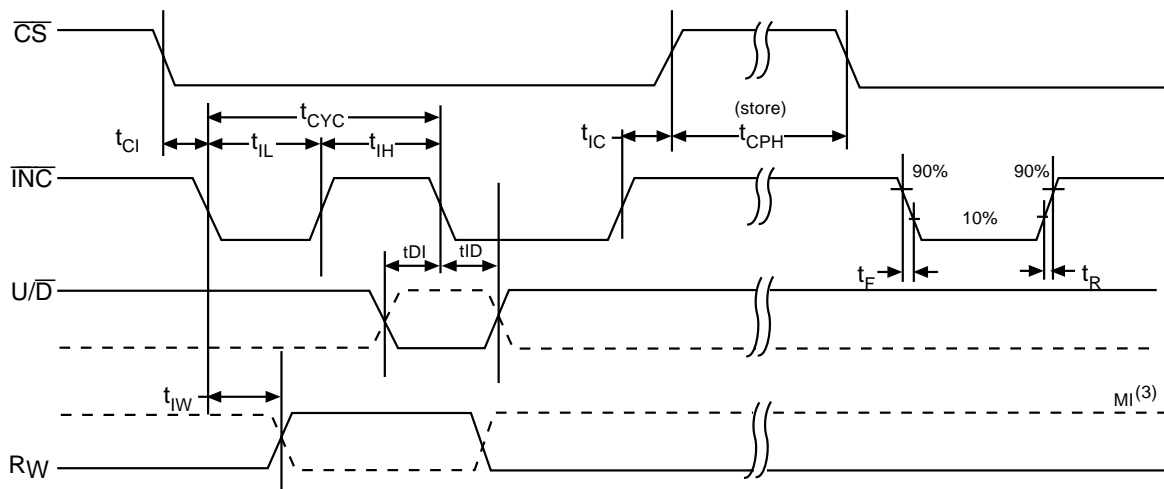
V _{CC} Range	2.5V ≤ V _{CC} ≤ 6V
Input Pulse Levels	0.2V _{CC} to 0.7V _{CC}
Input Rise and Fall Times	10ns
Input Reference Levels	0.5V _{CC}

AC OPERATING CHARACTERISTICS:

V_{CC} = +2.5V to +6.0V, V_H = V_{CC}, V_L = 0V, unless otherwise specified

Symbol	Parameter	Min	Typ ⁽¹⁾	Max	Units
t _{CI}	\overline{CS} to INC Setup	100	—	—	ns
t _{DI}	U/D to \overline{INC} Setup	50	—	—	ns
t _{ID}	U/D to \overline{INC} Hold	100	—	—	ns
t _{IL}	\overline{INC} LOW Period	250	—	—	ns
t _{IH}	\overline{INC} HIGH Period	250	—	—	ns
t _{IC}	\overline{INC} Inactive to \overline{CS} Inactive	1	—	—	μs
t _{CPH}	\overline{CS} Deselect Time (NO STORE)	100	—	—	ns
t _{CPH}	\overline{CS} Deselect Time (STORE)	10	—	—	ms
t _{IW}	\overline{INC} to V _{OUT} Change	—	1	5	μs
t _{CYC}	\overline{INC} Cycle Time	1	—	—	μs
t _R , t _F ⁽²⁾	\overline{INC} Input Rise and Fall Time	—	—	500	μs
t _{PU} ⁽²⁾	Power-up to Wiper Stable	—	—	1	msec
t _{WR}	Store Cycle	—	5	10	ms

A. C. TIMING

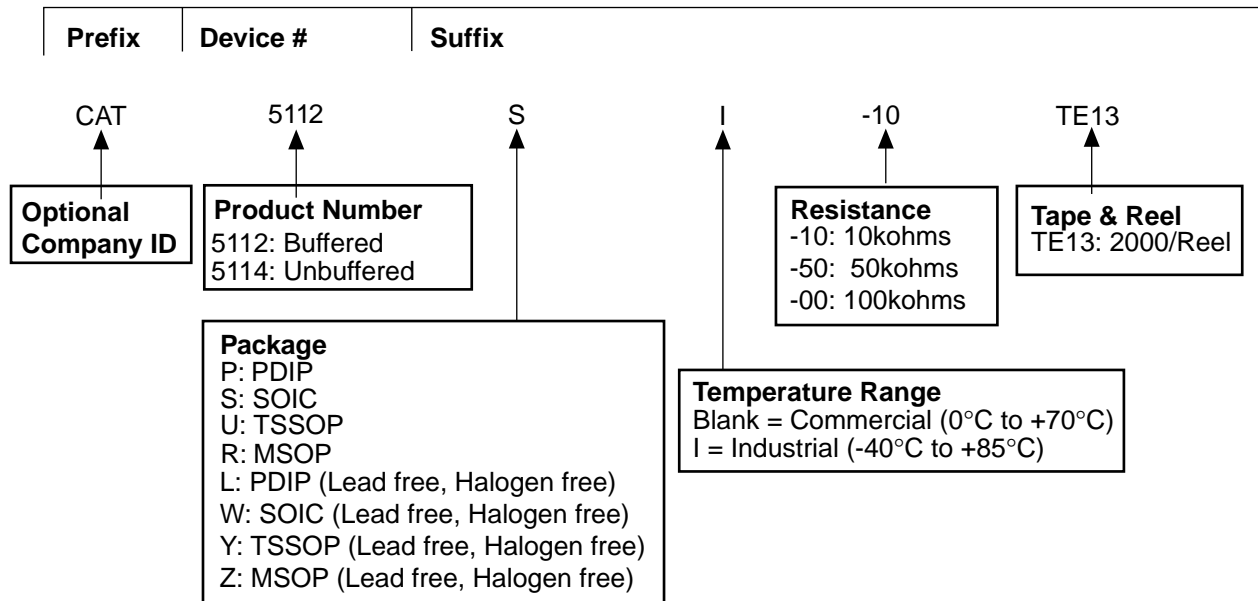


(1) Typical values are for T_A=25°C and nominal supply voltage.

(2) This parameter is periodically sampled and not 100% tested.

(3) MI in the A.C. Timing diagram refers to the minimum incremental change in the W output due to a change in the wiper position.

ORDERING INFORMATION



REVISION HISTORY

Date	Rev.	Reason
3/10/2004	J	Updated Potentiometer Parameters

Notes:

(1) The device used in the above example is a CAT5112 SI-10TE13 (SOIC, 10K Ohms, Industrial Temperature, Tape & Reel)

Copyrights, Trademarks and Patents

Trademarks and registered trademarks of Catalyst Semiconductor include each of the following:

DPP™ AE²™

Catalyst Semiconductor has been issued U.S. and foreign patents and has patent applications pending that protect its products. For a complete list of patents issued to Catalyst Semiconductor contact the Company's corporate office at 408.542.1000.

CATALYST SEMICONDUCTOR MAKES NO WARRANTY, REPRESENTATION OR GUARANTEE, EXPRESS OR IMPLIED, REGARDING THE SUITABILITY OF ITS PRODUCTS FOR ANY PARTICULAR PURPOSE, NOR THAT THE USE OF ITS PRODUCTS WILL NOT INFRINGE ITS INTELLECTUAL PROPERTY RIGHTS OR THE RIGHTS OF THIRD PARTIES WITH RESPECT TO ANY PARTICULAR USE OR APPLICATION AND SPECIFICALLY DISCLAIMS ANY AND ALL LIABILITY ARISING OUT OF ANY SUCH USE OR APPLICATION, INCLUDING BUT NOT LIMITED TO, CONSEQUENTIAL OR INCIDENTAL DAMAGES.

Catalyst Semiconductor products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Catalyst Semiconductor product could create a situation where personal injury or death may occur.

Catalyst Semiconductor reserves the right to make changes to or discontinue any product or service described herein without notice. Products with data sheets labeled "Advance Information" or "Preliminary" and other products described herein may not be in production or offered for sale.

Catalyst Semiconductor advises customers to obtain the current version of the relevant product information before placing orders. Circuit diagrams illustrate typical semiconductor applications and may not be complete.



CATALYST

Catalyst Semiconductor, Inc.
Corporate Headquarters
1250 Borregas Avenue
Sunnyvale, CA 94089
Phone: 408.542.1000
Fax: 408.542.1200
www.catsemi.com

Publication #: 2002
Revision: J
Issue date: 3/10/04
Type: Final