2.5V MULTI-QUEUE FIFO (8 QUEUES) 18 BIT WIDE CONFIGURATION 589,824 bits, 1,179,648 bits and 2,359,296 bits

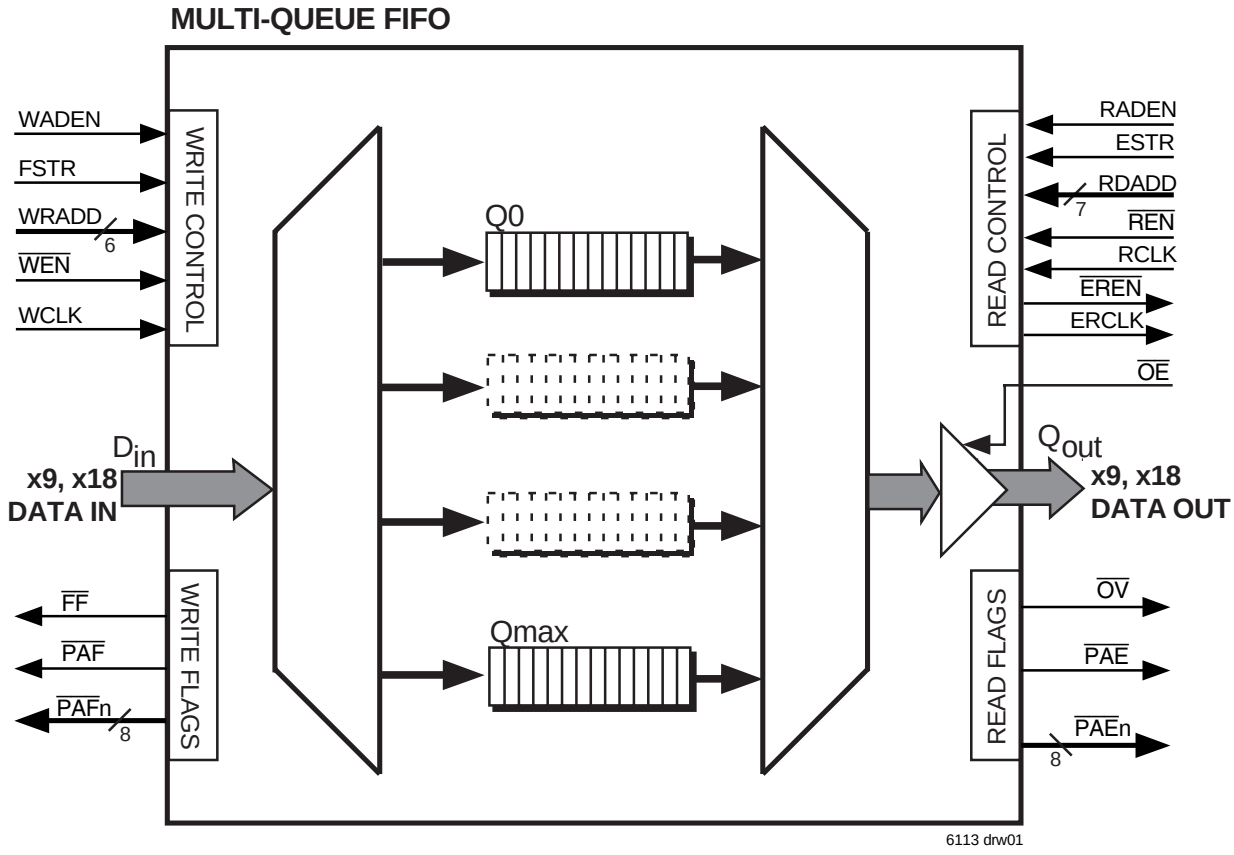
ADVANCE INFORMATION

IDT72T51333
IDT72T51343
IDT72T51353

FEATURES:

- Choose from among the following memory density options:
  IDT72T51333 — Total Available Memory = 589,824 bits
  IDT72T51343 — Total Available Memory = 1,179,648 bits
  IDT72T51353 — Total Available Memory = 2,359,296 bits
- Configurable from 1 to 8 Queues
- Queues may be configured at master reset from the pool of Total Available Memory in blocks of 512 x 18 or 1,024 x 9
- Independent Read and Write access per queue
- User selectable I/O: 2.5V LVTTL, 1.5V HSTL, 1.8V eHSTL
- User programmable via serial port
- Default Multi-Queue device configurations
  -IDT72T51333: 4,096 x 18 x 8Q
  -IDT72T51343: 8,192 x 18 x 8Q
  -IDT72T51353: 16,384 x 18 x 8Q
- 100% Bus Utilization, Read and Write on every clock cycle
- 200 MHz High speed operation (5ns cycle time)
- 3.6ns access time
- Echo Read Enable & Echo Read Clock Outputs
- Individual, Active queue flags ($\overline{OV}$, $\overline{FF}$, $\overline{PAE}$, $\overline{PAF}$, $\overline{PR}$)
- 8 bit parallel flag status on both read and write ports
- Provides continuous $\overline{PAE}$ and $\overline{PAF}$ status of up to 8 Queues
- Global Bus Matching - (All Queues have same Input Bus Width and Output Bus Width)
- User Selectable Bus Matching Options:
  - x18in to x18out
  - x9in to x18out
  - x18in to x9out
  - x9in to x9out
- FWFT mode of operation on read port
- Packet Ready mode of operation
- Partial Reset, clears data in single Queue
- Expansion of up to 8 Multi-Queue devices in parallel is available
- Power Down Input provides additional power savings in HSTL and eHSTL modes.
- JTAG Functionality (Boundary Scan)
- Available in a 256-pin PBGA, 1mm pitch, 17mm x 17mm
- HIGH Performance submicron CMOS technology

DATA PATH FLOW DIAGRAM



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DESCRIPTION:

The IDT72T51333/72T51343/72T51353 Multi-Queue FIFO device is a single chip within which anywhere between 1 and 8 discrete FIFO queues can be setup. All queues within the device have a common data input bus, (write port) and a common data output bus, (read port). Data written into the write port is directed to a respective queue via an internal de-multiplex operation, addressed by the user. Data read from the read port is accessed from a respective queue via an internal multiplex operation, addressed by the user. Data writes and reads can be performed at high speeds up to 200MHz, with access times of 3.6ns. Data write and read operations are totally independent of each other, a queue maybe selected on the write port and a different queue on the read port or both ports may select the same queue simultaneously.

The device provides Full flag and Output Valid flag status for the queue selected for write and read operations respectively. Also a Programmable Almost Full and Programmable Almost Empty flag for each queue is provided. Two 8 bit programmable flag busses are available, providing status of all queues, including queues not selected for write or read operations, these flag busses provide an individual flag per queue.

Bus Matching is available on this device, either port can be 9 bits or 18 bits wide. When Bus Matching is used the device ensures the logical transfer of data throughput in a Little Endian manner.

The user has full flexibility configuring queues within the device, being able to program the total number of queues between 1 and 8, the individual queue depths being independent of each other. The programmable flag positions are also user programmable. All programming is done via a dedicated serial port. If the user does not wish to program the Multi-Queue device, a default option is available that configures the device in a predetermined manner.

Both Master Reset and Partial Reset pins are provided on this device. A Master Reset latches in all configuration setup pins and must be performed before programming of the device can take place. A Partial Reset will reset the read and write pointers of an individual FIFO queue, provided that the queue is selected on both the write port and read port at the time of partial reset.

Echo Read Enable, $\overline{EREN}$ and Echo Read Clock, ERCLK outputs are provided. These are outputs from the read port of the FIFO that are required for high speed data communication, to provide tighter synchronization between the data being transmitted from the Qn outputs and the data being received by the input device. Data read from the read port is available on the output bus with respect to $\overline{EREN}$ and ERCLK, this is very useful when data is being read at high speed.

The Multi-Queue FIFO has the capability of operating its IO in either 2.5V LVTTL, 1.5V HSTL or 1.8V eHSTL mode. The type of IO is selected via the IOSEL input. The core supply voltage (V_{CC}) to the Multi-Queue is always 2.5V, however the output levels can be set independently via a separate supply, V_{DDQ}.

The devices also provide additional power savings via a Power Down Input. This input disables the write port data inputs when no write operations are required.

A JTAG test port is provided, here the Multi-Queue FIFO has a fully functional Boundary Scan feature, compliant with IEEE 1449.1 Standard Test Access Port and Boundary Scan Architecture.

See Figure 1, *Multi-Queue FIFO Block Diagram* for an outline of the functional blocks within the device.

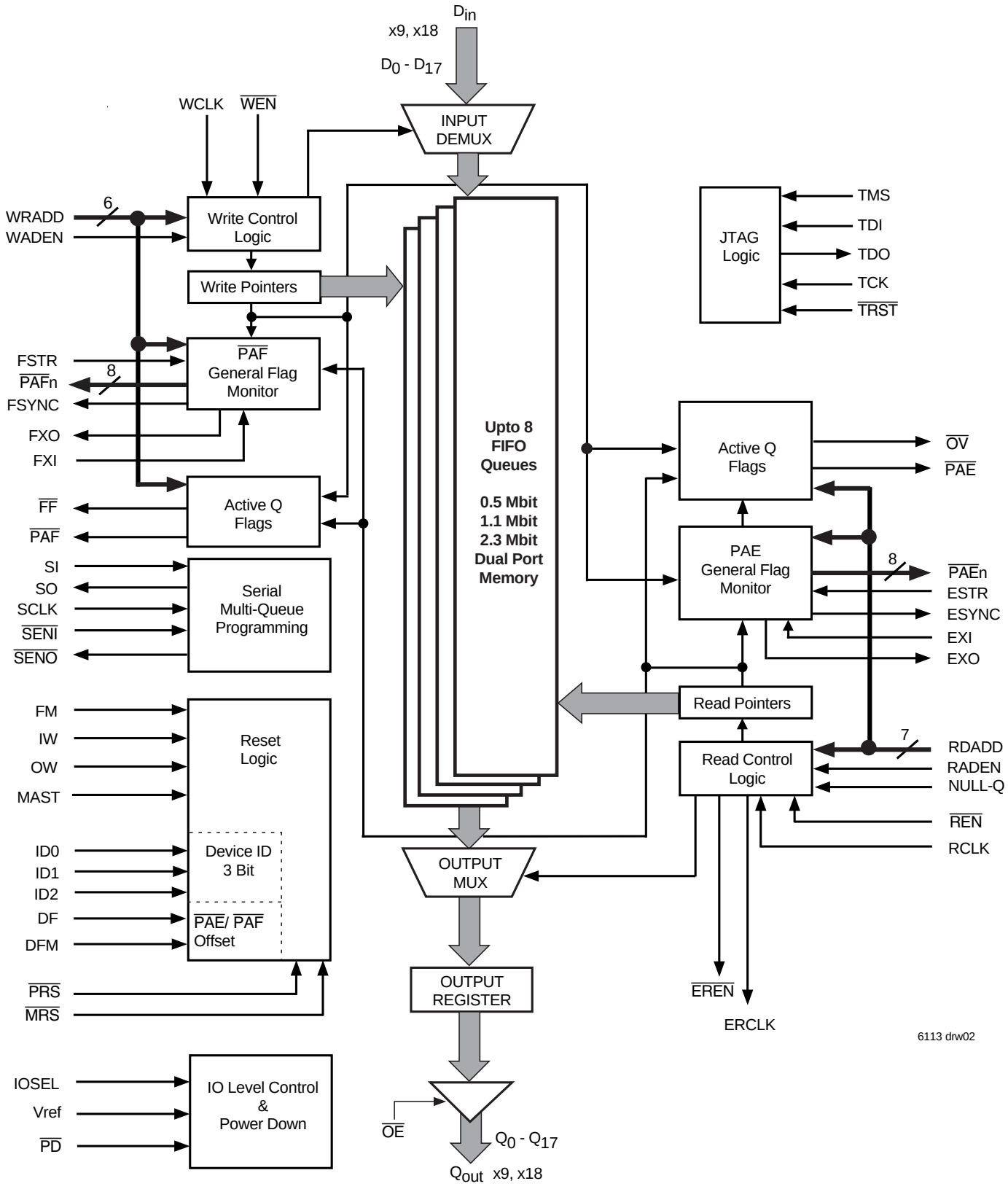
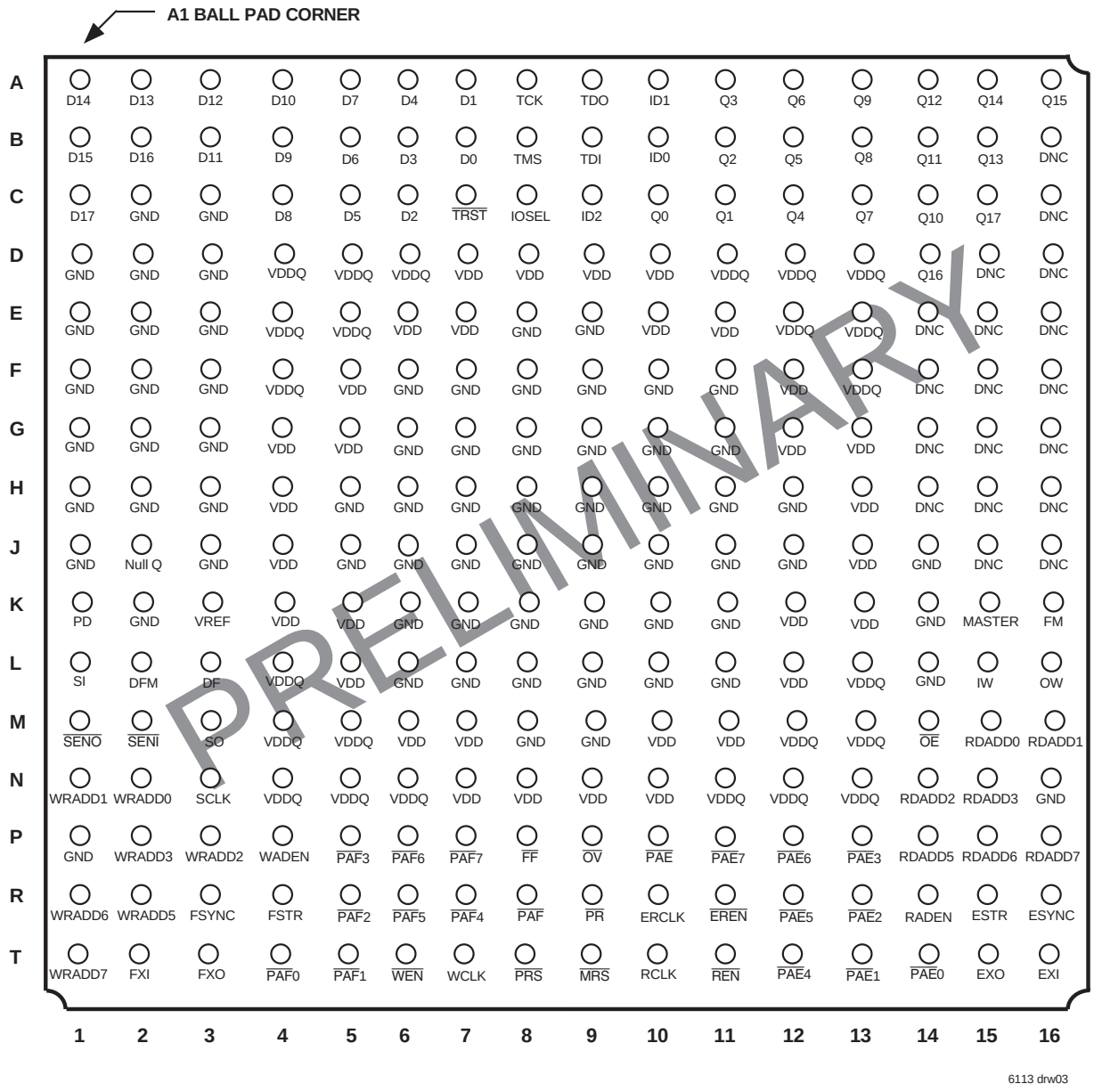


Figure 1. Multi-Queue Block Diagram

PIN CONFIGURATION



PBGA (BB256-1, order code: BB)
TOP VIEW

NOTE:

1. DNC - Do Not Connect.

DETAILED DESCRIPTION

MULTI-QUEUE STRUCTURE

The IDT Multi-Queue FIFO has a single data input port and single data output port with up to 8 FIFO queues in parallel buffering between the two ports. The user can setup between 1 and 8 FIFO Queues within the device. These queues can be configured to utilize the total available memory, providing the user with full flexibility and ability to configure the queues to be various depths, independent of one another.

MEMORY ORGANIZATION/ ALLOCATION

The memory is organized into what is known as "blocks", each block being 512 x 18 or 1,024 x 9 bits. When the user is configuring the number of queues and individual queue sizes the user must allocate the memory to respective queues, in units of blocks, that is, a single queue can be made up from 0 to m blocks, where m is the total number of blocks available within a device. Also the total size of any given queue must be in increments of 512 x 18 or 1,024 x 9. For the IDT72T51333, IDT72T51343 and IDT72T51353 the Total Available Memory is 64, 128 and 256 blocks respectively (a block being 512 x 18 or 1,024 x 9). If any port is configured for x18 bus width, a block size is 512 x 18. If both the write and read ports are configured for x9 bus width, a block size is 1,024 x 9. Queues can be built from these blocks to make any size queue desired and any number of queues desired.

BUS WIDTHS

The input port is common to all FIFO queues within the device, as is the output port. The device provides the user with Bus Matching options such that the input port and output port can be either x9 or x18 bits wide, the read and write port widths being set independently of one another. Because the ports are common to all queues the width of the queues is not individually set, so that the input width of all queues are equal and the output width of all queues are equal.

WRITING TO & READING FROM THE MULTI-QUEUE

Data being written into the device via the input port is directed to a discrete FIFO queue via the write queue select address inputs. Conversely, data being read from the device read port is read from a queue selected via the read queue select address inputs. Data can be simultaneously written into and read from the same FIFO queue or different FIFO queues. Once a queue is selected for data writes or reads, the writing and reading operation is performed in the same manner as conventional IDT synchronous FIFO's, utilizing clocks and enables, there is a single clock and enable per port. When a specific queue is addressed on the write port, data placed on the data inputs is written to that queue sequentially based on the rising edge of a write clock provided setup and hold times are met. Conversely, data is read on to the output port after an access time from a rising edge on a read clock.

The operation of the write port is comparable to the function of a conventional FIFO operating in standard IDT mode. Write operations can be performed on the write port provided that the queue currently selected is not full, a full flag output provides status of the selected queue. The operation of the read port is comparable to the function of a conventional FIFO operating in FWFT mode. When a FIFO queue is selected on the output port, the next word in that queue will automatically fall through to the output register. All subsequent words from that queue require an enabled read cycle. Data cannot be read from a selected queue if that queue is empty, the read port provides an Output Valid flag indicating when data read out is valid. If the user switches to a queue that is empty, the last word from the previous queue will remain on the output register.

As mentioned, the write port has a full flag, providing full status of the selected queue. Along with the full flag a dedicated almost full flag is provided, this almost full flag is similar to the almost full flag of a conventional IDT FIFO. The device provides a user programmable almost full flag for all 8 FIFO queues and when a respective queue is selected on the write port, the almost full flag provides status for that queue. Conversely, the read port has an output valid flag, providing status of the data being read from the queue selected on the read port. As well as the output valid flag the device provides a dedicated almost empty flag. This almost empty flag is similar to the almost empty flag of a conventional IDT FIFO. The device provides a user programmable almost empty flag for all 4 FIFO queues and when a respective queue is selected on the read port, the almost empty flag provides status for that queue.

PROGRAMMABLE FLAG BUSSES

In addition to these dedicated flags, full & almost full on the write port and output valid & almost empty on the read port, there are two flag status busses. An almost full flag status bus is provided, this bus is 8 bits wide. Also, an almost empty flag status bus is provided, again this bus is 8 bits wide. The purpose of these flag busses is to provide the user with a means by which to monitor the data levels within FIFO queues that may not be selected on the write or read port. As mentioned, the device provides almost full and almost empty registers (programmable by the user) for each of the 8 FIFO queues in the device.

The 4 bit $\overline{PAE}$n and 4 bit $\overline{PAF}$n busses provide a discrete status of the Almost Empty and Almost Full conditions of all 8 queue's. If the device is programmed for less than 8 queue's, then there will be a corresponding number of active outputs on the $\overline{PAE}$n and $\overline{PAF}$n busses.

The flag busses can provide a continuous status of all queues. If devices are connected in expansion mode the individual flag busses can be left in a discrete form, providing constant status of all queues, or the busses of individual devices can be connected together to produce a single bus of 8 bits. The device can then operate in a "Polled" or "Direct" mode.

When operating in polled mode the flag bus provides status of each device sequentially, that is, on each rising edge of a clock the flag bus is updated to show the status of each device in order. The rising edge of the write clock will update the Almost Full bus and a rising edge on the read clock will update the Almost Empty bus.

When operating in direct mode the device driving the flag bus is selected by the user. The user addresses the device that will take control of a respective flag bus, these $\overline{PAF}$n and $\overline{PAE}$n flag busses operating independently of one another. Addressing of the Almost Full flag bus is done via the write port and addressing of the Almost Empty flag bus is done via the read port.

EXPANSION

Expansion of Multi-Queue devices is also possible, up to 8 devices can be connected in a parallel fashion providing the possibility of both depth expansion or queue expansion. Depth Expansion means expanding the depths of individual queues. Queue expansion means increasing the total number of queues available. Depth expansion is possible by virtue of the fact that more memory blocks within a Multi-Queue device can be allocated to increase the depth of a queue. For example, depth expansion of 8 devices provides the possibility of 8 queues of 32K x 18 deep within the IDT72T51333, 64K x 18 deep within the IDT72T51343 and 128K x 18 deep within the IDT72T51353, each queue being setup within a single device utilizing all memory blocks available to produce a single queue. This is the deepest FIFO queue that can setup within a device.

For queue expansion of the 8 queue device, a maximum number of 64 (8 x 8) queues may be setup, each queue being 16K x18 or 32K x 9 deep, if less queues are setup, then more memory blocks will be available to increase queue depths if desired. When connecting Multi-Queue devices in expansion mode all respective input pins (data & control) and output pins (data & flags), should be "connected" together between individual devices.

PIN DESCRIPTIONS

Symbol	Name	I/O TYPE	Description
D[17:0] Din	Data Input Bus	LVTTL INPUT	These are the 18 data input pins. Data is written into the device via these input pins on the rising edge of WCLK provided that $\overline{WEN}$ is LOW. Due to bus matching not all inputs may be used, any unused inputs should be tied LOW.
DF[1]	Default Flag	LVTTL INPUT	If the user requires default programming of the Multi-Queue device, this pin must be setup before Master Reset and must not toggle during any device operation. The state of this input at master reset determines the value of the $\overline{PAE}$/$\overline{PAF}$ flag offsets. If DF is LOW the value is 8, if DF is HIGH the value is 128.
DFM[1]	Default Mode	LVTTL INPUT	The Multi-Queue device requires programming after master reset. The user can do this serially via the serial port, or the user can use the default method. If DFM is LOW at master reset then serial mode will be selected, if HIGH then default mode is selected.
ERCLK	RCLK Echo	HSTL-LVTTL OUTPUT	Read Clock Echo output, this output generates a clock based on the read clock input, this is used for Source Synchronous clocking where the receiving devices utilizes the ERCLK to clock data output from the FIFO.
$\overline{EREN}$	$\overline{REN}$ Echo	HSTL-LVTTL OUTPUT	Read Enable Echo output, can be used in conjunction with the ERCLK output to load data output from the FIFO into the receiving device.
ESTR	$\overline{PAE}$n Flag Bus Strobe	LVTTL INPUT	If direct operation of the $\overline{PAE}$n bus has been selected, the ESTR input is used in conjunction with RCLK and the RDADD bus to select a device for its queues to be placed on to the $\overline{PAE}$n bus outputs. A device addressed via the RDADD bus is selected on the rising edge of RCLK provided that ESTR is HIGH. If Polled operations has been selected, ESTR should be tied inactive, LOW.
ESYNC	$\overline{PAE}$n Bus Sync	LVTTL OUTPUT	ESYNC is an output from the Multi-Queue device that provides a synchronizing pulse for the $\overline{PAE}$n bus during Polled operation of the $\overline{PAE}$n bus. During Polled operation each devices queue status flags are loaded on to the $\overline{PAE}$n bus outputs sequentially based on RCLK. The first RCLK rising edge loads device 1 on to $\overline{PAE}$n, the second RCLK rising edge loads device 2 and so on. During the RCLK cycle that a selected device is placed on to the $\overline{PAE}$n bus, the ESYNC output will be HIGH.
EXI	$\overline{PAE}$n Bus Expansion In	LVTTL INPUT	The EXI input is used when Multi-Queue devices are connected in expansion mode and Polled $\overline{PAE}$n bus operation has been selected . EXI of device 'N' connects directly to EXO of device 'N-1'. The EXI receives a token from the previous device in a chain. In single device mode the EXI input should be tied LOW if the $\overline{PAE}$n bus is operated in direct mode. If the $\overline{PAE}$n bus is operated in polled mode the EXI input should be connected to the EXO output of the same device. In expansion mode the EXI of the first device should be tied LOW, when direct mode is selected.
EXO	$\overline{PAE}$n Bus Expansion Out	LVTTL OUTPUT	EXO is an output that is used when Multi-Queue devices are connected in expansion mode and Polled $\overline{PAE}$n bus operation has been selected . EXO of device 'N' connects directly to EXI of device 'N+1'. This pin pulses HIGH when device N places its $\overline{PAE}$ status on to the $\overline{PAE}$n bus with respect to RCLK. This pulse (token) is then passed on to the next device in the chain 'N+1' and on the next RCLK rising edge the first quadrant of device N+1 will be loaded on to the $\overline{PAE}$n bus. This continues through the chain and EXO of the last device is then looped back to EXI of the first device. The ESYNC output of each device in the chain provides synchronization to the user of this looping event.
$\overline{FF}$	Full Flag	LVTTL OUTPUT	This pin provides the full flag output for the active FIFO queue, that is, the queue selected on the input port for write operations, (selected via WCLK, WRADD bus and WADEN). On the WCLK cycle after a queue selection, this flag will show the status of the newly selected queue. Data can be written to this queue on the next cycle provided $\overline{FF}$ is HIGH. This flag has High-Impedance capability, this is important during expansion of devices, when the $\overline{FF}$ flag output of up to 8 devices may be connected together on a common line. The device with a queue selected takes control of the $\overline{FF}$ bus, all other devices place their $\overline{FF}$ output into High-Impedance. When a queue selection is made on the write port this output will switch from High-Impedance control on the next WCLK cycle. This flag is synchronized to WCLK.
FM[1]	Flag Mode	LVTTL INPUT	This pin is setup before a master reset and must not toggle during any device operation. The state of the FM pin during Master Reset will determine whether the $\overline{PAF}$n and $\overline{PAE}$n flag busses operate in either Polled or Direct mode. If this pin is HIGH the mode is Polled, if LOW then it will be Direct.
FSTR	$\overline{PAF}$n Flag Bus Strobe	LVTTL INPUT	If direct operation of the $\overline{PAF}$n bus has been selected, the FSTR input is used in conjunction with WCLK and the WRADD bus to select a device for its queues to be placed on to the $\overline{PAF}$n bus outputs. A device addressed via the WRADD bus is selected on the rising edge of WCLK provided that FSTR is HIGH. If Polled operations has been selected, FSTR should be tied inactive, LOW.

PIN DESCRIPTIONS (CONTINUED)

Symbol	Name	I/O TYPE	Description
FSYNC	$\overline{PAF}$n Bus Sync	LVTTL OUTPUT	FSYNC is an output from the Multi-Queue device that provides a synchronizing pulse for the $\overline{PAF}$n bus during Polled operation of the $\overline{PAF}$n bus. During Polled operation each quadrant of queue status flags is loaded on to the $\overline{PAF}$n bus outputs sequentially based on WCLK. The first WCLK rising edge loads device1on to the $\overline{PAF}$n bus outputs, the second WCLK rising edge loads device 2 and so on. During the WCLK cycle that a selected device is placed on to the $\overline{PAF}$n bus, the FSYNC output will be HIGH.
FXI	$\overline{PAF}$n Bus Expansion In	LVTTL INPUT	The FXI input is used when Multi-Queue devices are connected in expansion mode and Polled $\overline{PAF}$n bus operation has been selected. FXI of device 'N' connects directly to FXO of device 'N-1'. The FXI receives a token from the previous device in a chain. In single device mode the FXI input should be tied LOW if the $\overline{PAE}$n bus is operated in direct mode. If the $\overline{PAE}$n bus is operated in polled mode the FXI input should be connected to the FXO output of the same device. In expansion mode the FXI of the first device should be tied LOW, when direct mode is selected.
FXO	$\overline{PAF}$n Bus Expansion Out	LVTTL OUTPUT	FXO is an output that is used when Multi-Queue devices are connected in expansion mode and Polled $\overline{PAF}$n bus operation has been selected . FXO of device 'N' connects directly to FXI of device 'N+1'. This pin pulses HIGH when device N places its $\overline{PAF}$ status on to the $\overline{PAF}$n bus with respect to WCLK. This pulse (token) is then passed on to the next device in the chain 'N+1' and on the next WCLK rising edge the first quadrant of device N+1 will be loaded on to the $\overline{PAF}$n bus. This continues through the chain and FXO of the last device is then looped back to FXI of the first device. The FSYNC output of each device in the chain provides synchronization to the user of this looping event.
ID[2:0][1]	Device ID Pins	LVTTL INPUT	For the 4Q Multi-Queue device the WRADD address bus is 5 bits and RDADD address bus is 6 bits wide. When a queue selection takes place the 3 MSB's of this address bus are used to address the specific device (the LSB's are used to address the queue within that device). During write/read operations the 3 MSB's of the address are compared to the device ID pins. The first device in a chain of Multi-Queue's (connected in expansion mode), may be setup as '000', the second as '001' and so on through to device 8 which is '111', however the ID does not have to match the device order. In single device mode these pins should be setup as '000' and the 3 MSB's of the WRADD and RDADD address busses should be tied LOW. The ID[2:0] inputs setup a respective devices ID during master reset. These ID pins must not toggle during any device operation. Note, the device selected as the 'Master' does not have to have the ID of '000'.
IOSEL	IO Select	LVTTL INPUT	This pin is used to select either HSTL or 2.5V LVTTL operation for the I/O. If HSTL or eHSTL I/O are required then IOSEL should be tied LOW. If LVTTL I/O are required then it should be tied HIGH.
IW[1]	Input Width	LVTTL INPUT	IW selects the bus width for the data input bus. If IW is LOW during a Master Reset then the bus width is x18, if HIGH then it is x9.
MAST[1]	Master Device	LVTTL INPUT	The state of this input at Master Reset determines whether a given device (within a chain of devices), is the Master device or a Slave. If this pin is HIGH, the device is the master, if it is LOW then it is a Slave. The master device is the first to take control of all outputs after a master reset, all slave devices go to High-Impedance, preventing bus contention. If a Multi-Queue device is being used in single device mode, this pin must be set HIGH.
$\overline{MRS}$	Master Reset	LVTTL INPUT	A master reset is performed by taking $\overline{MRS}$ from HIGH to LOW, to HIGH. Device programming is required after master reset.
NULL-Q	Null Queue Select	HSTL-LVTTL INPUT	This pin is used on the read port when a Null-Q is required, it is used in conjunction with the RDADD address bus to address the Null-Q.
$\overline{OE}$	Output Enable	LVTTL INPUT	The Output enable signal is an Asynchronous signal used to providethree-state control of the Multi-Queue data output bus, Qout. If a devicehas been configured as a "Master" device, the Qout data outputs will be in aLow Impedance condition if the $\overline{OE}$ input is LOW. If $\overline{OE}$ is HIGH then the Qout data outputs will be in High Impedance. If a device is configured a "Slave" device, then the Qout data outputs will always be in High Impedance until that device has been selected on the Read Port, at which point $\overline{OE}$ provides three-state of that respective device.
$\overline{OV}$	Output Valid Flag	LVTTL OUTPUT	This output flag provides output valid status for the data word present on the Multi-Queue FIFO data output port, Qout. This flag is therefore, 2-stage delayed to match the data output path delay. That is, there is a 2 RCLK cycle delay from the time a given queue is selected for reads, to the time the $\overline{OV}$ flag represents the data in that respective queue. When a selected queue on the read port is read to empty, the $\overline{OV}$ flag will go HIGH, indicating that data on the output bus is not valid. The $\overline{OV}$ flag also has High-Impedance capability, required when multiple devices are used and the $\overline{OV}$ flags are tied together.

PIN DESCRIPTIONS (CONTINUED)

Symbol	Name	I/O TYPE	Description
OW[1]	Output Width	LVTTL INPUT	OW selects the bus width for the data output bus. If OW is LOW during a Master Reset then the bus width is x18, if HIGH then it is x9.
$\overline{PAE}$	Programmable Almost-Empty Flag	LVTTL OUTPUT	This pin provides the Almost-Empty flag status for the FIFO queue that has been selected on the output port for read operations, (selected via RCLK, RDADD and RADEN). This pin is LOW when the selected FIFO queue almost-empty. This flag output may be duplicated on one of the $\overline{PAE}$n bus lines. This flag is synchronized to RCLK.
$\overline{PAE}$n	Programmable Almost-Empty Flag Bus	LVTTL OUTPUT	On the 4Q device the $\overline{PAE}$n bus is 4 bits wide. This output bus provides $\overline{PAE}$ status of all 4 queues, within a selected device. During FIFO read/write operations these outputs provide programmable empty flag status in either director polled mode. The mode of flag operation is determined during master reset via the state of the FM input. This flag bus is capable of High-Impedance state, this is important during expansion of Multi-Queue devices. During direct operation the $\overline{PAE}$n bus is updated to show the $\overline{PAE}$ status of queues within a selected device. Selection is made using RCLK, ESTR and Flag Bus RDADD. During Polled operation the $\overline{PAE}$n bus is loaded with the $\overline{PAE}$ status of Multi-Queue FIFO devices sequentially based on the rising edge of RCLK.
$\overline{PAF}$	Programmable Almost-Full Flag	LVTTL OUTPUT	This pin provides the Almost-Full flag status for the FIFO queue that has been selected on the input port for write operations, (selected via WCLK, WRADD and WADEN). This pin is LOW when the selected FIFO queue is almost-full. This flag output may be duplicated on one of the $\overline{PAF}$n bus lines. This flag is synchronized to WCLK.
$\overline{PAF}$n	Programmable Almost-Full Flag Bus	LVTTL OUTPUT	On the 4Q device the $\overline{PAF}$n bus is 8 bits wide. This output bus provides $\overline{PAF}$ status of all 8 queues, within a selected device. During FIFO read/write operations these outputs provide programmable full flag status, in either direct or polled mode. The mode of flag operation is determined during master reset via the state of the FM input. This flag bus is capable of High-Impedance state, this is important during expansion of Multi-Queue devices. During direct operation the $\overline{PAF}$n bus is updated to show the $\overline{PAF}$ status of a queues within a selected device. Selection is made using WCLK, FSTR, WRADD and WADEN. During Polled operation the $\overline{PAF}$n bus is loaded with the $\overline{PAF}$ status of Multi-Queue FIFO devices sequentially based on the rising edge of WCLK.
PD	Power Down	HSTL INPUT	This input is used to provide additional power savings. When the device I/O is setup for HSTL/eHSTL mode a HIGH on the PD input disables the data inputs on the write port only, providing significant power savings. In LVTTL mode this pin has no operation
$\overline{PRS}$	Partial Reset	LVTTL INPUT	A Partial Reset can be performed on a single queue selected within the Multi-Queue device. Before a Partial Reset can be performed on a queue, that queue must be selected on both the write port and read port 2 clock cycles before the reset is performed. A Partial Reset is then performed by taking $\overline{PRS}$ LOW for one WCLK cycle and one RCLK cycle. The Partial Reset will only reset the read and write pointers to the first memory location, none of the devices configuration will be changed.
Q[17:0] Qout	Data Output Bus	LVTTL OUTPUT	These are the 18 data output pins. Data is read out of the device via these output pins on the rising edge of RCLK provided that $\overline{REN}$ is LOW, $\overline{OE}$ is LOW and the FIFO queue is selected. Due to bus matching not all outputs may be used, any unused outputs should not be connected.
RADEN	Read Address Enable	LVTTL INPUT	The RADEN input is used in conjunction with RCLK and the RDADD address bus to select a queue to be read from. A FIFO queue addressed via the RDADD bus is selected on the rising edge of RCLK provided that RADEN is HIGH. RADEN cannot be HIGH for the same RCLK cycle as ESTR.
RCLK	Read Clock	LVTTL INPUT	When enabled by $\overline{REN}$, the rising edge of RCLK reads data from the selected FIFO queue via the output bus Qout. The FIFO queue to be read is selected via the RDADD address bus and a rising edge of RCLK while RADEN is HIGH. A rising edge of RCLK in conjunction with ESTR and RDADD will also select the device to be placed on the $\overline{PAE}$n bus during direct flag operation. During polled flag operation the $\overline{PAE}$n bus is cycled with respect to RCLK and the ESYNC signal is synchronized to RCLK. The $\overline{PAE}$ and $\overline{OV}$ outputs are all synchronized to RCLK. During device expansion the EXO and EXI signals are based on RCLK. RCLK must be continuous and free-running.
RDADD [6:0]	Read Address Bus	LVTTL INPUT	For the 8Q device the RDADD bus is 7 bits. The RDADD bus is a dual purpose address bus. The first function of RDADD is to select a FIFO queue to be read from. The least significant 3 bits of the bus, RDADD[2:0] are used to address 1 of 8 possible queues within a Multi-Queue device. Address pin, RDADD[3] provides the user with a Null-Q address. If the user does not wish to address one of the 8 queues, a Null-Q can be addressed using this pin. The Null-Q operation is discussed in more detail later. The most

PIN DESCRIPTIONS (CONTINUED)

Symbol	Name	I/O TYPE	Description
RDADD [6:0] (Continued)	Read Address Bus	LVTTL INPUT	significant 3 bits, RDADD[6:4] are used to select 1 of 8 possible Multi-Queue devices that may be connected in expansion mode. These 3 MSB's will address a device with the matching ID code. The address present on the RDADD bus will be selected on a rising edge of RCLK provided that RADEN is HIGH, (note, that data can be placed on to the Qout bus, read from the previously selected FIFO queue on this RCLK edge). On the next rising RCLK edge after a read queue select, a data word from the previous queue will be placed onto the outputs, Qout, regardless of the $\overline{REN}$ input. Two RCLK rising edges after read queue select, data will be placed on to the Qout outputs from the newly selected queue, regardless of $\overline{REN}$ due to the first word fall through effect. The second function of the RDADD bus is to select the device of FIFO queues to be loaded on to the $\overline{PAE}$n bus during strobed flag mode. The most significant 3 bits, RDADD[6:4] are again used to select 1 of 8 possible Multi-Queue devices that may be connected in expansion mode. Address bits RDADD[3:0] are don't care during device selection. The device address present on the RDADD bus will be selected on the rising edge of RCLK provided that ESTR is HIGH, (note, that data can be placed on to the Qout bus, read from the previously selected FIFO Q on this RCLK edge). Please refer to Table 2 for details on RDADD bus.
$\overline{REN}$	Read Enable	LVTTL INPUT	The $\overline{REN}$ input enables read operations from a selected FIFO queue based on a rising edge of RCLK. A queue to be read from can be selected via RCLK, RADEN and the RDADD address bus regardless of the state of $\overline{REN}$. Data from a newly selected queue will be available on the Qout output bus on the second RCLK cycle after queue selection regardless of $\overline{REN}$ due to the FWFT operation. A read enable is not required to cycle the $\overline{PAE}$n bus (in polled mode) or to select the device , (in direct mode).
SCLK	Serial Clock	LVTTL INPUT	If serial programming of the Multi-Queue device has been selected during master reset, the SCLK input clocks the serial data through the Multi-Queue device. Data setup on the SI input is loaded into the device on the rising edge of SCLK provided that $\overline{SENI}$ is enabled, LOW. When expansion of devices is performed the SCLK of all devices should be connected to the same source.
$\overline{SENI}$	Serial Input Enable	LVTTL INPUT	During serial programming of a Multi-Queue device, data loaded onto the SI input will be clocked into the part (via a rising edge of SCLK), provided the $\overline{SENI}$ input of that device is LOW. If multiple devices are cascaded, the $\overline{SENI}$ input should be connected to the $\overline{SENO}$ output of the previous device. So when serial loading of a given device is complete, its $\overline{SENO}$ output goes LOW, allowing the next device in the chain to be programmed ($\overline{SENO}$ will follow $\overline{SENI}$ of a given device once that device is programmed). The $\overline{SENI}$ input of the master device (or single device), should be controlled by the user.
$\overline{SENO}$	Serial Output Enable	LVTTL OUTPUT	This output is used to indicate that serial programming or default programming of the Multi-Queue device has been completed. $\overline{SENO}$ follows $\overline{SENI}$ once programming of a device is complete. Therefore, $\overline{SENO}$ will go LOW after programming provided $\overline{SENI}$ is LOW, once $\overline{SENI}$ is taken HIGH again, $\overline{SENO}$ will also go HIGH. When the $\overline{SENO}$ output goes LOW, the device is ready to begin normal read/write operations. If multiple devices are cascaded and serial programming of the devices will be used, the $\overline{SENO}$ output should be connected to the $\overline{SENI}$ input of the next device in the chain. When serial programming of the first device is complete, $\overline{SENO}$ will go LOW, thereby taking the $\overline{SENI}$ input of the next device LOW and so on throughout the chain. When a given device in the chain is fully programmed the $\overline{SENO}$ output essentially follows the $\overline{SENI}$ input. The user should monitor the $\overline{SENO}$ output of the final device in the chain. When this output goes LOW, serial loading of all devices has been completed.
SI	Serial In	LVTTL INPUT	During serial programming this pin is loaded with the serial data that will configure the Multi-Queue devices. Data present on SI will be loaded on a rising edge of SCLK provided that $\overline{SENI}$ is LOW. In expansion mode the serial data input is loaded into the first device in a chain. When that device is loaded and its $\overline{SENO}$ has gone LOW, the data present on SI will be directly output to the SO output. The SO pin of the first device connects to the SI pin of the second and so on. The Multi-Queue device setup registers are shift registers.
SO	Serial Out	LVTTL OUTPUT	This output is used in expansion mode and allows serial data to be passed through devices in the chain to complete programming of all devices. The SI of a device connects to SO of the previous device in the chain. The SO of the final device in a chain should not be connected.
TCK	JTAG Clock	LVTTL INPUT	Clock input for JTAG function. TMS and TDI are sampled on the rising edge of TCK. TDO is output on the falling edge of TCK.
TDI	Test Data Input	LVTTL INPUT	During JTAG boundary scan operation test data is serially loaded via TDI on the rising edge of TCK. This is also the data for the Instruction Register, JTAG ID Register and Bypass Register.

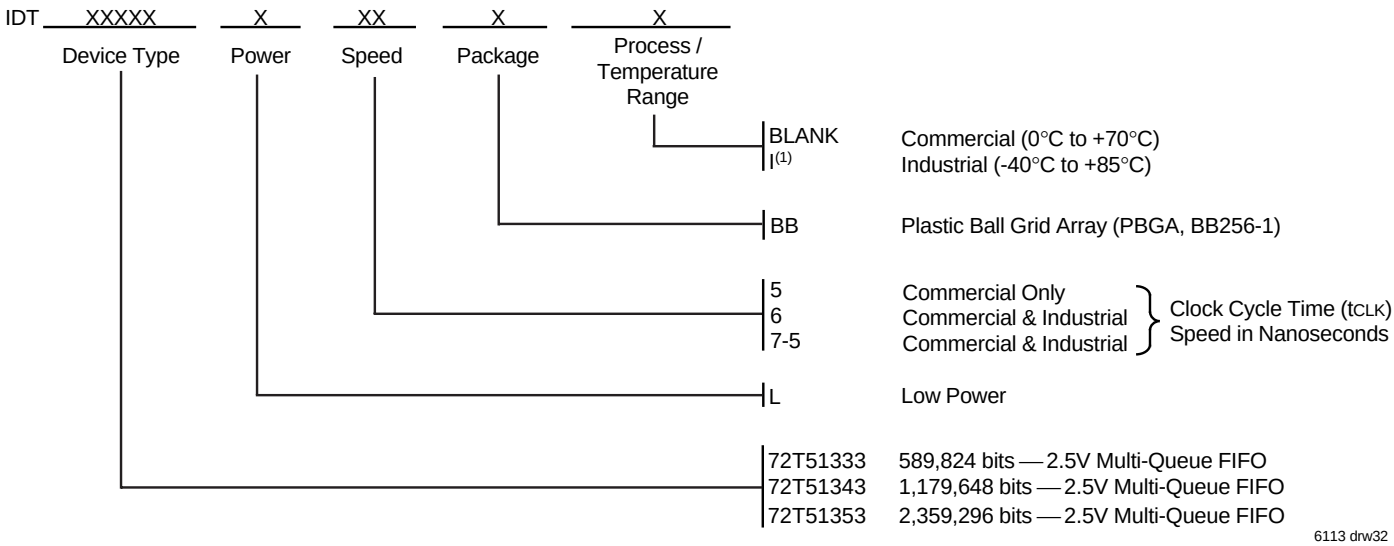
PIN DESCRIPTIONS (CONTINUED)

Symbol	Name	I/O TYPE	Description
TDO	Test Data Output	LVTTL INPUT	During JTAG boundary scan operation test data is serially output via TDO on the falling edge of TCK. This output is in High-Impedance except when shifting data while in SHIFT-DR and SHIFT-IR controller states.
TMS	JTAG Mode Select	LVTTL INPUT	TMS is a serial input pin. Bits are serially loaded on the rising edge of TCK, which selects 1 of 5 modes of operation for the JTAG boundary scan.
$\overline{TRST}$	JTAG Reset	LVTTL INPUT	$\overline{TRST}$ is the asynchronous reset pin for the JTAG controller. If the JTAG port is not utilized, $\overline{TRST}$ should be tied to GND.
WADEN	Write Address Enable	LVTTL INPUT	The WADEN input is used in conjunction with WCLK and the WRADD address bus to select a queue to be written in to. A FIFO queue addressed via the WRADD bus is selected on the rising edge of WCLK provided that WADEN is HIGH. WADEN cannot be HIGH for the same WCLK cycle as FSTR.
WCLK	Write Clock	LVTTL INPUT	When enabled by $\overline{WEN}$, the rising edge of WCLK writes data into the selected FIFO queue via the input bus, Din. The FIFO queue to be written to is selected via the WRADD address bus and a rising edge of WCLK while WADEN is HIGH. A rising edge of WCLK in conjunction with FSTR and WRADD will also select the device to be placed on the $\overline{PAF}$n bus during direct flag operation. During polled flag operation the $\overline{PAF}$n bus is cycled with respect to WCLK and the FSYNC signal is synchronized to WCLK. The $\overline{PAF}$n, $\overline{PAF}$ and $\overline{FF}$ outputs are all synchronized to WCLK. During device expansion the FXO and FXI signals are based on WCLK. The WCLK must be continuous and free-running.
$\overline{WEN}$	Write Enable	LVTTL INPUT	The $\overline{WEN}$ input enables write operations to a selected FIFO queue based on a rising edge of WCLK. A queue to be written to can be selected via WCLK, WADEN and the WRADD address bus regardless of the state of $\overline{WEN}$. Data present on Din can be written to a newly selected queue on the second WCLK cycle after queue selection provided that $\overline{WEN}$ is LOW. A write enable is not required to cycle the $\overline{PAF}$n bus (in polled mode) or to select the device , (in direct mode).
WRADD [5:0]	Write Address Bus	LVTTL INPUT	For the 8Q device the WRADD bus is 6 bits. The WRADD bus is a dual purpose address bus. The first function of WRADD is to select a FIFO queue to be written to. The least significant 3 bits of the bus, WRADD[2:0] are used to address 1 of 8 possible queues within a Multi-Queue device. The most significant 3 bits, WRADD[5:3] are used to select 1 of 8 possible Multi-Queue devices that may be connected in expansion mode. These 3 MSB's will address a device with the matching ID code. The address present on the WRADD bus will be selected on a rising edge of WCLK provided that WADEN is HIGH, (note, that data present on the Din bus can be written into the previously selected FIFO queue on this WCLK edge and on the next rising WCLK also, providing that $\overline{WEN}$ is LOW). Two WCLK rising edges after write queue select, data can be written into the newly selected queue. The second function of the WRADD bus is to select the device of FIFO queues to be loaded on to the $\overline{PAF}$n bus during strobed flag mode. The most significant 3 bits, WRADD[6:3] are again used to select 1 of 8 possible Multi-Queue devices that may be connected in expansion mode. Address bits WRADD[2:0] are don't care during device selection. The device address present on the WRADD bus will be selected on the rising edge of WCLK provided that FSTR is HIGH, (note, that data can be written into the previously selected FIFO queue on this WCLK edge). Please refer to Table 1 for details on the WRADD bus.
V_{CC}	+2.5V Supply	Power	These are V_{CC} power supply pins and must all be connected to a +2.5V supply rail.
V_{DDQ}	O/P Rail Voltage	Power	These pins must be tied to the desired output rail voltage. For LVTTL I/O these pins must be connected to +2.5V, for HSTL these pins must be connected to +1.5V and for eHSTL these pins must be connected to +1.8V.
GND	Ground Pin	Power	These are Ground pins and must all be connected to the GND supply rail.
Vref	Reference Voltage	HSTL INPUT	This is a Voltage Reference input and must be connected to a voltage level determined from the table "Recommended DC Operating Conditions". The input provides the reference level for HSTL/eHSTL inputs. For LVTTL I/O mode this input should be tied to GND.

NOTE:

1. Inputs should not change after Master Reset.

ORDERING INFORMATION



NOTE:
1. Industrial temperature range product for 6ns and 7-5ns speed grades are available as a standard device. All other speed grades available by special order.

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