Ordering number : EN4627

CMOS LSI

LC74FCT16425T, 74FCT162245T

Fast 16-Bit CMOS Bidirectional Transceiver

Overview

The LC74FCT16245T and LC74FCT162245T 16-bit transceivers are fabricated in an advanced two-metal-layer CMOS technology. These fast, low-power transceivers are optimal for synchronous communication between two buses, referred to as the A and B busses. The directionality and output enable control in these products is designed to allow them to be used as either two independent 8-bit transceivers or as a single 16-bit transceiver. The direction control pin (× DIR) controls the data flow direction and the output enable pin (× $\overline{OE}$) disables directionality control and disables both ports.

The LC74FCT16245T is optimal for driving large-capacitance loads and low-impedance loads.

The LC74FCT162245T provides a balanced output drive function that incorporates current limiting resistors. These minimize ground bounce and undershoot, and limit the output fall time. As a result, external series terminating resistors are no longer required.

The LC74FCT162245T is a plug-in replacement for the LC74FCT16245T in on-board interface applications.

Features

- 0.8 µm CMOS technology
- Fast, low-power CMOS replacement products for use in ABT function applications
- ESD tolerance > 2000 V; MIL-STD-883 (when tested with the 3015 method)
- ESD tolerance > 200 V; For a machine model with C = 200 pF and R = 0 Ω
- Bidirectional data transfer
- 20 mil center SQFP
- Expanded temperature range: –40 to +85°C
- V_{CC} = 5 V ± 10%

LC74FCT16245T Features

- High drive output levels (I_{OH}: –32 mA, I_{OL}: 40 mA)

LC74FCT162245T Features

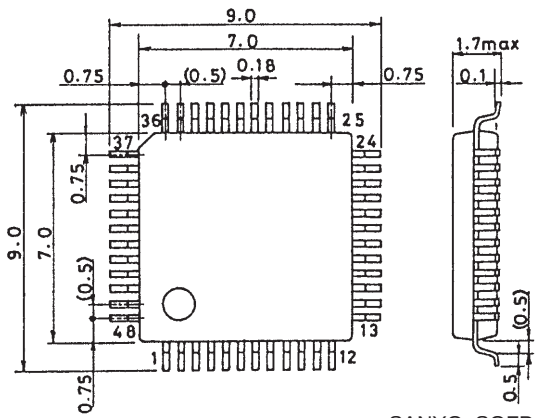
- Balanced output drive: ±24 mA
- Reduced system switching noise

Package Dimensions

unit: mm

3163A-SQFP48

[LC74FCT16245T, 74FCT162245T]



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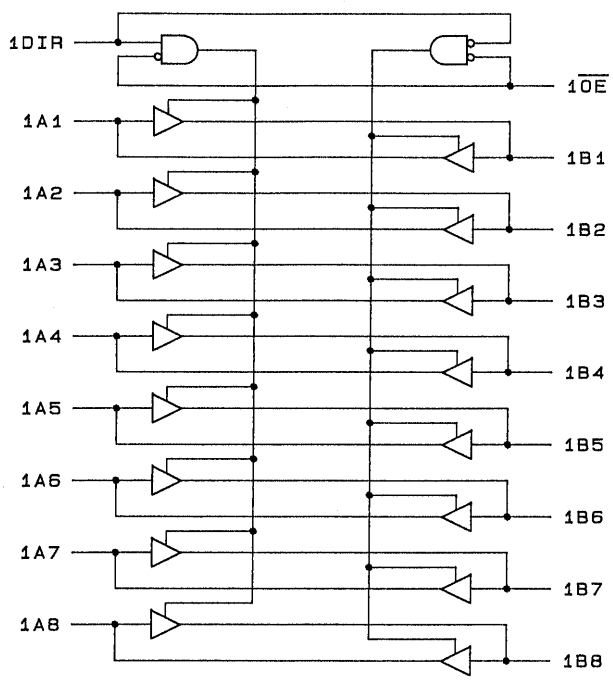
Function Block Diagram



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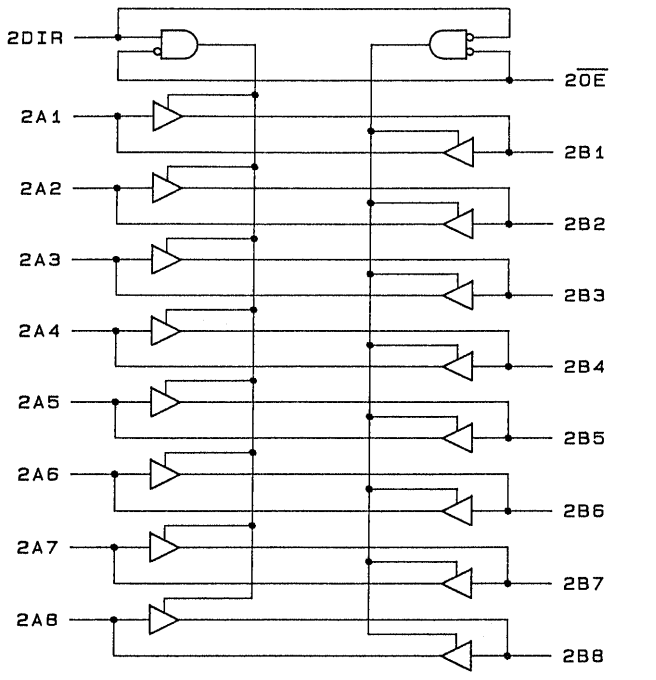

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Pin Functions

Pin	Function
× $\overline{OE}$	Output enable input (active low)
× DIR	Direction control input
× AX	A side input or three-state output
× BX	B side input or three-state output

Specifications

Absolute Maximum Ratings*1

Parameter	Symbol	Conditions	Ratings	Unit
Pin voltage referenced to GND	V_{TERM}*2		–0.5 to +7.0	V
Pin voltage referenced to GND	V_{TERM}*3		–0.5 to V_{CC} + 0.5	V
Operating temperature	Topr		–40 to +85	°C
Temperature when bias is applied	T_{BIAS}		–55 to +125	°C
Storage temperature	Tstg		–55 to +125	°C
Power dissipation	P_T		*4	W
DC output current	I_{OUT}		–60 to +60	mA

Note: 1. Applying stresses in excess of the absolute maximum ratings may permanently damage the device. The values specified here are stress ratings only, and do not refer to operation under conditions outside either these conditions or the operating conditions. Operating for extended periods at the absolute maximum ratings may adversely influence device reliability. Unless otherwise specified, pin voltages must not exceed V_{CC} + 0.5 V.
2. All pins except the FCT162xxxT output and I/O pins
3. All FCT162xxxT output and I/O pins
4. See Figure 1.

Function Truth Table*

Input		Output
× $\overline{OE}$	× DIR	
L	L	Bus B data output to bus A
L	H	Bus A data output to bus B
H	X	High-impedance state.

Note: * H = High level
L = Low level
X = Don't care

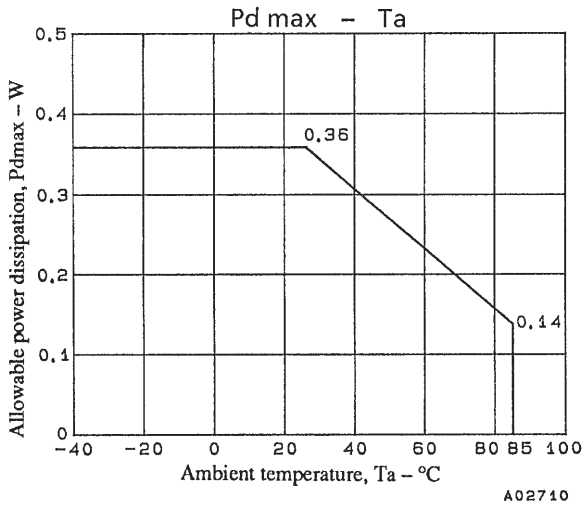


Figure 1

Capacitances (Ta = 25°C)

Parameter*	Symbol	Conditions	min	typ	max	Unit
Input capacitance	C_{IN}			5.5	8.0	pF
I/O capacitance	$C_{I/O}$			4.5	6.0	pF

Note: * These capacitance values are logic values, and are not tested.

DC Electrical Characteristics in the Operating Ranges

The following conditions apply unless otherwise specified.

Ta = –40 to +85°C, V_{CC} = +5.0 V ± 10%

Parameter	Symbol	Conditions*		min	typ	max	Unit
Input high level voltage	V_{IH}	Logic high level guaranteed		2.0			V
Input low level voltage	V_{IL}	Logic low level guaranteed				0.8	V
Input high level current (input pins)	I_{IH}	V_{CC} = max	$V_I = V_{CC}$			±5	µA
Input high level current (I/O pins)						±15	
Input low level current (input pins)	I_{IL}		V_I = GND			±5	
Input low level current (I/O pins)						±15	
Quiescent current	I_{CCL}, I_{CCH}, I_{CCZ}	V_{CC} = max, V_{IN} = GND or V_{CC}			0.05	1.5	mA

Note: * Values stipulated in the electrical characteristics for the corresponding product must be used for the test conditions for the maximum and minimum values.

LC74FCT16245T Output Drive Characteristics

Parameter	Symbol	Conditions*1		min	typ*2	max	Unit
Output high level voltage	V_{OH}	V_{CC} = min, $V_{IN} = V_{IH}$ or V_{IL}	I_{OH} = –3 mA	2.5	3.5		V
			I_{OH} = –15 mA	2.4	3.5		V
			I_{OH} = –32 mA*3	2.0	3.0		V
Output low level voltage	V_{OL}	V_{CC} = min, $V_{IN} = V_{IH}$ or V_{IL}	I_{OL} = 40 mA		0.2	0.55	V

Note: 1. Values stipulated in the electrical characteristics for the corresponding product must be used for the test conditions for the maximum and minimum values.
2. Typical values are values for V_{CC} = 5.0 V, and an ambient temperature of +25°C.
3. The test time must not exceed 1 second.

LC74FCT162245T Output Drive Characteristics

Parameter	Symbol	Conditions*1		min	typ*2	max	Unit
Output low level current	I_{ODL}	V_{CC} = 5 V, $V_{IN} = V_{IH}$ or V_{IL}, V_{OUT} = 1.5 V*3		60	115	150	mA
Output high level current	I_{ODH}	V_{CC} = 5 V, $V_{IN} = V_{IH}$ or V_{IL}, V_{OUT} = 1.5 V*3		–60	–115	–150	mA
Output high level voltage	V_{OH}	V_{CC} = min, $V_{IN} = V_{IH}$ or V_{IL}	I_{OH} = –24 mA*4	2.4	3.3		V
Output low level voltage	V_{OL}	V_{CC} = min, $V_{IN} = V_{IH}$ or V_{IL}	I_{OL} = 24 mA		0.3	0.55	V

Note: 1. Values stipulated in the electrical characteristics for the corresponding product must be used for the test conditions for the maximum and minimum values.
2. Typical values are values for V_{CC} = 5.0 V, and an ambient temperature of +25°C.
3. Do not test more than one output at a time. The test time must not exceed 1 second.
4. The test time must not exceed 1 second.

Power Supply Current Characteristics

Parameter	Symbol	Conditions[*1]		min	typ[*2]	max	Unit
Quiescent current high-level TTL inputs	ΔI_{CC}	V_{CC} = max, V_{IN} = 3.4 V[*3]			0.5	1.5	µA
Operating supply current[*4]	I_{CCD}	V_{CC} = max, outputs open, × $\overline{OE}$ = × DIR = GND, toggling a single input, 50% duty cycle	V_{IN} = V_{CC}, V_{IN} = GND		100	160	µA/MHz
Total supply current[*6]	I_C	V_{CC} = max, outputs open, fi = 10 MHz, × $\overline{OE}$ = × DIR = GND, toggling a single bit, 50% duty cycle	V_{IN} = V_{CC}, V_{IN} = GND		0.7	2.5	mA
			V_{IN} = 3.4 V, V_{IN} = GND		0.9	3.3	
		V_{CC} = max, outputs open, fi = 2.5 MHz, × $\overline{OE}$ = × DIR = GND, toggling a 16 bits, 50% duty cycle	V_{IN} = V_{CC}, V_{IN} = GND		2.5	5.5[*5]	
			V_{IN} = 3.4 V, V_{IN} = GND		6.5	17.5[*5]	

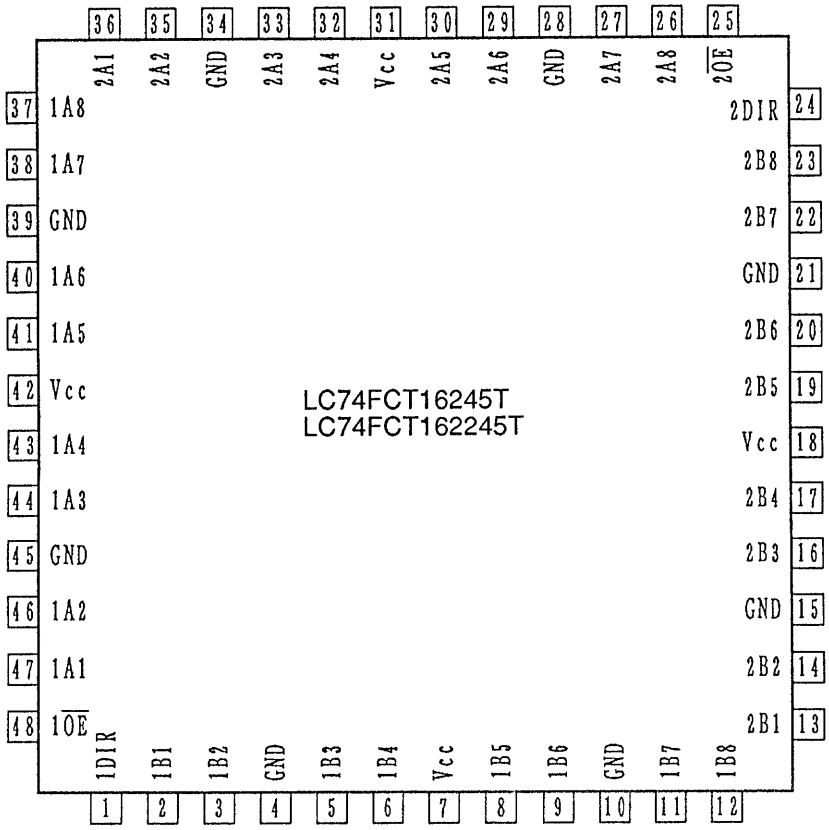
Note: 1. Values stipulated in the electrical characteristics for the corresponding product must be used for the test conditions for the maximum and minimum values.
2. Typical values are values for V_{CC} = 5.0 V, and at an ambient temperature of +25°C.
3. For the TTL drive inputs (V_{IN} = 3.4 V), connect all the other inputs to V_{CC} or GND.
4. Although this parameter cannot be directly measured, it is provided for calculating the total power dissipation.
5. The values for these conditions are values with respect to the I_{CC} rating. Although these values are guaranteed, they are not tested.
6. $I_C + I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
$I_C + I_{CC} + \Delta I_{CC}, D_H N_T + I_{CCD} (f_{CP} N_{CP}/2 + fiNi)$
I_{CC} = Quiescent current (I_{CCL}, I_{CCH}, and I_{CCZ})
ΔI_{CC} = Supply current for the high-level TTL inputs (V_{IN} = 3.4 V)
D_H = Duty cycle for the high-level TTL inputs
N_T = The number of TTL inputs in D_H
I_{CCD} = Operating current due to input transition pairs (HLH or LHL)
f_{CP} = Clock frequency for register devices (zero for non-register devices)
N_{CP} = The number of clocks input in f_{CP}
fi = Input frequency
Ni = The number of inputs in fi.

LC74FCT16245T/162245T Switching Characteristics in the Operating Ranges

Parameter	Symbol	Conditions[*1]	min	typ	max	Unit
Transmission delay (From A to B or from B to A)	t_{PLH}, t_{PHL}	C_L = 50 pF, R_L = 500 Ω	1.5		7.0	ns
Output enable time (From × $\overline{OE}$ to A or B)	t_{PZH}[*1], t_{PZL}[*1]		1.5		12.0	ns
Output disable time (From × $\overline{OE}$ to A or B)	t_{PHZ}[*1], t_{PLZ}[*1]		1.5		7.5	ns
Output enable time (From × DIRS to A or B[*3])	t_{PZH}[*2], t_{PZL}[*2]		1.5		9.5	ns
Output disable time (From × DIRS to A or B[*3])	t_{PHZ}[*2], t_{PLZ}[*2]		1.5		7.5	ns
Output skew[*4]	t_{SK} (O)				0.5	ns

Note: 1. See the figures for the test circuit and waveforms.
2. Although the minimum values are guaranteed, the transmission delay is not tested.
3. Although these items are guaranteed, they are not tested.
4. The skew between two outputs in the same package switched in the same direction. This parameter is a design guarantee.

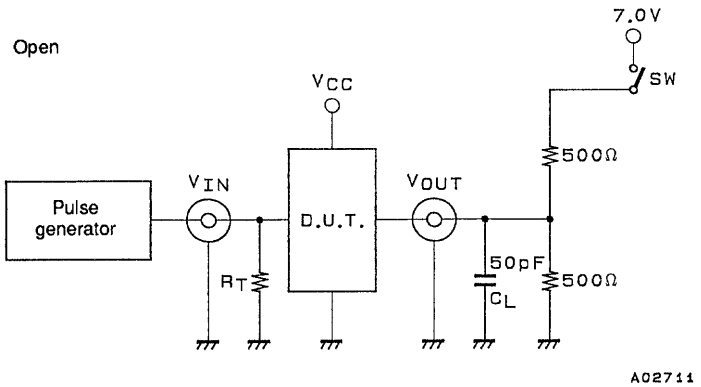
Pin Assignment



Top view

Test Circuit and Waveform Diagrams

Test Circuit for All Outputs

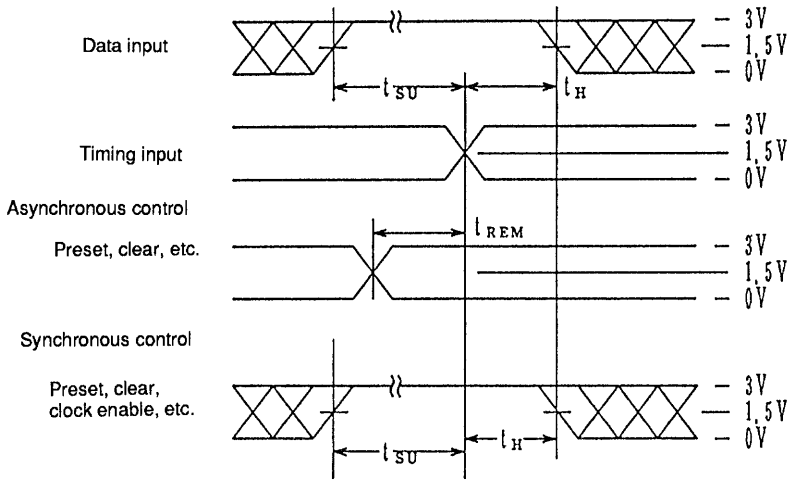


Switch Positions

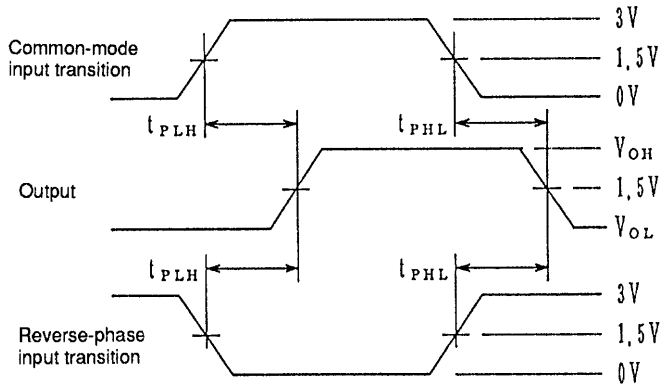
Test	Switch
Open drain, Disable low level, Enable low level	Closed
All other tests	Open

Definitions: C_L = Load capacitance: including the jig and probe capacitances
R_T = Terminating resistance: equivalent to the pulse generator's Zout.

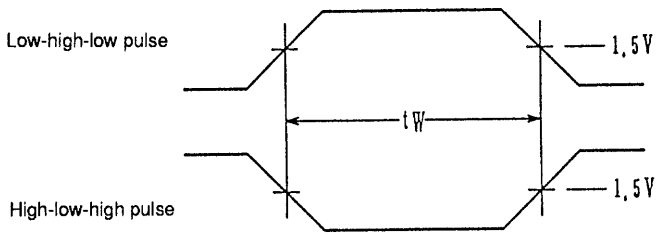
Setup, Hold, and Release Timing



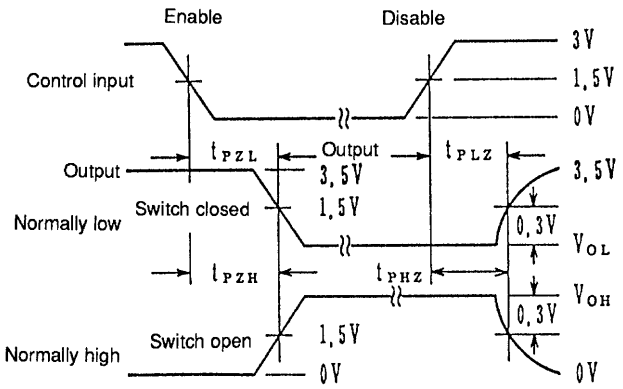
Transmission Delay



Pulse Width



Enable and Disable Timing



Note: 1. These diagrams are for the input enable low level and the input control disable high level cases.
2. Pulse generator setup for all pulses: rate ≤ 1.0 MHz, Zo ≤ 50 Ω, t_f ≤ 2.5 ns, t_r ≤ 2.5 ns