

## 74ACQ574 • 74ACTQ574

### Quiet Series™ Octal D-Type Flip-Flop with 3-STATE Outputs

#### General Description

The ACQ/ACTQ574 is a high-speed, low-power octal D-type flip-flop with a buffered Common Clock (CP) and a buffered common Output Enable ( $\overline{OE}$ ). The information presented to the D inputs is stored in the flip-flops on the LOW-to-HIGH clock (CP) transition.

ACQ/ACTQ574 utilizes FACT Quiet Series™ technology to guarantee quiet output switching and improve dynamic threshold performance. FACT Quiet Series features GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance.

The ACQ/ACTQ574 is functionally identical to the ACTQ374 but with different pin-out.

#### Features

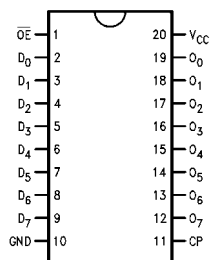
- $I_{CC}$  and  $I_{OZ}$  reduced by 50%
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin skew AC performance
- Inputs and outputs on opposite sides of the package allowing easy interface with microprocessors
- Functionally identical to the ACQ/ACTQ374
- 3-STATE outputs drive bus lines or buffer memory address registers
- Outputs source/sink 24 mA
- Faster prop delays than the standard AC/ACT574

#### Ordering Code:

Order Number	Package Number	Package Description
74ACQ574SC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide Body
74ACQ574SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74ACQ574PC	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
74ACTQ574SC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide Body
74ACTQ574SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74ACTQ574PC	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Device also available in Tape and Reel. Specify by appending suffix "X" to the ordering code.

#### Connection Diagram

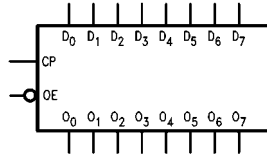


#### Pin Descriptions

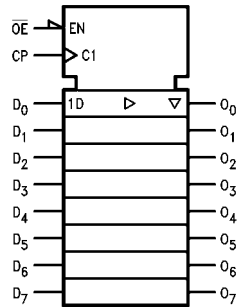
Pin Names	Description
$D_0$ – $D_7$	Data Inputs
CP	Clock Pulse Input
$\overline{OE}$	3-STATE Output Enable Input
$O_0$ – $O_7$	3-STATE Outputs

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### Logic Symbols



IEEE/IEC



### Functional Description

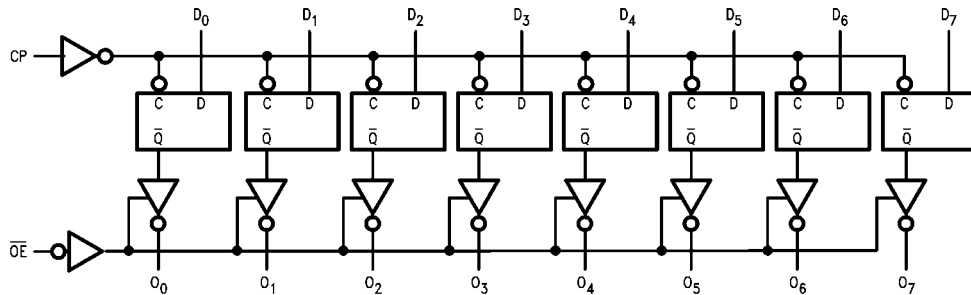
The ACQ/ACTQ574 consists of eight edge-triggered flip-flops with individual D-type inputs and 3-STATE true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D-type inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable ( $\overline{OE}$ ) LOW, the contents of the eight flip-flops are available at the outputs. When  $\overline{OE}$  is HIGH, the outputs go to the high impedance state. Operation of the  $\overline{OE}$  input does not affect the state of the flip-flops.

### Function Table

Inputs			Internal	Outputs	Function
$\overline{OE}$	CP	D	Q	$O_N$	
H	H	L	NC	Z	Hold
H	H	H	NC	Z	Hold
H	↗	L	L	Z	Load
H	↗	H	H	Z	Load
L	↗	L	L	L	Data Available
L	↗	H	H	H	Data Available
L	H	L	NC	NC	No Change in Data
L	H	H	NC	NC	No Change in Data

H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Immaterial  
 Z = High Impedance  
 ↗ = LOW-to-HIGH Transition  
 NC = No Change

### Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

**Absolute Maximum Ratings**(Note 1)

Supply Voltage ( $V_{CC}$ )	-0.5V to +7.0V
DC Input Diode Current ( $I_{IK}$ )	
$V_I = -0.5V$	-20 mA
$V_I = V_{CC} + 0.5V$	+20 mA
DC Input Voltage ( $V_I$ )	-0.5V to $V_{CC} + 0.5V$
DC Output Diode Current ( $I_{OK}$ )	
$V_O = -0.5V$	-20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage ( $V_O$ )	-0.5V to $V_{CC} + 0.5V$
DC Output Source or Sink Current ( $I_O$ )	$\pm 50$ mA
DC $V_{CC}$ or Ground Current per Output Pin ( $I_{CC}$ or $I_{GND}$ )	$\pm 50$ mA
Storage Temperature ( $T_{STG}$ )	-65°C to +150°C
DC Latch-Up Source or Sink Current	$\pm 300$ mA
Junction Temperature ( $T_J$ )	
PDIP	140°C

**Recommended Operating Conditions**

Supply Voltage ( $V_{CC}$ )	
ACQ	2.0V to 6.0V
ACTQ	4.5V to 5.5V
Input Voltage ( $V_I$ )	0V to $V_{CC}$
Output Voltage ( $V_O$ )	0V to $V_{CC}$
Operating Temperature ( $T_A$ )	-40°C to +85°C
Minimum Input Edge Rate $\Delta V/\Delta t$	
ACQ Devices	
$V_{IN}$ from 30% to 70% of $V_{CC}$	
$V_{CC}$ @ 3.0V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate $\Delta V/\Delta t$	
ACTQ Devices	
$V_{IN}$ from 0.8V to 2.0V	
$V_{CC}$ @ 4.5V, 5.5V	125 mV/ns

**Note 1:** Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation of FACT™ circuits outside databook specifications.

**DC Electrical Characteristics for ACQ**

Symbol	Parameter	$V_{CC}$ (V)	$T_A = +25^\circ\text{C}$		$T_A = -40^\circ\text{C to } +85^\circ\text{C}$	Units	Conditions
			Typ	Guaranteed Limits			
$V_{IH}$	Minimum HIGH Level Input Voltage	3.0	1.5	2.1	2.1	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
		4.5	2.25	3.15	3.15		
		5.5	2.75	3.85	3.85		
$V_{IL}$	Maximum LOW Level Input Voltage	3.0	1.5	0.9	0.9	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
		4.5	2.25	1.35	1.35		
		5.5	2.75	1.65	1.65		
$V_{OH}$	Minimum HIGH Level Output Voltage	3.0	2.99	2.9	2.9	V	$I_{OUT} = -50 \mu A$
		4.5	4.49	4.4	4.4		
		5.5	5.49	5.4	5.4		
	3.0		2.56	2.46	V	$V_{IN} = V_{IL}$ or $V_{IH}$ $I_{OH} = -12 \text{ mA}$ $I_{OH} = -24 \text{ mA}$ $I_{OH} = -24 \text{ mA (Note 2)}$	
	4.5		3.86	3.76			
5.5		4.86	4.76				
$V_{OL}$	Maximum LOW Level Output Voltage	3.0	0.002	0.1	0.1	V	$I_{OUT} = 50 \mu A$
		4.5	0.001	0.1	0.1		
		5.5	0.001	0.1	0.1		
	3.0		0.36	0.44	V	$V_{IN} = V_{IL}$ or $V_{IH}$ $I_{OL} = 12 \text{ mA}$ $I_{OL} = 24 \text{ mA}$ $I_{OL} = 24 \text{ mA (Note 2)}$	
	4.5		0.36	0.44			
5.5		0.36	0.44				
$I_{IN}$ (Note 4)	Maximum Input Leakage Current	5.5		$\pm 0.1$	$\pm 1.0$	$\mu A$	$V_I = V_{CC}, GND$
$I_{OLD}$	Minimum Dynamic	5.5			75	mA	$V_{OLD} = 1.65V \text{ Max}$
$I_{OHD}$	Output Current (Note 3)	5.5			-75	mA	$V_{OHD} = 3.85V \text{ Min}$
$I_{CC}$ (Note 4)	Maximum Quiescent Supply Current	5.5		4.0	40.0	$\mu A$	$V_{IN} = V_{CC}$ or GND
$I_{OZ}$	Maximum 3-STATE Leakage Current	5.5		$\pm 0.25$	$\pm 2.5$	$\mu A$	$V_I$ (OE) = $V_{IL}, V_{IH}$ $V_I = V_{CC}, GND$ $V_O = V_{CC}, GND$

DC Electrical Characteristics for ACQ (Continued)								
Symbol	Parameter	V <sub>CC</sub> (V)	T <sub>A</sub> = +25°C		T <sub>A</sub> = -40°C to +85°C	Units	Conditions	
			Typ	Guaranteed Limits				
V <sub>OLP</sub>	Quiet Output Maximum Dynamic V <sub>OL</sub>	5.0	1.1	1.5		V	Figure 1, Figure 2 (Note 5)(Note 6)	
V <sub>OLV</sub>	Quiet Output Minimum Dynamic V <sub>OL</sub>	5.0	-0.6	-1.2		V	Figure 1, Figure 2 (Note 5)(Note 6)	
V <sub>IHD</sub>	Minimum HIGH Level Dynamic Input Voltage	5.0	3.1	3.5		V	(Note 5)(Note 7)	
V <sub>ILD</sub>	Maximum LOW Level Dynamic Input Voltage	5.0	1.9	1.5		V	(Note 5)(Note 7)	
<p><b>Note 2:</b> All outputs loaded; thresholds on input associated with output under test.</p> <p><b>Note 3:</b> Maximum test duration 2.0 ms, one output loaded at a time.</p> <p><b>Note 4:</b> I<sub>IN</sub> and I<sub>CC</sub> @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V<sub>CC</sub>.</p> <p><b>Note 5:</b> DIP package.</p> <p><b>Note 6:</b> Max number of outputs defined as (n). Data inputs are driven 0V to 5V. One output @ GND.</p> <p><b>Note 7:</b> Maximum number of data inputs (n) switching. (n-1) inputs switching 0V to 5V (ACQ). Input-under-test switching: 5V to threshold (V<sub>ILD</sub>), 0V to threshold (V<sub>IHD</sub>). f = 1 MHz.</p>								
DC Electrical Characteristics for ACTQ								
Symbol	Parameter	V <sub>CC</sub> (V)	T <sub>A</sub> = +25°C		T <sub>A</sub> = -40°C to +85°C	Units	Conditions	
			Typ	Guaranteed Limits				
V <sub>IH</sub>	Minimum HIGH Level Input Voltage	4.5	1.5	2.0	2.0	V	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> - 0.1V	
		5.5	1.5	2.0	2.0			
V <sub>IL</sub>	Maximum LOW Level Input Voltage	4.5	1.5	0.8	0.8	V	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> - 0.1V	
		5.5	1.5	0.8	0.8			
V <sub>OH</sub>	Minimum HIGH Level Output Voltage	4.5	4.49	4.4	4.4	V	I <sub>OUT</sub> = -50 μA	
		5.5	5.49	5.4	5.4			
			4.5		3.85	3.76	V	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> I <sub>OH</sub> = -24 mA I <sub>OH</sub> = -24 mA (Note 8)
			5.5		4.86	4.76		
V <sub>OL</sub>	Maximum LOW Level Output Voltage	4.5	0.001	0.1	0.1	V	I <sub>OUT</sub> = 50 μA	
		5.5	0.001	0.1	0.1			
			4.5		0.36	0.44	V	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> I <sub>OL</sub> = 24 mA I <sub>OL</sub> = 24 mA (Note 8)
			5.5		0.36	0.44		
I <sub>IN</sub>	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V <sub>I</sub> = V <sub>CC</sub> , GND	
I <sub>OZ</sub>	Maximum 3-STATE Leakage Current	5.5		±0.25	±2.5	μA	V <sub>I</sub> = V <sub>IL</sub> , V <sub>IH</sub> V <sub>O</sub> = V <sub>CC</sub> , GND	
I <sub>CCT</sub>	Maximum I <sub>CC</sub> /Input	5.5	0.6		1.5	mA	V <sub>I</sub> = V <sub>CC</sub> - 2.1V	
I <sub>OLD</sub>	Minimum Dynamic	5.5			75	mA	V <sub>OLD</sub> = 1.65V Max	
I <sub>OHD</sub>	Output Current (Note 9)	5.5			-75	mA	V <sub>OHD</sub> = 3.85V Min	
I <sub>CC</sub>	Maximum Quiescent Supply Current	5.5		4.0	40.0	μA	V <sub>IN</sub> = V <sub>CC</sub> or GND	
V <sub>OLP</sub>	Quiet Output Maximum Dynamic V <sub>OL</sub>	5.0	1.1	1.5		V	Figure 1, Figure 2 (Note 10)(Note 11)	
V <sub>OLV</sub>	Quiet Output Minimum Dynamic V <sub>OL</sub>	5.0	-0.6	-1.2		V	Figure 1, Figure 2 (Note 10)(Note 11)	
V <sub>IHD</sub>	Minimum HIGH Level Dynamic Input Voltage	5.0	1.9	2.2		V	(Note 10)(Note 12)	
V <sub>ILD</sub>	Maximum LOW Level Dynamic Input Voltage	5.0	1.2	0.8		V	(Note 10)(Note 12)	
<p><b>Note 8:</b> All outputs loaded; thresholds on input associated with output under test.</p> <p><b>Note 9:</b> Maximum test duration 2.0 ms, one output loaded at a time.</p> <p><b>Note 10:</b> DIP package.</p> <p><b>Note 11:</b> Max number of outputs defined as (n). Data inputs are driven 0V to 3V. One output @ GND.</p>								

**DC Electrical Characteristics for ACTQ** (Continued)

**Note 12:** Max number of data inputs (n) switching, (n-1) inputs switching 0V to 3V (ACTQ). Input-under-test switching: 3V to threshold ( $V_{ILD}$ ), 0V to threshold ( $V_{IHD}$ ),  $f = 1$  MHz.

**AC Electrical Characteristics for ACQ**

Symbol	Parameter	$V_{CC}$ (V) (Note 13)	$T_A = +25^\circ\text{C}$ $C_L = 50$ pF			$T_A = -40^\circ\text{C to } +85^\circ\text{C}$ $C_L = 50$ pF		Units
			Min	Typ	Max	Min	Max	
$f_{MAX}$	Maximum Clock Frequency	3.3 5.0	75 90			70 85		MHz
$t_{PLH}$ $t_{PHL}$	Propagation Delay CP to $\overline{O}_n$	3.3 5.0	3.0 2.0	9.5 6.5	13.0 8.5	3.0 2.0	13.5 9.0	ns
$t_{PZH}$ $t_{PZL}$	Output Enable Time	3.3 5.0	3.0 2.0	9.5 6.5	13.0 8.5	3.0 2.0	13.5 9.0	ns
$t_{PHZ}$ $t_{PLZ}$	Output Disable Time	3.3 5.0	1.0 1.0	9.5 8.0	14.5 9.5	1.0 1.0	15.0 10.0	ns
$t_{OSHL}$ $t_{OSLH}$	Output to Output Skew (Note 14) CP to $\overline{O}_n$	3.3 5.0		1.0 0.5	1.5 1.0		1.5 1.0	ns

**Note 13:** Voltage Range 5.0 is  $5.0V \pm 0.5V$   
Voltage Range 3.3 is  $3.3V \pm 0.3V$

**Note 14:** Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW ( $t_{OSHL}$ ) or LOW-to-HIGH ( $t_{OSLH}$ ). Parameter guaranteed by design.

**AC Operating Requirements for ACQ**

Symbol	Parameter	$V_{CC}$ (V) (Note 15)	$T_A = +25^\circ\text{C}$ $C_L = 50$ pF		$T_A = -40^\circ\text{C to } +85^\circ\text{C}$ $C_L = 50$ pF		Units
			Typ	Guaranteed Minimum			
$t_S$	Setup Time, HIGH or LOW $D_n$ to CP	3.3 5.0	0 0	3.0 3.0	3.0 3.0		ns
$t_H$	Hold Time, HIGH or LOW $D_n$ to CP	3.3 5.0	0 0	1.5 1.5	1.5 1.5		ns
$t_W$	CP Pulse Width, HIGH or LOW	3.3 5.0	2.0 2.0	4.0 4.0	4.0 4.0		ns

**Note 15:** Voltage Range 5.0 is  $5.0V \pm 0.5V$   
Voltage Range 3.3 is  $3.3V \pm 0.3V$

**AC Electrical Characteristics for ACTQ**

Symbol	Parameter	$V_{CC}$ (V) (Note 16)	$T_A = +25^\circ\text{C}$ $C_L = 50$ pF			$T_A = -40^\circ\text{C to } +85^\circ\text{C}$ $C_L = 50$ pF		Units
			Min	Typ	Max	Min	Max	
$f_{MAX}$	Maximum Clock Frequency	5.0	85			80		MHz
$t_{PLH}$ $t_{PHL}$	Propagation Delay CP to $\overline{O}_n$	5.0	2.0	7.0	9.0	2.0	9.5	ns
$t_{PZH}$ $t_{PZL}$	Output Enable Time	5.0	2.0	7.0	9.0	2.0	9.5	ns
$t_{PHZ}$ $t_{PLZ}$	Output Disable Time	5.0	1.0	8.0	10.0	1.0	10.5	ns
$t_{OSHL}$ $t_{OSLH}$	Output to Output Skew (Note 17) CP to $\overline{O}_n$	5.0		0.5	1.0		1.0	ns

**Note 16:** Voltage Range 5.0 is  $5.0V \pm 0.5V$ .

**Note 17:** Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW ( $t_{OSHL}$ ) or LOW-to-HIGH ( $t_{OSLH}$ ). Parameter guaranteed by design.

### AC Operating Requirements for ACTQ

Symbol	Parameter	V <sub>CC</sub> (V) (Note 18)	T <sub>A</sub> = +25°C C <sub>L</sub> = 50 pF		T <sub>A</sub> = -40°C to +85°C C <sub>L</sub> = 50 pF	Units
			Typ	Guaranteed Minimum		
t <sub>S</sub>	Setup Time, HIGH or LOW D <sub>n</sub> to CP	5.0	0	3.0	3.0	ns
t <sub>H</sub>	Hold Time, HIGH or LOW D <sub>n</sub> to CP	5.0	0	1.5	1.5	ns
t <sub>W</sub>	CP Pulse Width, HIGH or LOW	5.0	2.0	4.0	4.0	ns

Note 18: Voltage Range 5.0 is 5.0V ± 0.5V

### Capacitance

Symbol	Parameter	Typ	Units	Conditions
C <sub>IN</sub>	Input Capacitance	4.5	pF	V <sub>CC</sub> = OPEN
C <sub>PD</sub>	Power Dissipation Capacitance	40.0	pF	V <sub>CC</sub> = 5.0V

## FACT Noise Characteristics

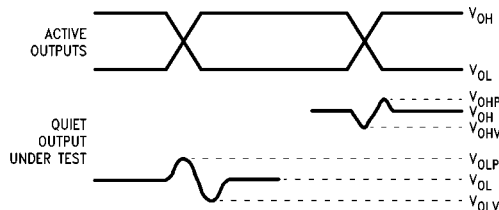
The setup of a noise characteristics measurement is critical to the accuracy and repeatability of the tests. The following is a brief description of the setup used to measure the noise characteristics of FACT.

### Equipment:

Hewlett Packard Model 8180A Word Generator  
PC-163A Test Fixture  
Tektronics Model 7854 Oscilloscope

### Procedure:

1. Verify Test Fixture Loading: Standard Load 50 pF, 500Ω.
2. Deskew the HFS generator so that no two channels have greater than 150 ps skew between them. This requires that the oscilloscope be deskewed first. It is important to deskew the HFS generator channels before testing. This will ensure that the outputs switch simultaneously.
3. Terminate all inputs and outputs to ensure proper loading of the outputs and that the input levels are at the correct voltage.
4. Set the HFS generator to toggle all but one output at a frequency of 1 MHz. Greater frequencies will increase DUT heating and effect the results of the measurement.
5. Set the HFS generator input levels at 0V LOW and 3V HIGH for ACT devices and 0V LOW and 5V HIGH for AC devices. Verify levels with an oscilloscope.



**Note 19:**  $V_{OHV}$  and  $V_{OLP}$  are measured with respect to ground reference.

**Note 20:** Input pulses have the following characteristics:  $f = 1$  MHz,  $t_r = 3$  ns,  $t_f = 3$  ns, skew < 150 ps.

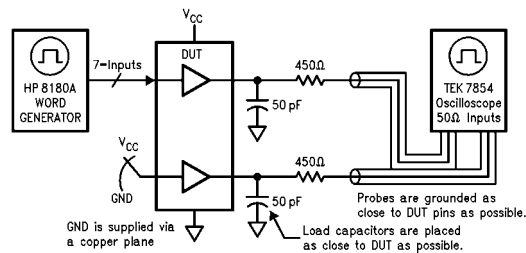
**FIGURE 1. Quiet Output Noise Voltage Waveforms**

$V_{OLP}/V_{OLV}$  and  $V_{OHP}/V_{OHV}$ :

- Determine the quiet output pin that demonstrates the greatest noise levels. The worst case pin will usually be the furthest from the ground pin. Monitor the output voltages using a 50Ω coaxial cable plugged into a standard SMB type connector on the test fixture. Do not use an active FET probe.
- Measure  $V_{OLP}$  and  $V_{OLV}$  on the quiet output during the worst case for active and enable transition. Measure  $V_{OHP}$  and  $V_{OHV}$  on the quiet output during the worst case active and enable transition.
- Verify that the GND reference recorded on the oscilloscope has not drifted to ensure the accuracy and repeatability of the measurements.

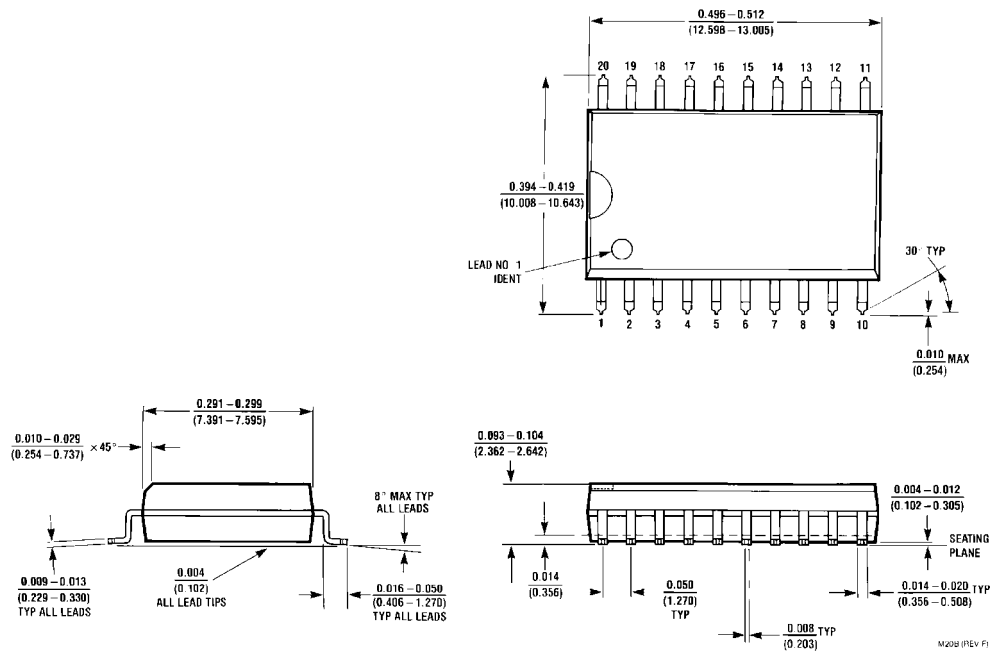
$V_{ILD}$  and  $V_{IHD}$ :

- Monitor one of the switching outputs using a 50Ω coaxial cable plugged into a standard SMB type connector on the test fixture. Do not use an active FET probe.
- First increase the input LOW voltage level,  $V_{IL}$ , until the output begins to oscillate or steps out a min of 2 ns. Oscillation is defined as noise on the output LOW level that exceeds  $V_{IL}$  limits, or on output HIGH levels that exceed  $V_{IH}$  limits. The input LOW voltage level at which oscillation occurs is defined as  $V_{ILD}$ .
- Next decrease the input HIGH voltage level,  $V_{IH}$ , until the output begins to oscillate or steps out a min of 2 ns. Oscillation is defined as noise on the output LOW level that exceeds  $V_{IL}$  limits, or on output HIGH levels that exceed  $V_{IH}$  limits. The input HIGH voltage level at which oscillation occurs is defined as  $V_{IHD}$ .
- Verify that the GND reference recorded on the oscilloscope has not drifted to ensure the accuracy and repeatability of the measurements.



**FIGURE 2. Simultaneous Switching Test Circuit**

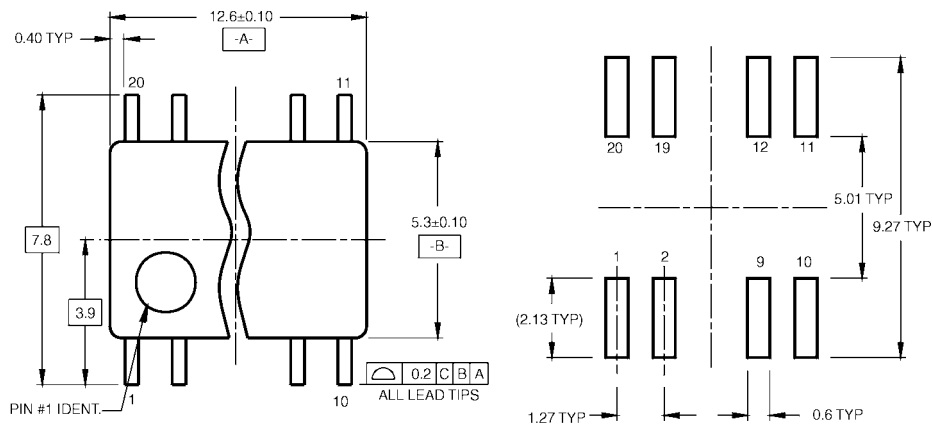
**Physical Dimensions** inches (millimeters) unless otherwise noted



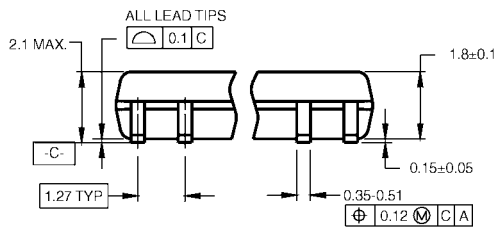
**20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide Body  
Package Number M20B**



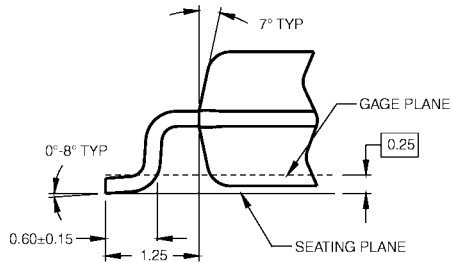
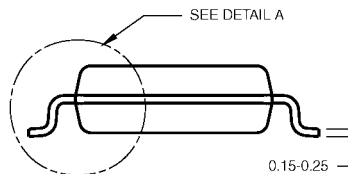
**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



LAND PATTERN RECOMMENDATION



DIMENSIONS ARE IN MILLIMETERS



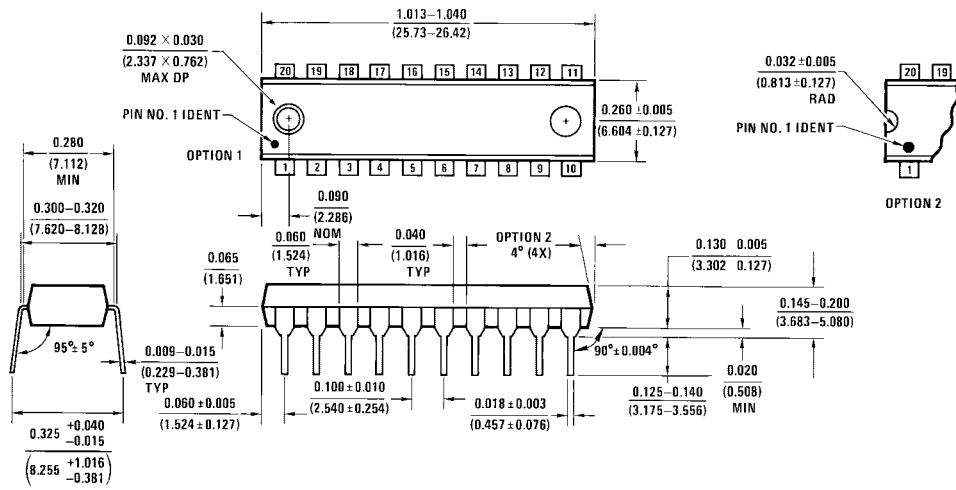
DETAIL A

- NOTES:  
 A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.  
 B. DIMENSIONS ARE IN MILLIMETERS.  
 C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M20DRevB1

**20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide  
 Package Number M20D**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide  
Package Number N20A

N20A (REV G)

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

**LIFE SUPPORT POLICY**

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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