FAIRCHILD SEMICONDUCTOR®

June 2002
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OCX256L • OCX256P
Crosspoint Switch with LVDS (Preliminary) • Crosspoint Switch with LVPECL (Preliminary)

General Description

The OCX256 SRAM-based devices are non-blocking 128 X 128 digital crosspoint switches and are available in LVDS (Low Voltage Differential Signaling) and LVPECL (Low Voltage PECL) versions. Both devices are capable of data rates of 667 Megabits per second per port. The I/O ports are fixed as either input or output ports. The input ports support flow-through mode only. The output ports are individually programmable to operate in either flow-through (asynchronous) or registered (synchronous) mode. Each output register may be clocked by a global clock or a next neighbor clock source.

The patented ActiveArray provides greater density, superior performance, and greater flexibility compared to a traditional n:1 multiplexer architecture. The OCX devices support various operating modes covering one input to one output at a time as well as one input to many outputs, plus a special broadcast mode to program one input to all outputs while maintaining maximum data rates. In all modes data integrity and connections are maintained on all unchanged data paths.

The RapidConfigure™ parallel interface allows fast configuration of both the Output Buffers and the switch matrix. Readback is supported for device test and verification purposes. The OCX256 also supports the industry standard JTAG (IEEE 1149.1) interface for boundary scan testing. The JTAG interface can also be used to download configuration data to the device and readback data. A functional block diagram of the OCX256 is shown in Figure 1.

Features

- 667 Mb/s port data bandwidth, >85Gb/s aggregate bandwidth
- Low power CMOS, 2.5V and 3.3V power supply
- SRAM-based, in-system programmable
- LVDS I/O (OCX256L) and LVPECL I/O (OCX256P) versions
- 256 configurable I/O ports
  - 128 dedicated differential input ports
  - 128 dedicated differential output ports
  - LVTTL control interface
  - Output Enable control for all outputs
- Non-blocking switch matrix
  - Patented ActiveArray™ matrix for superior performance
  - Double-buffered configuration RAM cells for simultaneous global updates
  - ImpliedDisconnect™ function for single cycle disconnect/connect
- Full Broadcast and multicast capability
  - One-to-One and One-to-Many connections
  - Special broadcast mode routes one input to all outputs at maximum data rate
- Registered and flow-through data modes
  - 333 MHz synchronous mode
  - 667 Mb/s asynchronous mode
  - Low jitter and signal skew
  - Low duty cycle distortion
- RapidConfigure parallel interface for configuration and readback
- JTAG serial interface for configuration and Boundary Scan testing
- 792 TBGA package with 1.00mm ball spacing
- Integrated Termination Resistors

Applications

- SONET/SDH and DWDM
- Digital Cross-Connects
- System Backplanes and Interconnects
- High Speed Test Equipment
- ATM Switch Cores
- Video Switching

Ordering Code:

Order Number	Package Number	Package Description
OCX256LTB792	BGA792A	792-Ball Thermally-Enhanced Ball Grid Array (TBGA), JEDEC MO-149, 1.0mm pitch, 40mm Square
OCX256PTB792	BGA792A	792-Ball Thermally-Enhanced Ball Grid Array (TBGA), JEDEC MO-149, 1.0mm pitch, 40mm Square

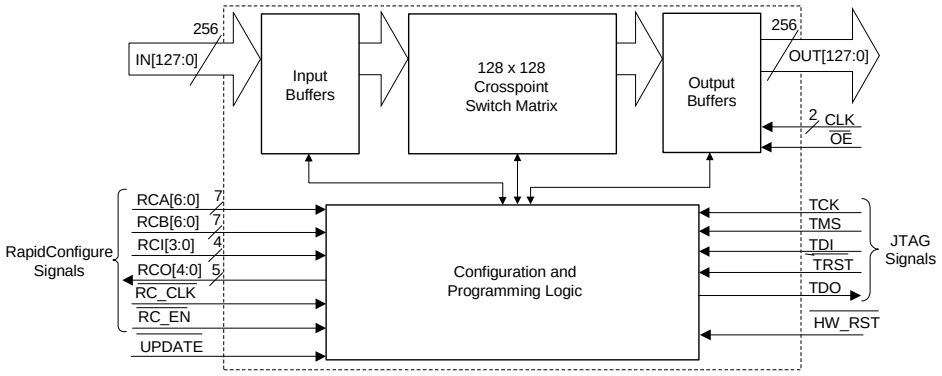


FIGURE 1. OCX256 Functional Block Diagram

Introduction

The OCX256 is a differential crosspoint-switching device. The main functional block of the device is a Switch Matrix as shown in Figure 1. The Switch Matrix is a x-y structure supporting an input-to-output data flow. Figure 2 shows a conceptual view of the switch matrix with inputs connected to the horizontal trace and outputs to the vertical trace. Connections between vertical and horizontal lines are implemented with a proprietary high-performance buffering circuit. Signal path delays through the Switch Matrix are very well balanced, resulting in predictable and uniform pin-to-pin delays.

Note: For the purpose of clarity, the logic diagrams within this datasheet are conceptual representations only and do not show actual circuit implementation.

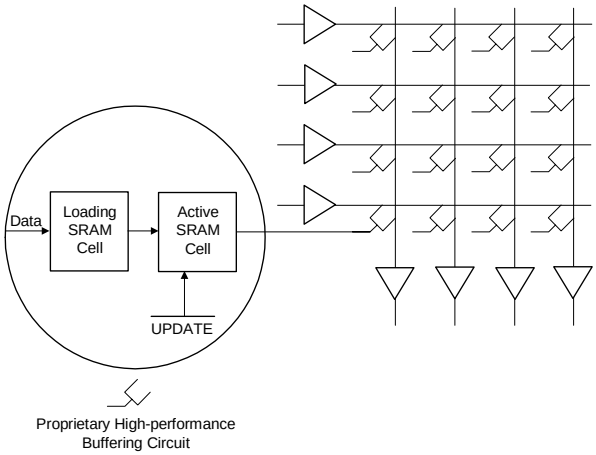


FIGURE 2. OCX256 Switch Matrix

The Active SRAM cells are responsible for establishing connections in the switch matrix by turning on the interconnect circuit, while the Loading SRAM cell can be used to store a second configuration that can be transferred to the Active SRAM cell at a later time. The two SRAM cells are arranged so that a double buffered scheme can be employed. Through the use of an internal signal (generated automatically during a programming cycle) it is possible to store a second configuration map in the Loading SRAM while the Active SRAM maintains its present connection status. When the $\overline{\text{UPDATE}}$ signal is asserted LOW (Active LOW), the contents of the Loading SRAM cell are transferred to the Active SRAM cell and the switch matrix connection is either made or broken.

The $\overline{\text{UPDATE}}$ signal can be used to control when the switch matrix is reconfigured. For instance, as long as the $\overline{\text{UPDATE}}$ signal is de-asserted (held HIGH), the Loading SRAM cells for the entire switch matrix could be changed without affecting the current configuration of the switch. When the $\overline{\text{UPDATE}}$ signal is asserted LOW, the entire switch matrix would be reconfigured simultaneously. If the $\overline{\text{UPDATE}}$ signal is asserted continuously, all crosspoint programming commands (generated by RapidConfigure or JTAG programming cycles) will take effect immediately, since the Loading SRAM cell's contents will be transferred directly to the Active SRAM cell.

Introduction (Continued)

Input and Output Buffers

All of the input buffers are differential inputs with flow-through mode. The output buffers are programmable for either flow-through or registered mode. Figure 3 shows the basic block diagram of the input and output blocks with the sources for the output control signals ($\overline{OE}$ and CLK). The control signals are explained in more details in the following sections

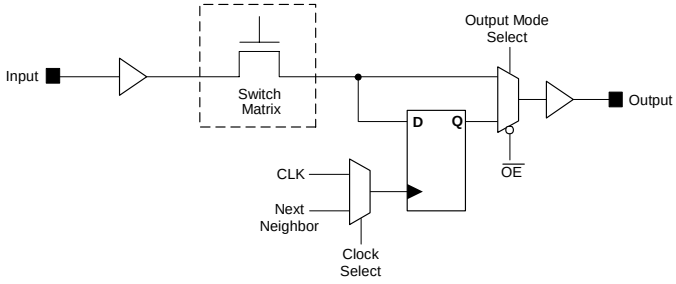


FIGURE 3. Input and Output Buffer Configuration

Input and Output Port Function Mode

The following legend describes the various modes of the Input and Output Ports and the specification used by the OCXPro Software.

Legend:

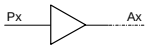
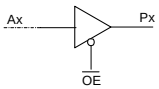
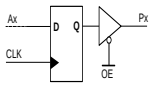
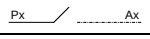
Ax–Switch Matrix Signal

Px–Port Signal

$\overline{OE}$–Output Enable (Active LOW)

CLK–Clock

TABLE 1. Summary for Programmable I/O Attributes for OCX256

Symbol	I/O Port Function		Mnemonic
	Input	The external signal is buffered from the Input Port pin to the corresponding Switch Matrix line.	IN
	Output	The internal signal is buffered from the corresponding Switch Matrix line to the Output Port pin. In this mode an optional output enable ($\overline{OE}$) can be selected. The default state is logic high with enable set to ON.	OP
	Registered Output	The internal signal on the Switch Matrix line is registered by an edge-triggered register within the Output Port. A clock source is required in this mode. An output enable ($\overline{OE}$) is available but not required.	RO
	No Connect	In this mode, the output Port pin is isolated from the Switch Matrix	NC

Broadcast Mode

The OCX256 has a special Broadcast Mode which connects any input to all outputs without performance degradation. The input is selected using RapidConfigure or JTAG and disconnects all other inputs. The Global Update pin ($\overline{UPDATE}$) must be held high during Broadcast Mode. Asserting the $\overline{UPDATE}$ pin returns the array to the previous program condition.

Output Buffer Configuration

Every output port of the OCX256 can be configured as either a flow-through or registered output. In registered mode there are two clock sources that are available:

- Global Clock
- Next Neighbor

Additionally, there are output control signals.

Output Control Signals

Every output port of the OCX has a global Output Enable signal ($\overline{OE}$). All output buffers have output enables that have programmable polarity and are individually configurable.

Additionally each output can be permanently enabled (always ON) or disabled (always OFF) which is useful for applications which need to 3-STATE outputs (for example when using multiple chips in expansion mode) or for power saving in designs that do not need to use all the outputs available.

Two control bits are used to control the function of the output enable function as described in Table 5.

Introduction (Continued)

Neighboring Output Port as a Clock Source

A physically adjacent port can be used as a clock source for an output port configured in registered mode. These outputs are grouped in pairs such that the signal being switched through OUT0 can be used to clock the signal being switched through OUT1, and vice versa. Any single clock or data input signal can be used to clock any other input signal provided they are switched to an appropriate output pair (see Table 2). Figure 4 shows the implementation of next neighbor output port clocking in the OCX256 switch.

For example, INx is used for data input while INy is used for the corresponding clock. INx is connected to OUT0 via the crosspoint array while INy is connected to OUT1 via the crosspoint array. OUT0 is configured in registered output (RO) mode with OUT1 as its next neighbor clock selection. OUT1 will output the clock signal as well as clock the data in OUT0. Adjacent port selection is required for next neighbor clocking in the registered output mode.

This feature is useful in many applications where different types of data switching through the crosspoint array have various associated clocks. To match the delays in the data and corresponding clocks, it is common practice to pass the clocks through the switch along with the data.

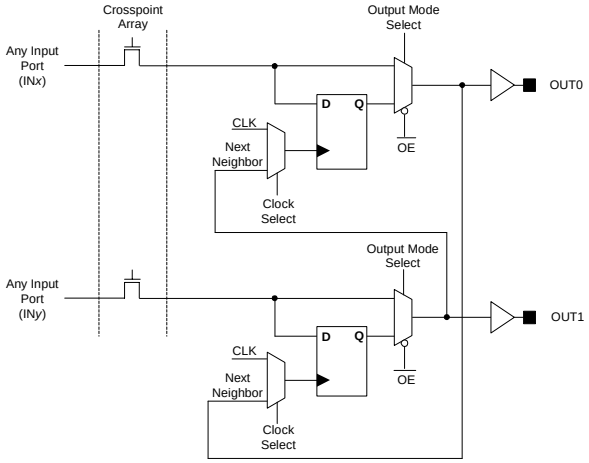


FIGURE 4. Next Neighbor Clock Block Diagram

The advantages of next neighbor clocking are:

1. Using next neighbor clocking in the registered output (RO) mode helps reduce the skew in outgoing data.
2. For a design with a large number of outputs switching simultaneously, next neighbor clocking mode is useful to stagger outputs for reduced board noise caused by simultaneous switching outputs.

Note: Selecting the next neighbor clock for both outputs at the same time is not recommended. Only one output in the pair at a time can be clocked by its next neighbor.

TABLE 2. Next Neighbor Outputs

Pairing Sequence for Neighboring Outputs								
Output Next Neighbor Pairs	0,1	2,3	4,5	6,7	8,9	• • • •	124,125	126,127

Only OUT1 can neighbor with OUT0, OUT3 with OUT2, etc. OUT2 cannot neighbor with OUT1, or OUT4 with OUT3, etc.

RapidConfigure Interface

RapidConfigure (RC) is a 25 signal parallel interface that is used to program the OCX256 device. The 25 pins are allocated as follows:

RCA[6:0] = RapidConfigure Address A.
RCA are input pins.

RCB[6:0] = RapidConfigure Address B.
RCB are input pins.

RCI[3:0] = RapidConfigure Instruction Bits

RCO[4:0] = RapidConfigure Readback.
RCO are output pins.

RC_$\overline{\text{CLK}}$ = RapidConfigure Clock

RC_$\overline{\text{EN}}$ = RapidConfigure Cycle Enable
(state is sensed on negative edge of clock)

RapidConfigure Programming Instructions

The RC interface supports both write and read types of operations:

1. Write Operations (reset crosspoint and Input or Output Buffer (IOB), configure an Output Buffer, connect/disconnect crosspoint)
2. Read Operations (Output Buffer and crosspoint configuration read)

Introduction (Continued)

TABLE 3. RapidConfigure Programming Instructions

RCI[3:0]	RCA[6:0]	RCB[6:0]	RCO[4:0]	Instruction	Description
0000				Reserved	
0001				Reserved	
0010	X	X		Reset Crosspoint Array	Reset, along with an Update operation ($\overline{\text{UPDATE}}$ pin or Update command), resets the entire crosspoint array to no connect. All Output Buffers remain unchanged by this operation.
0011	X	Input Port Address		Set Array to Broadcast Mode	Connects the input selected by RCB[6:0] to all output ports and disconnects all other inputs. The Global Update ($\overline{\text{UPDATE}}$) pin must be held high during Broadcast mode. Activating the Global Update pin returns the array to the previous program condition.
0100	Output Port Address	Data		Configure an Output Buffer	Program an Output Buffer specified by RCA[6:0]. See Table 5 for RCB[6:0] bit assignment and buffer functionality.
0101				Readback Crosspoint, Output Buffer Status	This is a two-cycle instruction.
Cycle 1	Output Port Address	Input Port Address	X		Specify the crosspoint connect status at output location specified by RCA[6:0] to the input location specified by RCB[6:0].
Cycle 2	X	X	Output Data		Readback (using RCO[4:0]) the status of the output buffer specified in Cycle 1 by RCA[6:0], the output buffer specified in Cycle 1 by RCO[4:0] and the crosspoint connect status. See Table 4 for RCO[4:0] readback pin assignment.
0110	X	X		Update	Program the Global Update function without the use of the $\overline{\text{UPDATE}}$ pin.
0111	X	Input Port Address		Disconnect Input	Disconnect the crosspoint cells of the output row location specified by RCA[6:0].
1000	Output Port Address	Input Port Address		Disconnect Input and Output	Disconnect the crosspoint cell at the output location specified by RCA[6:0] to the input location specified by RCB[6:0]. All other connections from the source input address or to the same output address remain the same as before.
1001	Output Port Address	Input Port Address		Connect, with ImpliedDisconnect	Connect the crosspoint cell at the output location specified by RCA[6:0] to the input location specified by RCB[6:0]. All other connections from the same input address or to the same output address are set to No Connect (NC).
1010	Output Port Address	Input Port Address		Connect, without ImpliedDisconnect	Connect the crosspoint cell at the output location specified by RCA[6:0] to the input location specified by RCB[6:0]. All other connections to the same output address are set to No Connect while all other connections from the same input address remain the same as before.
1011				Reserved	
1100				Reserved	
1101	X	X		Reset All	Reset the switch matrix to No Connects (NC). Update is forced internally. Sets the Output Buffer to Flow-through mode with Output Enabled.
1110				Reserved	
1111				Reserved	

X = Don't care.

Introduction (Continued)

TABLE 4. RCO[4:0] Readback Pin Assignment

RCO[4:0]	Readback Location	Signal/Function
O4	Crosspoint	Connection Status: 0 = No connection (NC) — (default state at reset) 1 = Connected
O3	Output Buffer	Clock Select: 0 = Global Clock — (default state at reset) 1 = Next Neighbor
O2	Output Buffer	Output Mode: 0 = Flow-through (OP) — (default state at reset) 1 = Registered (RO)
O1, O0 0, 0 0, 1 1, 0 1, 1	Output Buffer	Output Enable: Output enabled (ON) – this is the default state at reset Output disabled (OFF) Output controlled by OE (Active HIGH) Output controlled by $\overline{OE}$ (Active LOW)

TABLE 5. Programming an Output Buffer using RapidConfigure

RCB[6:0]	Signal/Function
B6, B5, B4	Don't Care
B3	Clock Select: 0 = Global Clock 1 = Next Neighbor
B2	Output Mode: 0 = Flow-through (OP) 1 = Registered (RO)
B1, B0 0, 0 0, 1 1, 0 1, 1	Output Enable: Output Enabled (ON) – this is the default state at reset Output Disabled (OFF) Output Controlled by OE (Active HIGH) Output Controlled by $\overline{OE}$ (Active LOW)

JTAG Configuration Controller

The Output port attributes and the Switch Matrix connections can be programmed using the JTAG serial bus. The RapidConfigure Interface can be enabled or disabled using the JTAG serial bus.

The JTAG–based serial mode is always available for configuration regardless of whether the RapidConfigure mode is enabled or disabled. However, proper care must be taken when switching between JTAG and RapidConfigure for configuring the devices. Before attempting to change Switch Matrix connections or output port configuration through JTAG, the user must first ensure that the RapidConfigure mode is disabled by using JTAG serial mode to set the RCE bit to zero in the Mode Control Register.

JTAG Interface

The dedicated JTAG TAP interface is designed in compliance with the IEEE-1149.1. The standard interface has five pins: Test Data Out (TDO), Test Mode Select (TMS), Test Data In (TDI), Test Reset ($\overline{TRST}$), and Test Clock (TCK), which allow Boundary Scan Testing as well as device configuration and verification. The Fairchild supplied software will automatically generate the necessary bitstream from a higher-level textual description of the required configuration. Data on the TDI and TMS pins are clocked into the device on the rising edge of the TCK signal, while the valid data appears on the TDO pin after the falling edge of TCK. For more detailed information on JTAG programming, refer to the OCX Family Register Programming Manual.

Output Port Configuration

Output port configuration is accomplished by loading the appropriate bitstream into the programming registers present at each Output port. The JTAG serial bus is used to load configuration data into the Output port programming registers, one Output port at a time.

Switch Matrix Configuration

The contents of the SRAM cells controlling Switch Matrix connection can be modified using the JTAG. This is accomplished by loading the configuration data, one word at a time, into the SRAM cells in the Switch Matrix.

Introduction (Continued)

Mode Control Register Configuration

The OCX256 contains a single bit Mode Control Register used to store user flags for RapidConfigure Enable (RCE). These are required for proper functioning of the device. The contents of this register can be changed using the JTAG interface and a special JTAG instruction.

TABLE 6. Mode Control Register

RCE	Mode
0	RapidConfigure Interface Disabled (OFF)
1	RapidConfigure Interface Enabled (ON)

JTAG Architecture and Shift Registers

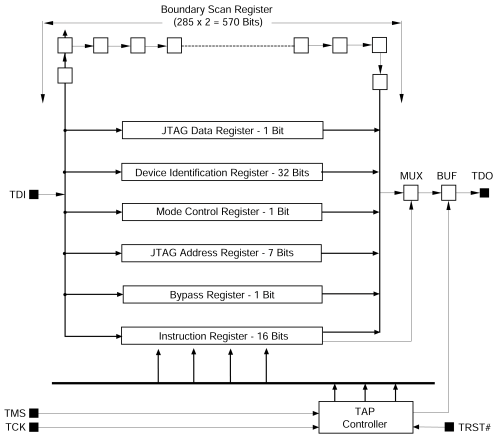


FIGURE 5. OCX256 JTAG Architecture

JTAG State Machine

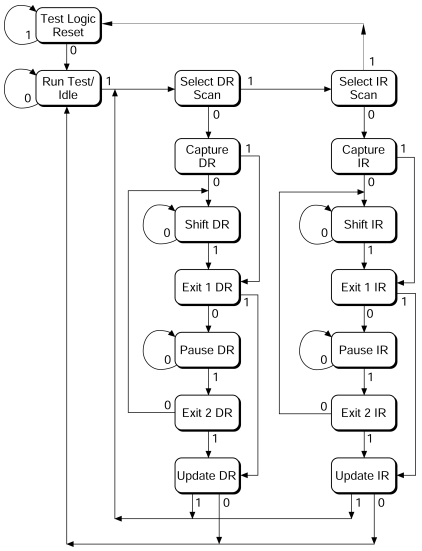


FIGURE 6. OCX256 JTAG State Machine

TABLE 7. JTAG Input Format

	Instruction				Data					Address A						
Bit Number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit Name	I3	I2	I1	I0	BB	BA	B9	B8	B7	A6	A5	A4	A3	A2	A1	A0

Introduction (Continued)

TABLE 8. JTAG Instructions

I [3:0]	BB	BA	B9	B8	B7	A6 - A0	Instruction	Description
0 0 0 0	X	X	X	X	X	X	Sample/EXTEST	Places the device in Scan Mode.
0 0 0 1	X	X	X	X	X	X	Sample/EXTEST	Places the device in Scan Mode.
0 0 1 0	X	X	X	X	X	X	Reset the Crosspoint Array	Resets the entire Crosspoint Array to No Connect. All other Output Buffer configurations are unchanged by this operation.
0 0 1 1	X	X	X	X	X	X	Set Array for Broadcast mode	Use the JTAG Address Register as the Input address to be the broadcast input Connects the selected Input to all Output cells and disconnects all other Inputs. Activating the Global Update JTAG instruction returns the Crosspoint array from the Broadcast mode to the previous programed state.
0 1 0 0	X	Clock Select	Data Mode	OE	OE	Output Buffer Address	Program a Buffer	Programs the Output Buffer address specified in the JTAG instruction (A6-A0). The configuration data is also specified in the JTAG instruction bits BA-B7. See Table 11 for bit assignment of the Buffer functionality.
0 1 0 1	X	X	X	X	X	Output Address/ Buffer	Configuration Readback	Readback the connectivity of the Crosspoint cell with the Input location specified in the JTAG Address Register and the Output location specified JTAG instruction (A0-A6). It also returns the configuration of the Output Buffer addressed in the JTAG instruction (A0-A6). The readback data is shifted out of TDO in the following sequence: 1. Crosspoint Connect (1 = Connected, 0 = No Connection) 2. Output Enable – B7 (see Table 11) 3. Output Enable – B8 (see Table 11) 4. Output Data Source – B9 (0 = Flow-through, 1 = registered) 5. Output Clock Select – BA (0 = Global Clock, 1 = Next Neighbor) 6. State of Broadcast bit 7. State of the RCE bit **Note:** This instruction does not increment the JTAG Address Register. This instruction also requires two DR cycles
0 1 1 0	X	X	X	X	X	X	Update the Crosspoint Array	Update the programmed connection from the Loading SRAM to the Active SRAM.
0 1 1 1	X	X	X	X	X	X	Disconnect Input Cell	Disconnect the Crosspoint connections from the Input address specified in the JTAG Address Register.
1 0 0 0	X	X	X	X	X	Output Address	Disconnect Input and Output	Disconnect the Crosspoint cell at the Input location specified at the JTAG Address Register and the Output location specified in the Disconnect JTAG instruction (A6-A0). All other connections from the same input address or to the same output address remain the same.
1 0 0 1	X	X	X	X	X	Output Address	Connect with ImpliedDisconnect	Connects the Crosspoint cell at the Input location specified on the JTAG Address Register and the output location specified in the Connect JTAG instruction (A6-A0). All other connections from the same Input address or the same Output address are set to no-connects. **Note:** This instruction increments the JTAG Address Register (Input address).

Introduction (Continued)

TABLE 9. JTAG Instructions (Continued)

I [3:0]	BB	BA	B9	B8	B7	A6 - A0	Instruction	Description
1 0 1 0	X	X	X	X	X	Output Address	Connect— No ImpliedDisconnect	Connects the Crosspoint cell at the Input address specified in the JTAG Address Register and the Output address specified in the Connect JTAG instruction (A6-A0). All connections to the same output address are set to “No Connect” while all other connections from the same input remain the same as before.
1 0 1 1	X	X	X	X	X	Input Address	Set the JTAG Address Register	Sets the 7-bit JTAG Address Register with the 7-bit address (A6-A0) of the JTAG Instruction Register. The 7-bit address of the JTAG Address Register becomes the Input port address for Crosspoint Access.
1 1 0 0	X	X	X	X	X	X	Device ID Out	Serialize the device ID and revision history out to TDO. ID for the OCX256 is 0x0000C89F
1 1 0 1	X	X	X	X	X	X	Reset Output Buffer and Crosspoint Array	Resets the Crosspoint Array to no-connects. Sets the Output buffer to Flow-through mode with Output Enabled. The device ID is serialized to TDO.
1 1 1 0	X	X	X	X	X	X	Set RCE Bit	Sets the RCE bit of the Mode Control Register with the JTAG instruction bit A0. To turn ON the RCE bit, encode bit A0 to 1. To turn OFF the RCE bit, encode bit A0 to 0.
1 1 1 1	X	X	X	X	X	X	Bypass	Places device in a mode to pass TDI data to TDO with one clock delay. Used for programming and testing devices through serial connected JTAG controls.

TABLE 10. Programming an Output using JTAG

BA, B9, B8, B7	Signal/Function
BA	Clock Select: 0 = Global Clock 1 = Next Neighbor
B9	Output Mode: 0 = Flow-through (OP) 1 = Registered (RO)
B8, B7	Output Enable:
0,0	Output Enabled (ON) – this is the default state at reset
0,1	Output Disabled (OFF)
1,0	Output Controlled by OE (Active HIGH)
1,1	Output Controlled by $\overline{OE}$ (Active LOW)

Introduction (Continued)

TABLE 11. Number of JTAG Cycles and Configuration Time

Operation	OCX256 JTAG Cycles
JTAG Reset Sequence (TMS = “11111”)	7
Enable or Disable RapidConfigure	28
Change Attributes of ONE Output Port	28
Change Attributes of ALL Output Ports	3,584
Reset JTAG Controller + Reset ALL Output Ports + Clear ALL SRAM Cells	35
Connect or Disconnect two Ports	56
Configure Entire Switch Matrix	462,336
Completely Configure the Device (All Output Ports and All Switch Matrix Connections)	456,920

ImpliedDisconnect

ImpliedDisconnect is a feature that provides the ability to make fast switch connection changes. When using the instruction “Connect, without ImpliedDisconnect” all other connections to the specified output are set to No Connect. However, the specified input remains connected to any output that it was connected to before.

When using the instruction “Connect, with ImpliedDisconnect” all connections from the specified input and to the specified output are set to No Connect.

Thus, a connection change, i.e. breaking an existing connection and then making a new one, can be accomplished in one RapidConfigure cycle.

Device Reset Options

The power-on reset, RapidConfigure reset, hardware reset, and JTAG reset functions will program the output buffers to flow-through mode (with Global Clock selected), and Output Enabled (ON). JTAG can be reset via the $\overline{\text{TRST}}$ pin or by clocking five consecutive one to the TMS pin. The hardware_reset pin can be done accomplished through the HW_$\overline{\text{RST}}$ pin (Active LOW). RC reset can be accomplished by applying the RC instruction 1101 to the RCI[3:0] pins.

TABLE 12. Device Reset Options

Programming Interface	Reset Method	Output Ports	Switch Matrix	RCE Mode Control	JTAG TAP
Hardware Reset	Power-on Reset	OP	NC	1 (RC Enabled)	TLR
	HW_$\overline{\text{RST}}$ (LOW Pulse)	OP	NC	1 (RC Enabled)	TLR
JTAG Reset	1. Low Pulse on $\overline{\text{TRST}}$	Unchanged	Unchanged	Unchanged	TLR
	2. TMS HIGH for 5 TCLK cycles	Unchanged	Unchanged	Unchanged	TLR
	3. Device Reset (Instruction 1101)	OP	NC	1 (RC Enabled)	TLR
	4. Reset Crosspoint Array (Instruction 0010)	Unchanged	NC	Unchanged	Unchanged
RapidConfigure Reset	1. Device reset (Instruction 1101)	OP	NC	1 (RC Enabled)	Unchanged
	2. Reset Crosspoint Array (Instruction 0010)	Unchanged	NC	Unchanged	Unchanged

TLR = Test Logic Reset state.

Pin Description

TABLE 13. OCX256 Pin Description

Pin Name	Number of Pins	Type	Description
INPP[127:0]	128	Input	Non-inverting Differential Input Signals
INN[127:0]	128	Input	Inverting Differential Input Signals
OUTP[127:0]	128	Output	Non-inverting Differential Input Signals
OUTN[127:0]	128	Output	Inverting Differential Input Signals
CLKP	1	Input	Non-inverting Differential Global Clock
CLKN	1	Input	Inverting Differential Global Clock
$\overline{OE}$	1	Input	Global Output Enable
$\overline{HW\_RST}$	1	Input	Hardware Reset
$\overline{UPDATE}$	1	Input	Global Update
RC Pins			
RCA[6:0]	7	Input	RapidConfigure Address A
RCB[6:0]	7	Input	RapidConfigure Address B
RCO[4:0]	5	Output	RapidConfigure Readback
RCI[3:0]	4	Input	RapidConfigure Instruction Bits
$\overline{RC\_CLK}$	1	Input	RapidConfigure Clock
$\overline{RC\_EN}$	1	Input	RapidConfigure Cycle Enable
JTAG Pins			
TCK	1	Input	JTAG Test Clock
TMS	1	Input	JTAG Test Mode Select
TDI	1	Input	JTAG Test Data In
$\overline{TRST}$	1	Input	JTAG Test Reset
TDO	1	Output	JTAG Test Data Out
Power and Ground Pins			
V_{DD}.CORE	100	2.5V Power	Core Voltage
V_{DD}.PAD (Note 2)	15	2.5V or 3.3V Power	Differential Output Buffer Voltage
V_{DD}.IN (Note 1) (Note 3)	16	3.3V Power	LVTTL Control pins Voltage and Differential Input Buffer Voltage
V_{SS}	111	Ground	Ground

The differential output pins powered from 2.5V are 3.3V tolerant.

Note 1: Dedicated differential input buffers can receive both LVDS and LVPECL voltage levels using 3.3V supply.

Note 2: V_{DD}.PAD is 2.5V for OCX256L or 3.3V for OCX256P.

Note 3: The LVTTL control, JTAG pins, and differential input ports are 3.3V—they are not 5V tolerant.

Differential I/O Standards

The OCX256 supports the two most popular differential signaling standards: Low Voltage Differential Signaling (LVDS) and Low Voltage Positive Emitter Coupled Logic (LVPECL).

LVDS is typically used in communication systems as high speed, low noise point-to-point links.

LVPECL is commonly used in video switching applications or those designs requiring transmission of high-speed clock signals.

LVDS

LVDS is a differential signaling standard. It requires that one data bit is carried through two signal lines. As with all differential signaling standards, LVDS has an inherent noise immunity over single-ended standards. The voltage swing between two signal lines is approximately 350mV. The use of a reference voltage or a board termination voltage is not required. LVDS requires the use of two pins per input or output. The OCX256L supports LVDS signalling. Integrated Output Attenuator resistors produce the required LVDS Output swing while providing a 100Ω output impedance to minimize return reflections.

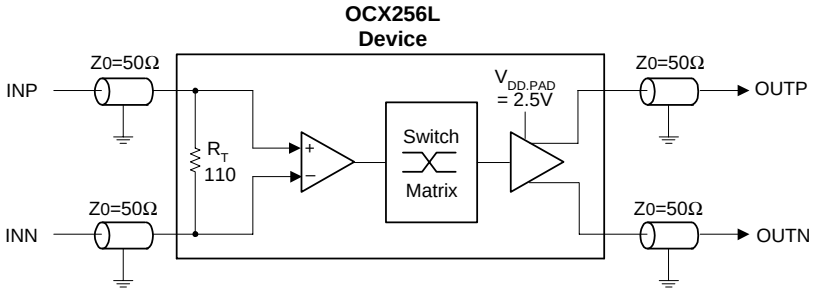


FIGURE 7. OCX256L LVDS Signal Circuit

LVPECL

LVPECL is another differential signaling standard that specifies two pins per input or output. The voltage swing between these two signal lines is approximately 850mV. The use of a reference voltage or a board termination voltage is not required. The OCX256P supports LVPECL signalling. Integrated Output Attenuator resistors produce the required LVPECL Output swing while providing a 100Ω output impedance to minimize return reflections.

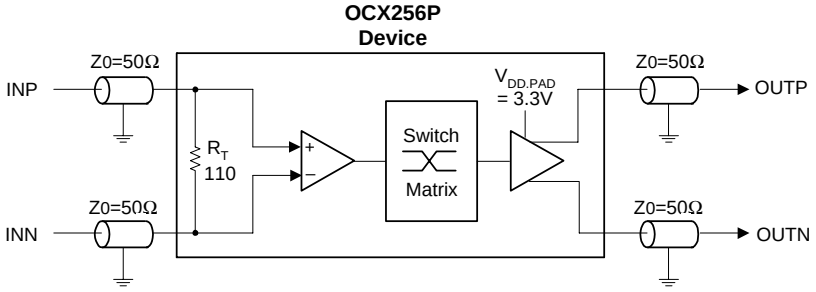


FIGURE 8. OCX256P LVPECL Signal Circuit

Absolute Maximum Ratings(Note 4)

Supply Voltage (Core)	
V_{DD}.CORE	-0.3V to +3.0V
Supply Voltage (Inputs)	
V_{DD}.IN	-0.3V to +3.6V
Supply Voltage (Differential Outputs)	
V_{DD}.PAD	-0.3V to +3.6V
Input Voltage V_{IN} (Note 5)(Note 6)	-0.3V to +3.6V
Junction Temperature T_J	+150°C
Storage Temperature T_{STG}	-65°C to +150°C
Maximum Power Dissipation P_{MAX}	8.6W
Electrostatic Discharge ESD	
(Note 7)	2000V

Recommended Operating Conditions

Supply Voltage (Core)	
V_{DD}.CORE	+2.375V to +2.625V
Supply Voltage	
(Differential Output Buffers)	
V_{DD}.PAD (Note 8)	3.3V ±10% or 2.5V ± 5%
Supply Voltage (Inputs)	
V_{DD}.IN	+3.0V to +3.6V
Operating Temperature T_A	
Commercial	0°C to +70°C
Industrial	-40°C to +85°C

Note 4: Absolute Maximum Ratings: are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 5: A maximum undershoot of 2V for a maximum duration of 20ns is acceptable. Overshoot to 3.6V is acceptable.

Note 6: All inputs are 3.3V tolerant with the V_{DD} pin at 2.5V or 3.3V.

Note 7: Measured using Human Body Model.

Note 8: Note that minimum and maximum values for V_{DD} for differential outputs are I/O Standard dependent.

Pin Capacitance (Note 9)

Symbol	Parameter	Limits	Units
C_{PIN}	Signal Pin Capacitance	10	pF

Note 9: Capacitance measured at 25°C. Sample tested only.

DC Electrical Specifications

(T_A = -40°C to 85°C, V_{DD}.IN = 3.3V ±10%, V_{DD}.CORE = 2.5V ±5%)

Symbol	Parameter	Conditions	Mln	Max	Units
V_{IH}	High Level Input	Ports are 3.3V Tolerant	2.0	3.6	V
V_{IL}	Low Level Input	Ports are 3.3V Tolerant	-0.3	0.8	V
V_{OH}	High Level Output	V_{DD}.PAD = Min I_{OH} = -4 mA	2.4	V_{DD}.PAD + 0.3	V
V_{OL}	Low Level Output	V_{DD}.PAD = Min I_{OL} = 8 mA		0.4	V
IL_{IH}, IL_{IL} (Note 10)	Input Pin Leakage Current (Note 11)	V_{DD}.IN = Max 0.0 < In < V_{DD}.PAD		+5 -50	mA
IL_{OZ}	3-STATE Leakage Output OFF State (Note 11)	V_{DD}.PAD = Max 0.0 < In < V_{DD}.PAD		+5 -5	mA
Power					
P_{DDQ} (Note 12)	Quiescent Power	All V_{DD} = Max		0.7	W

Note 10: All LVTTL input pins have pull-up resistors.

Note 11: Input leakage only valid when both positive and negative inputs/outputs area equal (i.e. both HIGH or both LOW)

Note 12: See Power Consumption for dynamic power consumption calculation.

OCX256L (LVDS) DC Electrical Specifications (V_{DD}.PAD = 2.5V)

Symbol	DC Parameter	Min	Typ	Max	Units
V_{OH}	Output High Voltage for OUTP and OUTN			1.6	V
V_{OL}	Output Low Voltage for OUTP and OUTN	0.90			V
V_{OUT_DIFF}	Differential Output Voltage (Note 13)	±250	±350	±450	mV
V_{OUT_COM}	Output Common-Mode Voltage	1.125	1.25	1.375	V
V_{IN_DIFF}	Differential Input Voltage	±100	±350		mV
V_{IN_COM}	Input Common-Mode Voltage	0.25	1.25	2.25	V
Z_{IN}	Z_{IN} — Termination Impedance	88		132	W

Note 13: Maximum capacitive load is 12 pF.

OCX256P (LVPECL) DC Electrical Specifications (V_{DD}.PAD = 3.3V)

Symbol	DC Parameters	Min	Max	Units
V_{IN_DIFF}	Input Differential Voltage	±100		mV
V_{IN_COM}	Input Common-Mode Voltage	0.25	2.25	V
V_{OUT_DIFF}	Output Differential Voltage	±350	±650	mV
V_{OUT_COM}	Output Common-Mode Voltage	V_{DD}.PAD / 2	V_{DD}.PAD / 2	V
Z_{IN}	Termination Impedance	80	120	W

AC Electrical Specifications (V_{DD}.IN = 3.3V ± 10%, V_{DD}.CORE = 2.5V ± 5%)

Symbol	Parameter	0°C to 70°C		−40°C to +85°C		Units
		Min	Max	Min	Max	
R_{DATA}	NRZ Data Rate (Note 14)		667		667	Mb/s
F_{RO}	Registered Output Clock Frequency (Note 14)		333		333	MHz
t_{W_RO}	Registered Clock Pulse Width, HIGH or LOW (Note 14)	2		2		ns
t_{S_RO}	Registered Output Setup Time to Clock	4		4		ns
t_{H_RO}	Registered Output Clock to Hold Data	0		0		ns
t_{CO_RO}	Registered Output Clock to Data Out Valid		2.5		2.5	ns
t_{PHL}, t_{PLH}	One Way Signal Propagation Delay, Fanout = 1		5.5		6.5	ns
t_{W+}	Input Flow-through Positive Pulse Width	1.5		1.5		ns
t_{W-}	Input Flow-through Negative Pulse Width	1.5		1.5		ns
t_{DCD+}, t_{DCD-}	Duty Cycle Distortion		0.5		0.6	ns
t_{JITTER}	Output Jitter		0.5		0.5	ns
t_{SK}	Skew Between Output Ports (Note 14)		0.5		0.6	ns
t_{PHZ_OT}, t_{PLZ_OT}	Output Enable to Valid Data		3		3	ns
t_{PZH_OT}, t_{PZL_OT}	Output Enable to High Z State		3		3	ns
t_{RC}	RapidConfigure Clock Period	12		12		ns
t_{W+_RC}, t_{W-_RC}	RapidConfigure Clock Pulse Width	5		5		ns
t_{S_RC}	RapidConfigure Address Setup to RC_$\overline{CLK}$	3		4		ns
t_{H_RC}	RapidConfigure Address and Enable Hold Time to RC_$\overline{CLK}$	3		4		ns
t_{P_UD}	Update of Crosspoint to Data Out		10		10	ns
f_{JTAG}	JTAG Clock Frequency (TCK)		20		20	MHz
t_{W_JTAG}	JTAG Clock Pulse Width (TCK) @ 20MHz cycle	20	30	20	30	ns
t_{S_JTAG}	JTAG Setup Time	4		4		ns
t_{H_JTAG}	JTAG Hold Time	0		0		ns
t_{P_JTAG}	JTAG Clock to Output Data Valid (TDO)		20		20	ns

Note 14: These parameters are guaranteed but not tested in production.

Timing Diagrams

For the purpose of clarity, the timing diagrams within this datasheet are conceptual representations only and do not show actual circuit implementation.

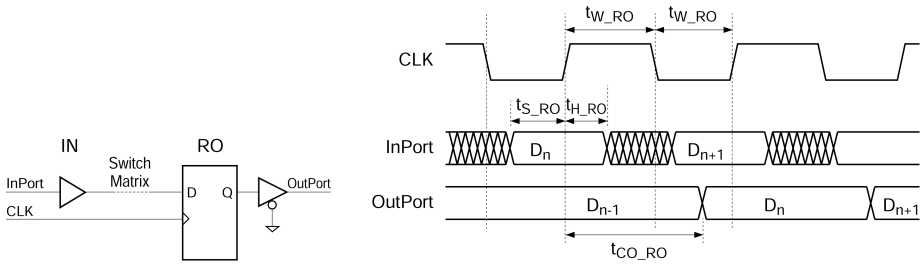


FIGURE 9. Registered Output Mode Timing

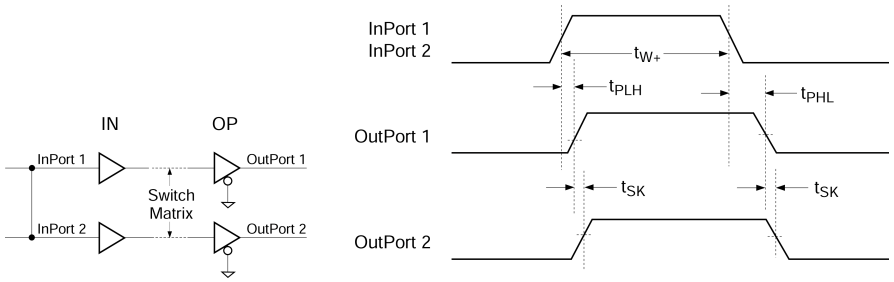


FIGURE 10. Flow-Through Mode Timing

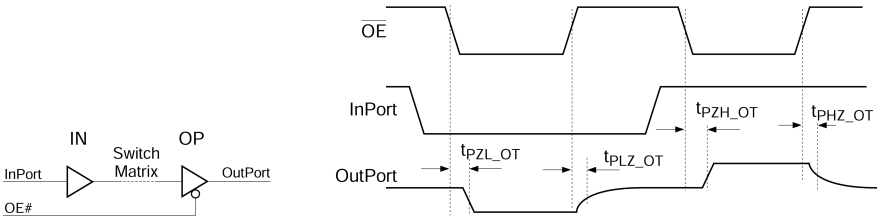


FIGURE 11. Output Enable Timing

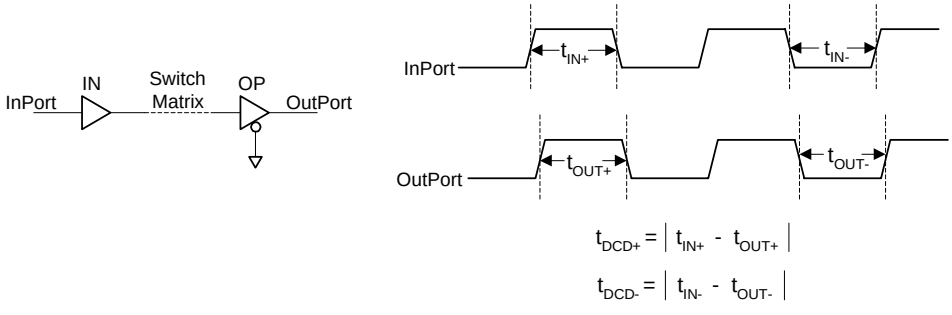


FIGURE 12. Duty Cycle Distortion

Timing Diagrams (Continued)

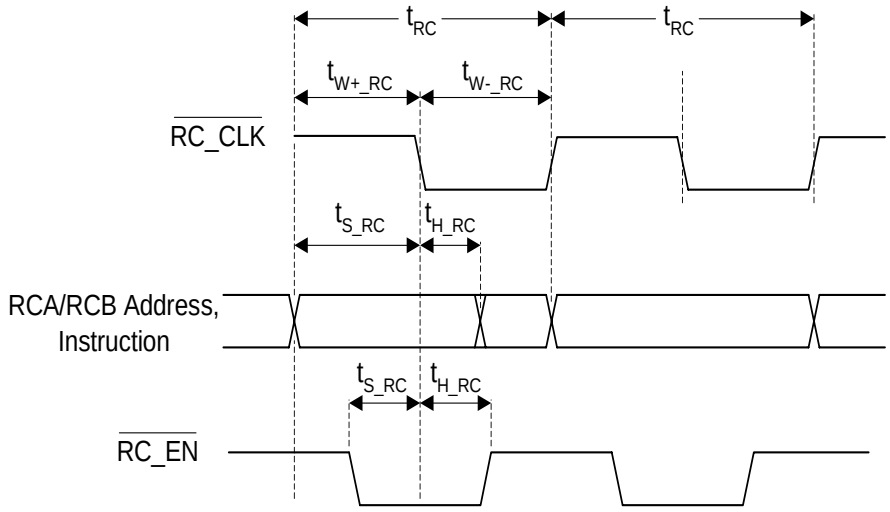


FIGURE 13. Rapid Configure Write Cycle

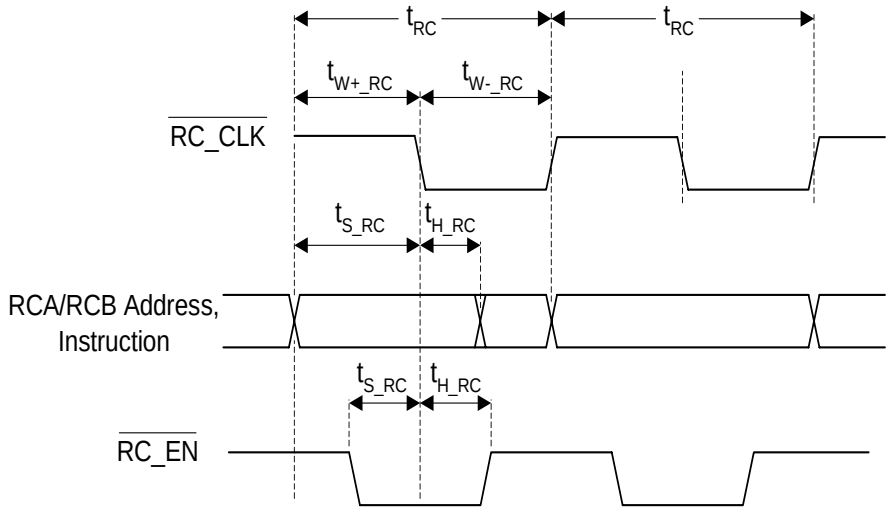


FIGURE 14. Rapid Configure Read Cycle

Timing Diagrams (Continued)

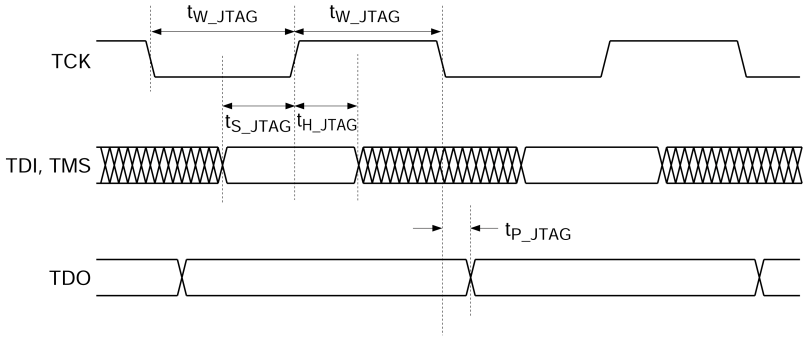


FIGURE 15. JTAG Timing

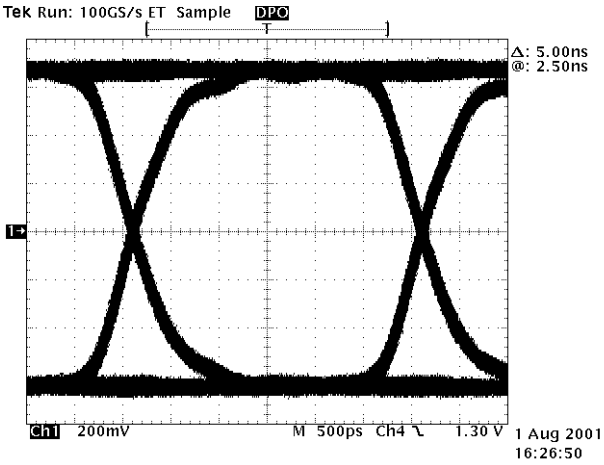


FIGURE 16. Typical Performance at 667 Mb/s with PRBS Data

Package and Pinout

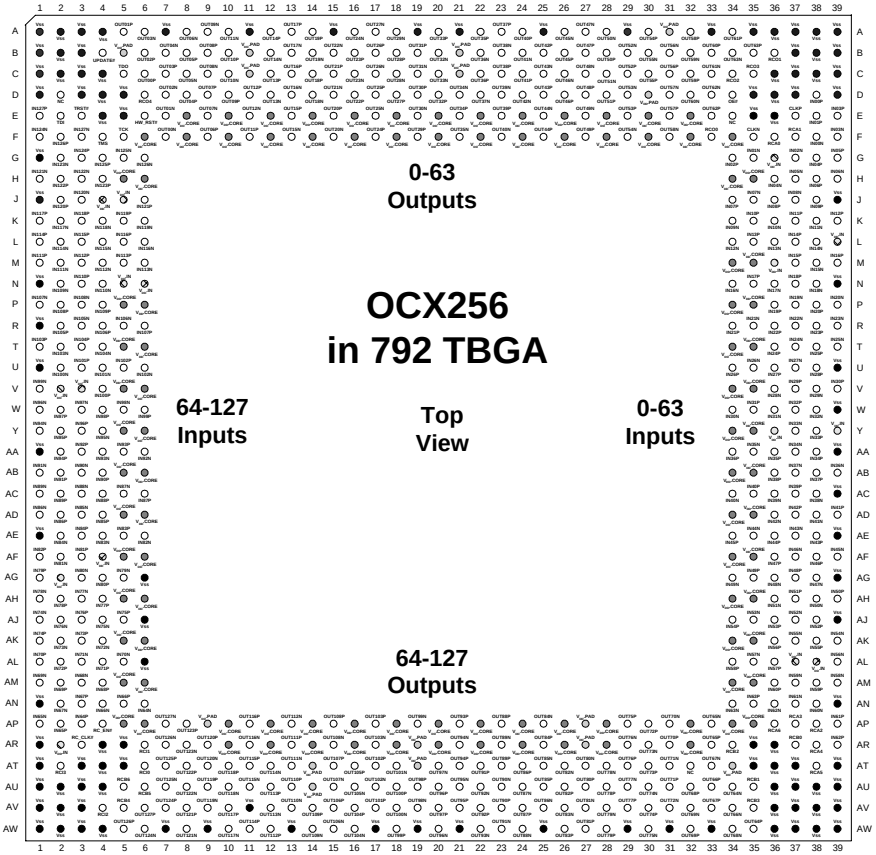


FIGURE 17. OCX256 Package Pinout

Package and Pinout (Continued)

TABLE 14. OCX256 Pinout By Ball Sequence

Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name
A1	V_{SS}	B1	V_{SS}	C1	V_{SS}	D1	V_{SS}	E1	IN127P	F1	IN124N
A2	V_{SS}	B2	V_{SS}	C2	V_{SS}	D2	NC	E2	TDI	F2	IN126P
A3	V_{SS}	B3	V_{SS}	C3	V_{SS}	D3	V_{SS}	E3	$\overline{TRST}$	F3	IN127N
A4	V_{SS}	B4	$\overline{UPDATE}$	C4	V_{SS}	D4	V_{SS}	E4	V_{SS}	F4	TMS
A5	OUT01P	B5	V_{DD}.PAD	C5	TDO	D5	V_{SS}	E5	V_{SS}	F5	TCK
A6	OUT03N	B6	OUT02P	C6	OUT00P	D6	RCO4	E6	$\overline{HW\_RST}$	F6	V_{DD}.CORE
A7	V_{SS}	B7	OUT04N	C7	OUT03P	D7	OUT02N	E7	OUT01N	F7	OUT00N
A8	OUT06N	B8	OUT05P	C8	OUT05N	D8	OUT04P	E8	V_{DD}.COR	F8	V_{DD}.CORE
A9	OUT09N	B9	OUT08P	C9	OUT08N	D9	OUT07P	E9	OUT07N	F9	OUT06N
A10	OUT11N	B10	OUT10P	C10	OUT10N	D10	OUT09P	E10	V_{DD}.COR	F10	V_{DD}.CORE
A11	V_{SS}	B11	V_{DD}.PAD	C11	V_{DD}.PAD	D11	OUT12P	E11	OUT12N	F11	OUT11P
A12	OUT14P	B12	OUT14N	C12	OUT13P	D12	OUT13N	E12	V_{DD}.COR	F12	V_{DD}.CORE
A13	OUT17P	B13	OUT17N	C13	OUT16P	D13	OUT16N	E13	OUT15P	F13	OUT15N
A14	OUT19P	B14	OUT19N	C14	OUT18P	D14	OUT18N	E14	V_{DD}.COR	F14	V_{DD}.CORE
A15	V_{SS}	B15	OUT22N	C15	OUT21P	D15	OUT21N	E15	OUT20P	F15	OUT20N
A16	OUT24N	B16	OUT23P	C16	OUT23N	D16	OUT22P	E16	V_{DD}.COR	F16	V_{DD}.CORE
A17	OUT27N	B17	OUT26P	C17	OUT26N	D17	OUT25P	E17	OUT25N	F17	OUT24P
A18	OUT29N	B18	OUT28P	C18	OUT28N	D18	OUT27P	E18	V_{DD}.COR	F18	V_{DD}.CORE
A19	V_{SS}	B19	OUT31P	C19	OUT31N	D19	OUT30P	E19	OUT30N	F19	OUT29P
A20	OUT33P	B20	OUT32N	C20	OUT33N	D20	OUT32P	E20	V_{DD}.COR	F20	V_{DD}.CORE
A21	V_{SS}	B21	V_{DD}.PAD	C21	V_{DD}.PAD	D21	OUT34N	E21	OUT34P	F21	OUT35N
A22	OUT35P	B22	OUT36N	C22	OUT36P	D22	OUT37N	E22	V_{DD}.COR	F22	V_{DD}.CORE
A23	OUT37P	B23	OUT38N	C23	OUT38P	D23	OUT39N	E23	OUT39P	F23	OUT40N
A24	OUT40P	B24	OUT41N	C24	OUT41P	D24	OUT42N	E24	V_{DD}.COR	F24	V_{DD}.CORE
A25	V_{SS}	B25	OUT42P	C25	OUT43N	D25	OUT43P	E25	OUT44N	F25	OUT44P
A26	OUT45N	B26	OUT45P	C26	OUT46N	D26	OUT46P	E26	V_{DD}.COR	F26	V_{DD}.CORE
A27	OUT47N	B27	OUT47P	C27	OUT48N	D27	OUT48P	E27	OUT49N	F27	OUT49P
A28	OUT50N	B28	OUT50P	C28	OUT51N	D28	OUT51P	E28	V_{DD}.COR	F28	V_{DD}.CORE
A29	V_{SS}	B29	OUT52N	C29	OUT52P	D29	OUT53N	E29	OUT53P	F29	OUT54N
A30	OUT54P	B30	OUT55N	C30	OUT55P	D30	V_{DD}.PAD	E30	V_{DD}.COR	F30	V_{DD}.CORE
A31	V_{DD}.PAD	B31	OUT56N	C31	OUT56P	D31	OUT57N	E31	OUT57P	F31	OUT58N
A32	OUT58P	B32	OUT59N	C32	OUT59P	D32	OUT60N	E32	V_{DD}.COR	F32	V_{DD}.CORE
A33	V_{SS}	B33	OUT60P	C33	OUT61N	D33	OUT62N	E33	OUT62P	F33	RCO0
A34	OUT61P	B34	OUT63N	C34	RCO2	D34	$\overline{OE}$	E34	NC	F34	V_{DD}.CORE
A35	V_{SS}	B35	OUT63P	C35	RCO3	D35	V_{SS}	E35	V_{SS}	F35	CLKN
A36	V_{SS}	B36	RCO1	C36	V_{SS}	D36	V_{SS}	E36	V_{SS}	F36	RCA0
A37	V_{SS}	B37	V_{SS}	C37	V_{SS}	D37	V_{SS}	E37	CLKP	F37	RCA1
A38	V_{SS}	B38	V_{SS}	C38	V_{SS}	D38	IN00P	E38	IN01P	F38	IN00N
A39	V_{SS}	B39	V_{SS}	C39	V_{SS}	D39	V_{SS}	E39	IN03P	F39	IN03N

Package and Pinout (Continued)

Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name
G1	V_{SS}	H1	IN121N	J1	V_{SS}	K1	IN117P	L1	IN114P	M1	IN111P
G2	IN123N	H2	IN122P	J2	IN120P	K2	IN117N	L2	IN114N	M2	IN111N
G3	IN124P	H3	IN122N	J3	IN120N	K3	IN118P	L3	IN115P	M3	IN112P
G4	IN125P	H4	IN123P	J4	V_{DD}.IN	K4	IN118N	L4	IN115N	M4	IN112N
G5	IN125N	H5	V_{DD}.CORE	J5	V_{DD}.IN	K5	IN119P	L5	IN116P	M5	IN113P
G6	IN126N	H6	V_{DD}.CORE	J6	IN121P	K6	IN119N	L6	IN116N	M6	IN113N
G34	IN02P	H34	V_{DD}.CORE	J34	IN07P	K34	IN09N	L34	IN12N	M34	V_{DD}.CORE
G35	IN01N	H35	V_{DD}.CORE	J35	IN07N	K35	IN10P	L35	IN13P	M35	V_{DD}.CORE
G36	V_{DD}.IN	H36	IN04N	J36	IN08P	K36	IN10N	L36	IN13N	M36	V_{DD}.IN
G37	IN02N	H37	IN05N	J37	IN08N	K37	IN11P	L37	IN14P	M37	IN15P
G38	IN04P	H38	IN06P	J38	IN09P	K38	IN11N	L38	IN14N	M38	IN15N
G39	IN05P	H39	IN06N	J39	Vss	K39	IN12P	L39	Vdd.IN	M39	IN16P
N1	V_{SS}	P1	IN107N	R1	V_{SS}	T1	IN103P	U1	V_{SS}	V1	IN99N
N2	IN109N	P2	IN108P	R2	IN105P	T2	IN103N	U2	IN100N	V2	V_{DD}.IN
N3	IN110P	P3	IN108N	R3	IN105N	T3	IN104P	U3	IN101P	V3	V_{DD}.IN
N4	IN110N	P4	IN109P	R4	IN106P	T4	IN104N	U4	IN101N	V4	IN100P
N5	V_{DD}.IN	P5	V_{DD}.CORE	R5	IN106N	T5	V_{DD}.CORE	U5	IN102P	V5	V_{DD}.CORE
N6	V_{DD}.IN	P6	V_{DD}.CORE	R6	IN107P	T6	V_{DD}.CORE	U6	IN102N	V6	V_{DD}.CORE
N34	IN16N	P34	V_{DD}.CORE	R34	IN21P	T34	V_{DD}.CORE	U34	IN26P	V34	V_{DD}.CORE
N35	IN17P	P35	V_{DD}.CORE	R35	IN21N	T35	V_{DD}.CORE	U35	IN26N	V35	V_{DD}.CORE
N36	IN17N	P36	IN19P	R36	IN22P	T36	IN24P	U36	IN27P	V36	IN28N
N37	IN18P	P37	IN19N	R37	IN22N	T37	IN24N	U37	IN27N	V37	IN29P
N38	IN18N	P38	IN20P	R38	IN23P	T38	IN25P	U38	IN28P	V38	IN29N
N39	V_{SS}	P39	IN20N	R39	IN23N	T39	IN25N	U39	V_{SS}	V39	IN30P
W1	IN96N	Y1	IN94N	AA1	V_{SS}	AB1	IN91N	AC1	IN89N	AD1	IN86N
W2	IN97P	Y2	IN95P	AA2	IN94P	AB2	IN91P	AC2	IN89P	AD2	IN86P
W3	IN97N	Y3	IN96P	AA3	IN92P	AB3	IN90N	AC3	IN88N	AD3	IN85N
W4	IN98P	Y4	IN95N	AA4	IN93N	AB4	IN90P	AC4	IN88P	AD4	IN85P
W5	IN98N	Y5	V_{DD}.CORE	AA5	IN93P	AB5	V_{DD}.CORE	AC5	IN87N	AD5	V_{DD}.CORE
W6	IN99P	Y6	V_{DD}.CORE	AA6	IN92N	AB6	V_{DD}.CORE	AC6	IN87P	AD6	V_{DD}.CORE
W34	IN30N	Y34	V_{DD}.CORE	AA34	IN36P	AB34	V_{DD}.CORE	AC34	IN40N	AD34	V_{DD}.CORE
W35	IN31P	Y35	V_{DD}.CORE	AA35	IN35N	AB35	V_{DD}.CORE	AC35	IN40P	AD35	V_{DD}.CORE
W36	IN31N	Y36	V_{DD}.IN	AA36	IN35P	AB36	IN38P	AC36	IN39N	AD36	IN42N
W37	IN32P	Y37	IN33N	AA37	IN34N	AB37	IN37N	AC37	IN39P	AD37	IN42P
W38	IN32N	Y38	IN33P	AA38	IN34P	AB38	IN37P	AC38	IN38N	AD38	IN41N
W39	V_{SS}	Y39	V_{DD}.IN	AA39	V_{SS}	AB39	IN36N	AC39	V_{SS}	AD39	IN41P

Package and Pinout (Continued)

Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name
AE1	V_{SS}	AF1	IN82P	AG1	IN79P	AH1	IN78N	AJ1	IN74N	AK1	IN74P
AE2	IN84N	AF2	IN81N	AG2	V_{DD}.IN	AH2	IN78P	AJ2	IN76N	AK2	IN73N
AE3	IN84P	AF3	IN81P	AG3	IN80N	AH3	IN77N	AJ3	IN76P	AK3	IN73P
AE4	IN83N	AF4	V_{DD}.IN	AG4	IN80P	AH4	IN77P	AJ4	IN75N	AK4	IN72N
AE5	IN83P	AF5	V_{DD}.CORE	AG5	IN79N	AH5	V_{DD}.CORE	AJ5	IN75P	AK5	V_{DD}.CORE
AE6	IN82N	AF6	V_{DD}.CORE	AG6	V_{SS}	AH6	V_{DD}.CORE	AJ6	V_{SS}	AK6	V_{DD}.CORE
AE34	IN45P	AF34	V_{DD}.CORE	AG34	IN49N	AH34	V_{DD}.CORE	AJ34	IN54P	AK34	V_{DD}.CORE
AE35	IN44N	AF35	V_{DD}.CORE	AG35	IN49P	AH35	V_{DD}.CORE	AJ35	IN53N	AK35	V_{DD}.CORE
AE36	IN44P	AF36	IN47P	AG36	IN48N	AH36	IN51N	AJ36	IN53P	AK36	IN56P
AE37	IN43N	AF37	IN46N	AG37	IN48P	AH37	IN51P	AJ37	IN52N	AK37	IN55N
AE38	IN43P	AF38	IN46P	AG38	IN47N	AH38	IN50N	AJ38	IN52P	AK38	IN55P
AE39	V_{SS}	AF39	IN45N	AG39	V_{SS}	AH39	IN50P	AJ39	V_{SS}	AK39	IN54N

AL1	IN70P	AM1	IN69N	AN1	V_{SS}
AL2	IN72P	AM2	IN69P	AN2	IN67N
AL3	IN71N	AM3	IN68N	AN3	IN67P
AL4	IN71P	AM4	IN68P	AN4	IN66N
AL5	IN70N	AM5	V_{DD}.CORE	AN5	IN66P
AL6	V_{SS}	AM6	V_{DD}.CORE	AN6	IN64N
AL34	IN58P	AM34	V_{DD}.CORE	AN34	IN63N
AL35	IN57N	AM35	V_{DD}.CORE	AN35	IN63P
AL36	IN57P	AM36	IN60P	AN36	IN62N
AL37	V_{DD}.IN	AM37	IN59N	AN37	IN61N
AL38	V_{DD}.IN	AM38	IN59P	AN38	IN60N
AL39	IN56N	AM39	IN58N	AN39	V_{SS}

Package and Pinout (Continued)

Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name
AP1	IN65N	AR1	V_{SS}	AT1	V_{SS}	AU1	V_{SS}	AV1	V_{SS}	AW1	V_{SS}
AP2	IN65P	AR2	V_{DD}.IN	AT2	RCI3	AU2	V_{SS}	AV2	V_{SS}	AW2	V_{SS}
AP3	IN64P	AR3	$\overline{RC\_CLK}$	AT3	V_{SS}	AU3	V_{SS}	AV3	V_{SS}	AW3	V_{SS}
AP4	$\overline{RC\_EN}$	AR4	V_{SS}	AT4	V_{SS}	AU4	V_{SS}	AV4	RCI2	AW4	V_{SS}
AP5	V_{DD}.CORE	AR5	V_{SS}	AT5	V_{SS}	AU5	RCB6	AV5	RCB4	AW5	OUT126P
AP6	V_{DD}.CORE	AR6	RCI1	AT6	RCI0	AU6	RCB5	AV6	OUT127P	AW6	OUT124N
AP7	OUT127N	AR7	OUT126N	AT7	OUT125P	AU7	OUT125N	AV7	OUT124P	AW7	V_{SS}
AP8	OUT123P	AR8	OUT123N	AT8	OUT122P	AU8	OUT122N	AV8	OUT121P	AW8	OUT121N
AP9	V_{DD}.PAD	AR9	OUT120P	AT9	OUT120N	AU9	OUT119P	AV9	OUT119N	AW9	V_{SS}
AP10	V_{DD}.CORE	AR10	V_{DD}.CORE	AT10	OUT118P	AU10	OUT118N	AV10	OUT117P	AW10	OUT117N
AP11	OUT116P	AR11	OUT116N	AT11	OUT115P	AU11	OUT115N	AV11	V_{SS}	AW11	OUT114P
AP12	V_{DD}.CORE	AR12	V_{DD}.CORE	AT12	OUT114N	AU12	OUT113P	AV12	OUT113N	AW12	OUT112P
AP13	OUT112N	AR13	OUT111P	AT13	OUT111N	AU13	OUT110P	AV13	OUT110N	AW13	V_{SS}
AP14	V_{DD}.CORE	AR14	V_{DD}.CORE	AT14	V_{DD}.PAD	AU14	V_{DD}.PAD	AV14	OUT109P	AW14	OUT109N
AP15	OUT108P	AR15	OUT108N	AT15	OUT107P	AU15	OUT107N	AV15	OUT106P	AW15	OUT106N
AP16	V_{DD}.CORE	AR16	V_{DD}.CORE	AT16	OUT105P	AU16	OUT105N	AV16	OUT104P	AW16	OUT104N
AP17	OUT103P	AR17	OUT103N	AT17	OUT102P	AU17	OUT102N	AV17	OUT101P	AW17	V_{SS}
AP18	V_{DD}.CORE	AR18	V_{DD}.CORE	AT18	OUT101N	AU18	OUT100P	AV18	OUT100N	AW18	OUT99P
AP19	OUT99N	AR19	V_{DD}.PAD	AT19	V_{DD}.PAD	AU19	OUT98P	AV19	OUT98N	AW19	V_{SS}
AP20	V_{DD}.CORE	AR20	V_{DD}.CORE	AT20	OUT97N	AU20	OUT96P	AV20	OUT97P	AW20	OUT96N
AP21	OUT93P	AR21	OUT94N	AT21	OUT94P	AU21	OUT95N	AV21	OUT95P	AW21	V_{SS}
AP22	V_{DD}.CORE	AR22	V_{DD}.CORE	AT22	OUT91P	AU22	OUT92N	AV22	OUT92P	AW22	OUT93N
AP23	OUT88P	AR23	OUT89N	AT23	OUT89P	AU23	OUT90N	AV23	OUT90P	AW23	OUT91N
AP24	V_{DD}.CORE	AR24	V_{DD}.CORE	AT24	OUT86P	AU24	OUT87N	AV24	OUT87P	AW24	OUT88N
AP25	OUT84N	AR25	OUT84P	AT25	OUT85N	AU25	OUT85P	AV25	OUT86N	AW25	V_{SS}
AP26	V_{DD}.CORE	AR26	V_{DD}.CORE	AT26	OUT82N	AU26	OUT82P	AV26	OUT83N	AW26	OUT83P
AP27	V_{DD}.PAD	AR27	V_{DD}.PAD	AT27	OUT80N	AU27	OUT80P	AV27	OUT81N	AW27	OUT81P
AP28	V_{DD}.CORE	AR28	V_{DD}.CORE	AT28	OUT78N	AU28	OUT78P	AV28	OUT79N	AW28	OUT79P
AP29	OUT75P	AR29	OUT76N	AT29	OUT76P	AU29	OUT77N	AV29	OUT77P	AW29	V_{SS}
AP30	OUT72P	AR30	OUT73N	AT30	OUT73P	AU30	OUT74N	AV30	OUT74P	AW30	OUT75N
AP31	OUT70N	AR31	OUT70P	AT31	OUT71N	AU31	OUT71P	AV31	OUT72N	AW31	V_{SS}
AP32	V_{DD}.CORE	AR32	V_{DD}.CORE	AT32	NC	AU32	OUT68P	AV32	OUT69N	AW32	OUT69P
AP33	OUT65N	AR33	OUT65P	AT33	OUT67N	AU33	OUT66P	AV33	OUT67P	AW33	V_{SS}
AP34	V_{DD}.CORE	AR34	RCB2	AT34	V_{DD}.PAD	AU34	OUT64N	AV34	OUT66N	AW34	OUT68N
AP35	V_{DD}.CORE	AR35	V_{SS}	AT35	V_{SS}	AU35	RCB1	AV35	RCB3	AW35	OUT64P
AP36	RCA6	AR36	V_{SS}	AT36	V_{SS}	AU36	V_{SS}	AV36	V_{SS}	AW36	V_{SS}
AP37	RCA3	AR37	RCB0	AT37	V_{SS}	AU37	V_{SS}	AV37	V_{SS}	AW37	V_{SS}
AP38	RCA2	AR38	RCA4	AT38	RCA5	AU38	Vss	AV38	Vss	AW38	Vss
AP39	IN61P	AR39	IN62P	AT39	V_{SS}	AU39	V_{SS}	AV39	V_{SS}	AW39	V_{SS}

Package and Pinout (Continued)

TABLE 15. OCX256 Pinout By Ball Name

Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #
CLKN	F35	IN21P	R34	IN44P	AE36	IN67P	AN3	IN90P	AB4
CLKP	E37	IN22N	R37	IN45N	AF39	IN68N	AM3	IN91N	AB1
$\overline{\text{HW\_RST}}$	E6	IN22P	R36	IN45P	AE34	IN68P	AM4	IN91P	AB2
IN00N	F38	IN23N	R39	IN46N	AF37	IN69N	AM1	IN92N	AA6
IN00P	D38	IN23P	R38	IN46P	AF38	IN69P	AM2	IN92P	AA3
IN01N	G35	IN24N	T37	IN47N	AG38	IN70N	AL5	IN93N	AA4
IN01P	E38	IN24P	T36	IN47P	AF36	IN70P	AL1	IN93P	AA5
IN02N	G37	IN25N	T39	IN48N	AG36	IN71N	AL3	IN94N	Y1
IN02P	G34	IN25P	T38	IN48P	AG37	IN71P	AL4	IN94P	AA2
IN03N	F39	IN26N	U35	IN49N	AG34	IN72N	AK4	IN95N	Y4
IN03P	E39	IN26P	U34	IN49P	AG35	IN72P	AL2	IN95P	Y2
IN04N	H36	IN27N	U37	IN50N	AH38	IN73N	AK2	IN96N	W1
IN04P	G38	IN27P	U36	IN50P	AH39	IN73P	AK3	IN96P	Y3
IN05N	H37	IN28N	V36	IN51N	AH36	IN74N	AJ1	IN97N	W3
IN05P	G39	IN28P	U38	IN51P	AH37	IN74P	AK1	IN97P	W2
IN06N	H39	IN29N	V38	IN52N	AJ37	IN75N	AJ4	IN98N	W5
IN06P	H38	IN29P	V37	IN52P	AJ38	IN75P	AJ5	IN98P	W4
IN07N	J35	IN30N	W34	IN53N	AJ35	IN76N	AJ2	IN99N	V1
IN07P	J34	IN30P	V39	IN53P	AJ36	IN76P	AJ3	IN99P	W6
IN08N	J37	IN31N	W36	IN54N	AK39	IN77N	AH3	IN100N	U2
IN08P	J36	IN31P	W35	IN54P	AJ34	IN77P	AH4	IN100P	V4
IN09N	K34	IN32N	W38	IN55N	AK37	IN78N	AH1	IN101N	U4
IN09P	J38	IN32P	W37	IN55P	AK38	IN78P	AH2	IN101P	U3
IN10N	K36	IN33N	Y37	IN56N	AL39	IN79N	AG5	IN102N	U6
IN10P	K35	IN33P	Y38	IN56P	AK36	IN79P	AG1	IN102P	U5
IN11N	K38	IN34N	AA37	IN57N	AL35	IN80N	AG3	IN103N	T2
IN11P	K37	IN34P	AA38	IN57P	AL36	IN80P	AG4	IN103P	T1
IN12N	L34	IN35N	AA35	IN58N	AM39	IN81N	AF2	IN104N	T4
IN12P	K39	IN35P	AA36	IN58P	AL34	IN81P	AF3	IN104P	T3
IN13N	L36	IN36N	AB39	IN59N	AM37	IN82N	AE6	IN105N	R3
IN13P	L35	IN36P	AA34	IN59P	AM38	IN82P	AF1	IN105P	R2
IN14N	L38	IN37N	AB37	IN60N	AN38	IN83N	AE4	IN106N	R5
IN14P	L37	IN37P	AB38	IN60P	AM36	IN83P	AE5	IN106P	R4
IN15N	M38	IN38N	AC38	IN61N	AN37	IN84N	AE2	IN107N	P1
IN15P	M37	IN38P	AB36	IN61P	AP39	IN84P	AE3	IN107P	R6
IN16N	N34	IN39N	AC36	IN62N	AN36	IN85N	AD3	IN108N	P3
IN16P	M39	IN39P	AC37	IN62P	AR39	IN85P	AD4	IN108P	P2
IN17N	N36	IN40N	AC34	IN63N	AN34	IN86N	AD1	IN109N	N2
IN17P	N35	IN40P	AC35	IN63P	AN35	IN86P	AD2	IN109P	P4
IN18N	N38	IN41N	AD38	IN64N	AN6	IN87N	AC5	IN110N	N4
IN18P	N37	IN41P	AD39	IN64P	AP3	IN87P	AC6	IN110P	N3
IN19N	P37	IN42N	AD36	IN65N	AP1	IN88N	AC3	IN111N	M2
IN19P	P36	IN42P	AD37	IN65P	AP2	IN88P	AC4	IN111P	M1
IN20N	P39	IN43N	AE37	IN66N	AN4	IN89N	AC1	IN112N	M4
IN20P	P38	IN43P	AE38	IN66P	AN5	IN89P	AC2	IN112P	M3
IN21N	R35	IN44N	AE35	IN67N	AN2	IN90N	AB3	IN113N	M6

Package and Pinout (Continued)

Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #
IN113P	M5	OUT07P	D9	OUT30N	E19	OUT54P	A30	OUT77N	AU29
IN114N	L2	OUT07N	E9	OUT31P	B19	OUT54N	F29	OUT78P	AU28
IN114P	L1	OUT08P	B9	OUT31N	C19	OUT55P	C30	OUT78N	AT28
IN115N	L4	OUT08N	C9	OUT32P	D20	OUT55N	B30	OUT79P	AW28
IN115P	L3	OUT09P	D10	OUT32N	B20	OUT56P	C31	OUT79N	AV28
IN116N	L6	OUT09N	A9	OUT33P	A20	OUT56N	B31	OUT80P	AU27
IN116P	L5	OUT10P	B10	OUT33N	C20	OUT57P	E31	OUT80N	AT27
IN117N	K2	OUT10N	C10	OUT34P	E21	OUT57N	D31	OUT81P	AW27
IN117P	K1	OUT11P	F11	OUT34N	D21	OUT58P	A32	OUT81N	AV27
IN118N	K4	OUT11N	A10	OUT35P	A22	OUT58N	F31	OUT82P	AU26
IN118P	K3	OUT12P	D11	OUT35N	F21	OUT59P	C32	OUT82N	AT26
IN119N	K6	OUT12N	E11	OUT36P	C22	OUT59N	B32	OUT83P	AW26
IN119P	K5	OUT13P	C12	OUT36N	B22	OUT60P	B33	OUT83N	AV26
IN120N	J3	OUT13N	D12	OUT37P	A23	OUT60N	D32	OUT84P	AR25
IN120P	J2	OUT14P	A12	OUT37N	D22	OUT61P	A34	OUT84N	AP25
IN121N	H1	OUT14N	B12	OUT38P	C23	OUT61N	C33	OUT85P	AU25
IN121P	J6	OUT15P	E13	OUT38N	B23	OUT62P	E33	OUT85N	AT25
IN122N	H3	OUT15N	F13	OUT39P	E23	OUT62N	D33	OUT86P	AT24
IN122P	H2	OUT16P	C13	OUT39N	D23	OUT63P	B35	OUT86N	AV25
IN123N	G2	OUT16N	D13	OUT40P	A24	OUT63N	B34	OUT87P	AV24
IN123P	H4	OUT17P	A13	OUT40N	F23	OUT64P	AW35	OUT87N	AU24
IN124N	F1	OUT17N	B13	OUT41P	C24	OUT64N	AU34	OUT88P	AP23
IN124P	G3	OUT18P	C14	OUT41N	B24	OUT65P	AR33	OUT88N	AW24
IN125N	G5	OUT18N	D14	OUT42P	B25	OUT65N	AP33	OUT89P	AT23
IN125P	G4	OUT19P	A14	OUT42N	D24	OUT66P	AU33	OUT89N	AR23
IN126N	G6	OUT19N	B14	OUT43P	D25	OUT66N	AV34	OUT90P	AV23
IN126P	F2	OUT20P	E15	OUT43N	C25	OUT67P	AV33	OUT90N	AU23
IN127N	F3	OUT20N	F15	OUT44P	F25	OUT67N	AT33	OUT91P	AT22
IN127P	E1	OUT21P	C15	OUT44N	E25	OUT68P	AU32	OUT91N	AW23
NC	E34	OUT21N	D15	OUT45P	B26	OUT68N	AW34	OUT92P	AV22
NC	D2	OUT22P	D16	OUT45N	A26	OUT69P	AW32	OUT92N	AU22
NC	AT32	OUT22N	B15	OUT46P	D26	OUT69N	AV32	OUT93P	AP21
$\overline{OE}$	D34	OUT23P	B16	OUT46N	C26	OUT70P	AR31	OUT93N	AW22
OUT00P	C6	OUT23N	C16	OUT47P	B27	OUT70N	AP31	OUT94P	AT21
OUT00N	F7	OUT24P	F17	OUT47N	A27	OUT71P	AU31	OUT94N	AR21
OUT01P	A5	OUT24N	A16	OUT48P	D27	OUT71N	AT31	OUT95P	AV21
OUT01N	E7	OUT25P	D17	OUT48N	C27	OUT72P	AP30	OUT95N	AU21
OUT02P	B6	OUT25N	E17	OUT49P	F27	OUT72N	AV31	OUT96P	AU20
OUT02N	D7	OUT26P	B17	OUT49N	E27	OUT73P	AT30	OUT96N	AW20
OUT03P	C7	OUT26N	C17	OUT50P	B28	OUT73N	AR30	OUT97P	AV20
OUT03N	A6	OUT27P	D18	OUT50N	A28	OUT74P	AV30	OUT97N	AT20
OUT04P	D8	OUT27N	A17	OUT51P	D28	OUT74N	AU30	OUT98P	AU19
OUT04N	B7	OUT28P	B18	OUT51N	C28	OUT75P	AP29	OUT98N	AV19
OUT05P	B8	OUT28N	C18	OUT52P	C29	OUT75N	AW30	OUT99P	AW18
OUT05N	C8	OUT29P	F19	OUT52N	B29	OUT76P	AT29	OUT99N	AP19
OUT06P	F9	OUT29N	A18	OUT53P	E29	OUT76N	AR29	OUT100P	AU18
OUT06N	A8	OUT30P	D19	OUT53N	D29	OUT77P	AV29	OUT100N	AV18

Package and Pinout (Continued)

Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #
OUT101P	AV17	OUT124N	AW6	V_{DD}.CORE	E26	V_{DD}.CORE	AD34	V_{DD}.IN	J4
OUT101N	AT18	OUT125P	AT7	V_{DD}.CORE	E28	V_{DD}.CORE	AD35	V_{DD}.IN	J5
OUT102P	AT17	OUT125N	AU7	V_{DD}.CORE	E30	V_{DD}.CORE	AF5	V_{DD}.IN	L39
OUT102N	AU17	OUT126P	AW5	V_{DD}.CORE	E32	V_{DD}.CORE	AF6	V_{DD}.IN	M36
OUT103P	AP17	OUT126N	AR7	V_{DD}.CORE	F6	V_{DD}.CORE	AF34	V_{DD}.IN	V2
OUT103N	AR17	OUT127P	AV6	V_{DD}.CORE	F8	V_{DD}.CORE	AF35	V_{DD}.IN	V3
OUT104P	AV16	OUT127N	AP7	V_{DD}.CORE	F10	V_{DD}.CORE	AH5	V_{DD}.IN	Y36
OUT104N	AW16	RCA0	F36	V_{DD}.CORE	F12	V_{DD}.CORE	AH6	V_{DD}.IN	Y39
OUT105P	AT16	RCA1	F37	V_{DD}.CORE	F14	V_{DD}.CORE	AH34	V_{DD}.IN	AF4
OUT105N	AU16	RCA2	AP38	V_{DD}.CORE	F16	V_{DD}.CORE	AH35	V_{DD}.IN	AG2
OUT106P	AV15	RCA3	AP37	V_{DD}.CORE	F18	V_{DD}.CORE	AK5	V_{DD}.IN	AL37
OUT106N	AW15	RCA4	AR38	V_{DD}.CORE	F20	V_{DD}.CORE	AK6	V_{DD}.IN	AL38
OUT107P	AT15	RCA5	AT38	V_{DD}.COR	F22	V_{DD}.CORE	AK34	V_{DD}.IN	AR2
OUT107N	AU15	RCA6	AP36	V_{DD}.COR	F24	V_{DD}.CORE	AK35	V_{DD}.PAD	A31
OUT108P	AP15	RCB0	AR37	V_{DD}.CORE	F26	V_{DD}.CORE	AM5	V_{DD}.PAD	B5
OUT108N	AR15	RCB1	AU35	V_{DD}.CORE	F28	V_{DD}.CORE	AM6	V_{DD}.PAD	B11
OUT109P	AV14	RCB2	AR34	V_{DD}.CORE	F30	V_{DD}.CORE	AM34	V_{DD}.PAD	B21
OUT109N	AW14	RCB3	AV35	V_{DD}.CORE	F32	V_{DD}.CORE	AM35	V_{DD}.PAD	C11
OUT110P	AU13	RCB4	AV5	V_{DD}.CORE	F34	V_{DD}.CORE	AP5	V_{DD}.PAD	C21
OUT110N	AV13	RCB5	AU6	V_{DD}.CORE	H5	V_{DD}.CORE	AP6	V_{DD}.PAD	D30
OUT111P	AR13	RCB6	AU5	V_{DD}.CORE	H6	V_{DD}.CORE	AP10	V_{DD}.PAD	AP9
OUT111N	AT13	$\overline{\text{RC\_CLK}}$	AR3	V_{DD}.CORE	H34	V_{DD}.CORE	AP12	V_{DD}.PAD	AP27
OUT112P	AW12	$\overline{\text{RC\_EN}}$	AP4	V_{DD}.CORE	H35	V_{DD}.CORE	AP14	V_{DD}.PAD	AR19
OUT112N	AP13	RCI0	AT6	V_{DD}.CORE	M34	V_{DD}.CORE	AP16	V_{DD}.PAD	AR27
OUT113P	AU12	RCI1	AR6	V_{DD}.CORE	M35	V_{DD}.CORE	AP18	V_{DD}.PAD	AT14
OUT113N	AV12	RCI2	AV4	V_{DD}.CORE	P5	V_{DD}.CORE	AP20	V_{DD}.PAD	AT19
OUT114P	AW11	RCI3	AT2	V_{DD}.CORE	P6	V_{DD}.CORE	AP22	V_{DD}.PAD	AT34
OUT114N	AT12	RCO0	F33	V_{DD}.CORE	P34	V_{DD}.CORE	AP24	V_{DD}.PAD	AU14
OUT115P	AT11	RCO1	B36	V_{DD}.CORE	P35	V_{DD}.CORE	AP26	V_{SS}	A1
OUT115N	AU11	RCO2	C34	V_{DD}.CORE	T5	V_{DD}.CORE	AP28	V_{SS}	A2
OUT116P	AP11	RCO3	C35	V_{DD}.CORE	T6	V_{DD}.CORE	AP32	V_{SS}	A3
OUT116N	AR11	RCO4	D6	V_{DD}.CORE	T34	V_{DD}.CORRE	AP34	V_{SS}	A4
OUT117P	AV10	TCK	F5	V_{DD}.CORE	T35	V_{DD}.CORE	AP35	V_{SS}	A7
OUT117N	AW10	TDI	E2	V_{DD}.CORE	V5	V_{DD}.CORE	AR10	V_{SS}	A11
OUT118P	AT10	TDO	C5	V_{DD}.CORE	V6	V_{DD}.CORE	AR12	V_{SS}	A15
OUT118N	AU10	TMS	F4	V_{DD}.CORE	V34	V_{DD}.CORE	AR14	V_{SS}	A19
OUT119P	AU9	$\overline{\text{TRST}}$	E3	V_{DD}.CORE	V35	V_{DD}.CORE	AR16	V_{SS}	A21
OUT119N	AV9	$\overline{\text{UPDATE}}$	B4	V_{DD}.CORE	Y5	V_{DD}.CORE	AR18	V_{SS}	A25
OUT120P	AR9	V_{DD}.CORE	E8	V_{DD}.CORE	Y6	V_{DD}.CORE	AR20	V_{SS}	A29
OUT120N	AT9	V_{DD}.CORE	E10	V_{DD}.CORE	Y34	V_{DD}.CORE	AR22	V_{SS}	A33
OUT121P	AV8	V_{DD}.CORE	E12	V_{DD}.CORE	Y35	V_{DD}.CORE	AR24	V_{SS}	A35
OUT121N	AW8	V_{DD}.CORE	E14	V_{DD}.COR	AB5	V_{DD}.CORE	AR26	V_{SS}	A36
OUT122P	AT8	V_{DD}.CORE	E16	V_{DD}.CORE	AB6	V_{DD}.CORE	AR28	V_{SS}	A37
OUT122N	AU8	V_{DD}.CORE	E18	V_{DD}.CORE	AB34	V_{DD}.CORE	AR32	V_{SS}	A38
OUT123P	AP8	V_{DD}.CORE	E20	V_{DD}.CORE	AB35	V_{DD}.IN	N6	V_{SS}	A39
OUT123N	AR8	V_{DD}.CORE	E22	V_{DD}.CORE	AD5	V_{DD}.IN	N5	V_{SS}	B1
OUT124P	AV7	V_{DD}.CORE	E24	V_{DD}.CORE	AD6	V_{DD}.IN	G36	V_{SS}	B2

Package and Pinout (Continued)

Ball Name	Ball #	Ball Name	Ball #
V_{SS}	B3	V_{SS}	AR5
Vss	B37	V_{SS}	AR35
V_{SS}	B38	V_{SS}	AR36
V_{SS}	B39	V_{SS}	AT1
V_{SS}	C1	V_{SS}	AT3
V_{SS}	C2	V_{SS}	AT4
V_{SS}	C3	V_{SS}	AT5
V_{SS}	C4	V_{SS}	AT35
V_{SS}	C36	V_{SS}	AT36
V_{SS}	C37	V_{SS}	AT37
V_{SS}	C38	V_{SS}	AT39
V_{SS}	C39	V_{SS}	AU1
V_{SS}	D1	V_{SS}	AU2
V_{SS}	D3	V_{SS}	AU3
V_{SS}	D4	V_{SS}	AU4
V_{SS}	D5	V_{SS}	AU36
V_{SS}	D35	V_{SS}	AU37
V_{SS}	D36	V_{SS}	AU38
V_{SS}	D37	V_{SS}	AU39
V_{SS}	D39	V_{SS}	AV1
V_{SS}	E4	V_{SS}	AV2
V_{SS}	E5	V_{SS}	AV3
V_{SS}	E35	V_{SS}	AV11
V_{SS}	E36	V_{SS}	AV36
V_{SS}	G1	V_{SS}	AV37
V_{SS}	J1	V_{SS}	AV38
V_{SS}	J39	V_{SS}	AV39
V_{SS}	N1	V_{SS}	AW1
V_{SS}	N39	V_{SS}	AW2
V_{SS}	R1	V_{SS}	AW3
V_{SS}	U1	V_{SS}	AW4
V_{SS}	U39	V_{SS}	AW7
V_{SS}	W39	V_{SS}	AW9
V_{SS}	AA1	V_{SS}	AW13
V_{SS}	AA39	V_{SS}	AW17
V_{SS}	AC39	V_{SS}	AW19
V_{SS}	AE1	V_{SS}	AW21
V_{SS}	AE39	V_{SS}	AW25
V_{SS}	AG6	V_{SS}	AW29
V_{SS}	AG39	V_{SS}	AW31
V_{SS}	AJ6	V_{SS}	AW33
V_{SS}	AJ39	V_{SS}	AW36
V_{SS}	AL6	V_{SS}	AW37
V_{SS}	AN1	V_{SS}	AW38
V_{SS}	AN39	V_{SS}	AW39
V_{SS}	AR1		
V_{SS}	AR4		

Package and Pinout (Continued)

Power Consumption

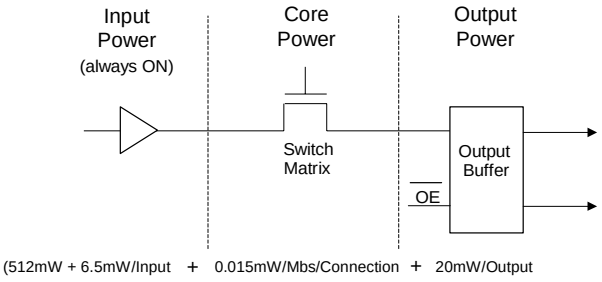
Chip power consists of three integral elements (refer to Table 18):

1. Input Power—This element has two components:

   a steady state component that is always ON, and

   a component that is based on the number of inputs being used.
2. Core Power—Core power is a function of data rate (Mb/s) and the number of connection paths through the switch matrix.
3. Output Power—This element is a fixed amount for each differential output. The value is zero if the Output Enable ($\overline{OE}$) is disabled or set to OFF.

The following diagram shows the chip power elements (as described above), the formulas used for determining chip power, and the total power consumption as determined by the formula.

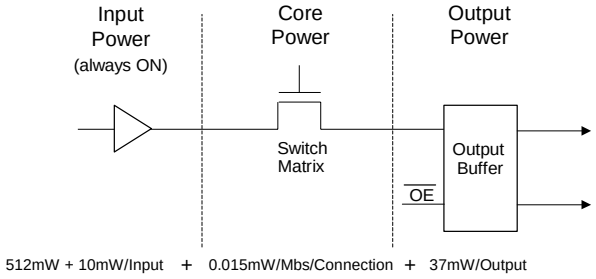


Example: Worst Case = (512mW + 832mW) + (0.015mW x 667 x 128) + (20mW x 128)

1344mW + 1280mW + 2560mW

= 5.18 watts

FIGURE 18. Power Consumption Diagram for the OCX256L using LVDS



Example: Worst Case = (512mW + 1280mW) + (0.015mW x 667 x 128) + (37mW x 128)

1792mW + 1280mW + 4736mW

= 7.81 watts

FIGURE 19. Power Consumption Diagram for the OCX256P using LVPECL

Package and Pinout (Continued)

Glossary

Clock: A single differential input used to gate data into registers in the Output Buffer. The input serves all outputs of the OCX. The neighbor input can also be used as a register clock.

Crosspoint: A single cell controlled by two RAM bits. The RAM bits are connected in a master-slave configuration to provide an update for programming and changing program information all at once.

Crosspoint Array: An array of Crosspoint cells used to connect any input port to any output port.

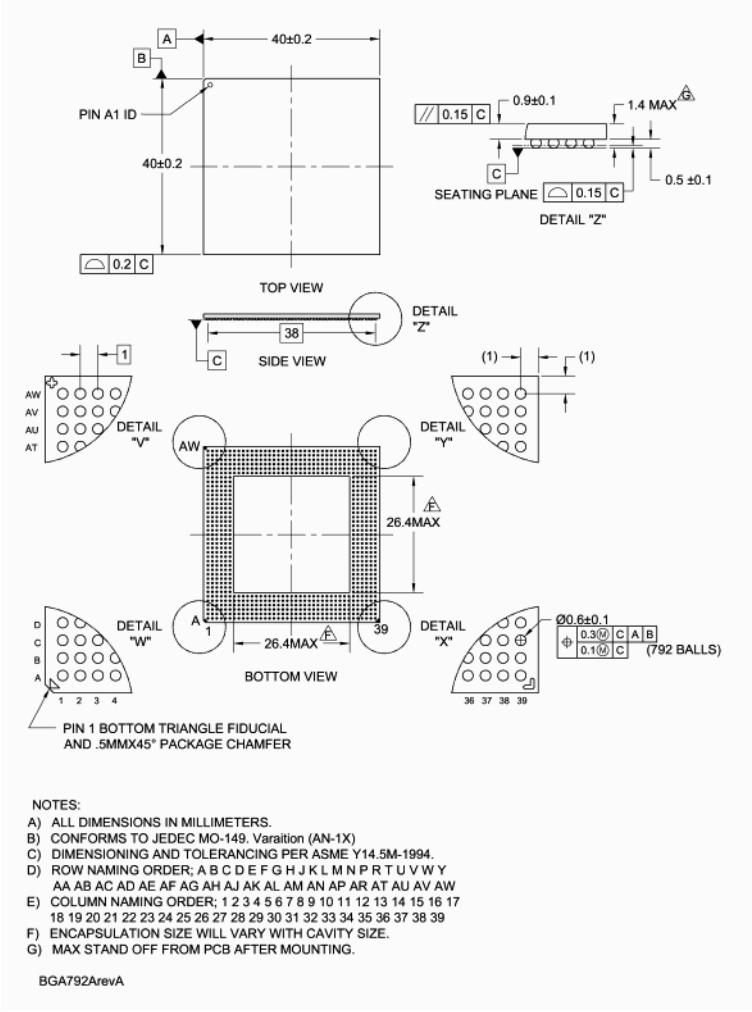
Input or Output Path: The signal flow from pin to array and array to pin. Each path has a register with selectable clocks, drivers for the loaded outputs with selectable enables, and sense circuits to detect changes on either side of the IO Buffer.

Next Neighbor: A physically adjacent port can be used as a clock source for an output configured in registered mode. These outputs are grouped in pairs such that the signal being switched through Output 0 can be used to clock the signal being switched through Output 1, or vice-versa. Any single clock or data input signal can be used to clock any other input signal provided they are switched to an appropriate output pair.

Port: A name followed by a number to identify a pin on the device.

RapidConfigure: A parallel programming method for the OCX devices. The RC mode uses 25 dedicated pins to program the Crosspoint Array and the I/O Buffers. The 25 pins consist of an enable, a clock, four instruction bits, two seven-bit address fields, and a five-bit data field.

Physical Dimensions inches (millimeters) unless otherwise noted



NOTES:
A) ALL DIMENSIONS IN MILLIMETERS.
B) CONFORMS TO JEDEC MO-149. Varaition (AN-1X)
C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
D) ROW NAMING ORDER; A B C D E F G H J K L M N P R T U V W Y
AA AB AC AD AE AF AG AH AJ AK AL AM AN AP AR AT AU AV AW
E) COLUMN NAMING ORDER; 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17
18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39
F) ENCAPSULATION SIZE WILL VARY WITH CAVITY SIZE.
G) MAX STAND OFF FROM PCB AFTER MOUNTING.

BGA792ArevA

792-Ball Thermally-Enhanced Ball Grid Array (TBGA), JEDEC MO-149, 1.0mm pitch, 40mm Square
Package Number BGA792A

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