NanoAmp Solutions, Inc.
1982 Zanker Road, San Jose, CA 95112
ph: 408-573-8878, FAX: 408-573-8877
www.nanoamp.com

N16T1625(18/30)C2A

Advance Information

16Mb Ultra-Low Power Asynchronous CMOS PSRAM

1M x 16 bit

Overview

The N16T1625(18/30)C2A is an integrated memory device containing a 16 Mbit Pseudo Static Random Access Memory using a self-refresh DRAM array organized as 1,048,576 words by 16 bits. It is designed to be identical in operation and interface to standard 6T SRAMS. The device is designed for low standby and operating current and includes a power-down feature to automatically enter standby mode. Also included are several other power saving modes: a deep sleep mode where data is not retained in the array and partial array refresh mode where data is retained in a portion of the array. Both these modes reduce standby current drain. The VFBGA package has an option for a separate Vcc and VccQ power structure for the I/O to be run from a separate power supply from the device core.

Features

- **Dual voltage for Optimum Performance:**
  Vccq - 1.7V to Vcc
  Vcc - 1.7 to 2.2 Volts
  Vcc - 2.3 to 2.7 Volts
  Vcc - 2.7 to 3.3 Volts
- **Fast Cycle Times**
  T_{ACC} < 60 nS for 3V device
  T_{ACC} < 70 nS for 2.5V device
  T_{ACC} < 85 nS for 1.8V device
- **Very low standby current**
  I_{SB} < 40µA for 1.8V device
  I_{SB} < 60µA for 2.5V device
- **Very low operating current**
  Icc < 20mA
- **48-Pin VFBGA, Wafers Available**
- **Dual rail operation**
  V_{CCQ} and V_{SSQ} for separate I/O power rail

Product Family

Part Number	Package Type	Operating Temperature	Power Supply	Speed	Standby Current (I_{SB}), Max	Operating Current (Icc), Max
N16T1618C2AB N16T1625C2AB N16T1630C2AB	48 - BGA	-25°C to +85°C	1.7V - 2.2V(V_{CC}) 2.3V - 2.7V(V_{CC}) 2.7V - 3.3V(V_{CC})	85ns @ 1.70V 70ns @ 2.30V 60ns @ 2.70V	40 µA 60 µA 80 µA	3 mA @ 1MHz

Pin Configuration

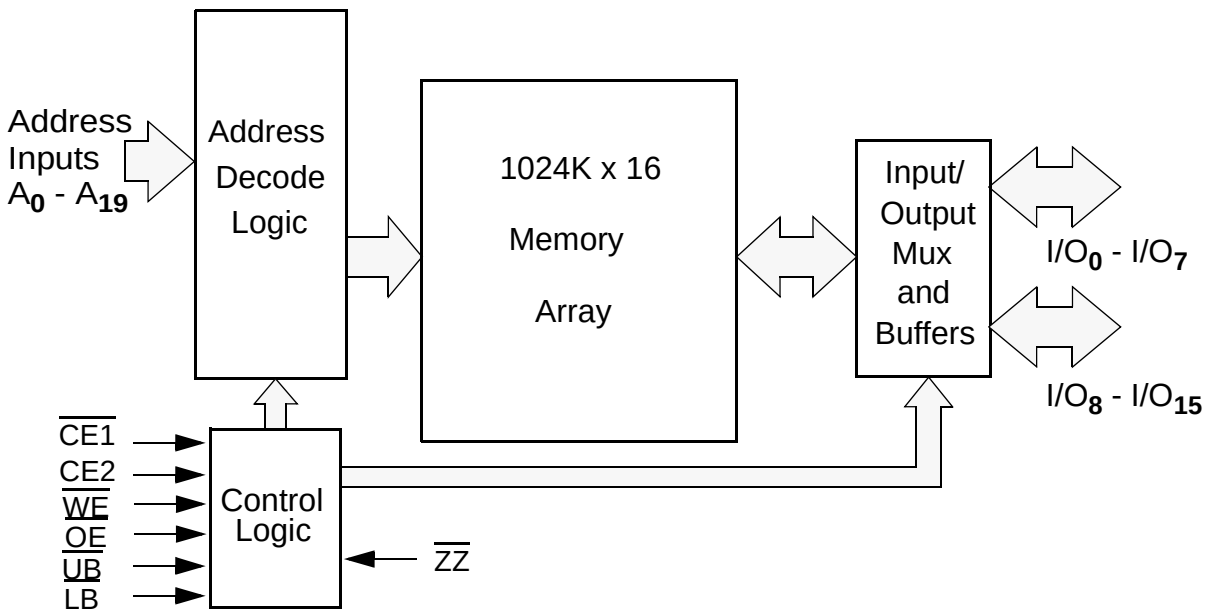
	1	2	3	4	5	6
A	$\overline{LB}$	$\overline{OE}$	A_0	A_1	A_2	CE2/$\overline{ZZ}$
B	I/O_8	$\overline{UB}$	A_3	A_4	$\overline{CE1}$	I/O_0
C	I/O_9	I/O_{10}	A_5	A_6	I/O_1	I/O_2
D	V_{SSQ}	I/O_{11}	A_{17}	A_7	I/O_3	V_{CC}
E	V_{CCQ}	I/O_{12}	DNU	A_{16}	I/O_4	V_{SS}
F	I/O_{14}	I/O_{13}	A_{14}	A_{15}	I/O_5	I/O_6
G	I/O_{15}	A_{19}	A_{12}	A_{13}	$\overline{WE}$	I/O_7
H	A_{18}	A_8	A_9	A_{10}	A_{11}	NC

48 Pin BGA (top)
6 x 8 mm

Pin Descriptions

Pin Name	Pin Function
A_0-A_{19}	Address Inputs
$\overline{WE}$	Write Enable Input
$\overline{CE1}$, CE2	Chip Enable Input
$\overline{ZZ}$	Deep Sleep Input
$\overline{OE}$	Output Enable Input
$\overline{LB}$	Lower Byte Enable Input
$\overline{UB}$	Upper Byte Enable Input
I/O_0-I/O_{15}	Data Inputs/Outputs
V_{CC}	Power
V_{SS}	Ground
V_{CCQ}	Power I/O pin only
V_{SSQ}	Ground I/O pin only
DNU	Do Not Use (or connect to V_{SS})

Functional Block Diagram



Functional Description

CE1	CE2 [1]	WE	OE	UB/LB	ZZ [2]	I/O[3]	MODE	POWER
H	X	X	X	X	H	High Z	Standby[4]	Standby
X	L	X	X	X	H	High Z	Standby[4]	Standby
X	X	X	X	H	H	High Z	Standby[4]	Standby
L	H	L	X[5]	L[3]	H	Data In	Write[5]	Active -> Standby[6]
L	H	H	L	L[3]	H	Data Out	Read	Active -> Standby[6]
L	H	H	H	L[3]	H	High Z	Active	Standby[6]

1.) Only on the two-CE option device.

2. Only on the one-CE option device with sleep mode.

3. When $\overline{UB}$ and $\overline{LB}$ are in select mode (low), I/O_0 - I/O_{15} are affected as shown. When $\overline{LB}$ only is in the select mode only I/O_0 - IO_7 are affected as shown. When $\overline{UB}$ is in the select mode only I/O_8 - I/O_{15} are affected as shown. If both $\overline{UB}$ and $\overline{LB}$ are in the deselect mode (high), the chip is in a standby mode regardless of the state of $\overline{CE1}$ or CE2.

4. When the device is in standby mode, control inputs ($\overline{WE}$, $\overline{OE}$, $\overline{UB}$, and $\overline{LB}$), address inputs and data input/outputs are internally isolated from any external influence and disabled from exerting any influence externally.

5. When $\overline{WE}$ is invoked, the $\overline{OE}$ input is internally disabled and has no effect on the circuit.

6. The device will consume active power in this mode whenever addresses are changed. Data inputs are internally isolated from any external influence.

Capacitance[1]

Item	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN} = 0V, f = 1 MHz, T_A = 25°C		8	pF
I/O Capacitance	$C_{I/O}$	V_{IN} = 0V, f = 1 MHz, T_A = 25°C		8	pF

1. These parameters are verified in device characterization and are not 100% tested

Absolute Maximum Ratings[1]

Item	Symbol	Rating	Unit
Voltage on any pin relative to V_{SS}	$V_{IN,OUT}$	–0.3 to V_{CC}+0.3	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	–0.3 to 4.0	V
Power Dissipation	P_D	500	mW
Storage Temperature	T_{STG}	–40 to 125	^oC
Operating Temperature	T_A	-25 to +85	^oC
Soldering Temperature and Time	T_{SOLDER}	240^{o}C, 10sec(Lead only)	^oC

1. Stresses greater than those listed above may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Operating Characteristics (Over Specified Temperature Range)

Item	Symbol	Comments	Min.	Typ[1]	Max.	Unit
Supply Voltage	V_{CC}	N16T1618	1.7	1.8	2.25	V
		N16T1625	2.3	2.5	2.7	
		N16T1630	2.7	3.0	3.3	
Supply Voltage for I/O	V_{CCQ}		1.7	-	Vcc	V
Input High Voltage	V_{IH}		1.4		V_{CC}+0.3	V
Input Low Voltage	V_{IL}		–0.3		0.4	V
Output High Voltage	V_{OH}	I_{OH} = 0.2mA	0.8V_{CCQ}			V
Output Low Voltage	V_{OL}	I_{OL} = -0.2mA			0.2	V
Input Leakage Current	I_{LI}	V_{IN} = 0 to V_{CC}			0.5	µA
Output Leakage Current	I_{LO}	$\overline{OE}$ = V_{IH} or Chip Disabled			0.5	µA
Read/Write Operating Supply Current @ 1 µs Cycle Time[2]	I_{CC1}	V_{CC}=V_{CC}MAX, V_{IN}=V_{IH} / V_{IL} Chip Enabled, I_{OUT} = 0			3	mA
Read/Write Operating Supply Current @ 70 ns Cycle Time[2]	I_{CC2}	V_{CC}=V_{CC}MAX, V_{IN}=V_{IH} / V_{IL} Chip Enabled, I_{OUT} = 0			20	mA
Read/Write Quiescent Operating Supply Current[3]	I_{CC3}	V_{CC}=V_{CC}MAX, V_{IN}=V_{IH} / V_{IL} Chip Enabled, I_{OUT} = 0, f = 0			200	µA
Standby Current[3]	I_{SB1}	V_{IN} = V_{CC} or 0V Chip Disabled t_A= 30^{o}C			tbd	µA
	I_{SB2}	t_A= 85^{o}C, V_{CC} = 2.2V			40	µA
		t_A= 85^{o}C, V_{CC} = 2.7V			60	µA
		t_A= 85^{o}C, V_{CC} = 3.3V			80	µA

1. Typical values are measured at Vcc=Vcc Typ., T_A=25°C and not 100% tested.

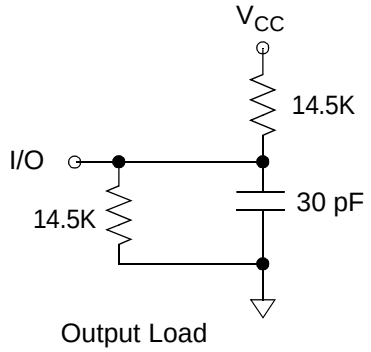
2. This parameter is specified with the outputs disabled to avoid external loading effects. The user must add current required to drive output capacitance expected in the actual system.

3. This device assumes a standby mode if the chip is disabled ($\overline{CE1}$ high or CE2 low). In order to achieve low standby current all inputs must be within 0.2 volts of either VCC or VSS.

Timing Test Conditions

Item	
Input Pulse Level	$0.1V_{CC}$ to 0.9 V_{CC}
Input Rise and Fall Time	5ns
Input and Output Timing Reference Levels	0.5 V_{CC}
Operating Temperature	-25 ^{o}C to +85 ^{o}C

Output Load Circuit

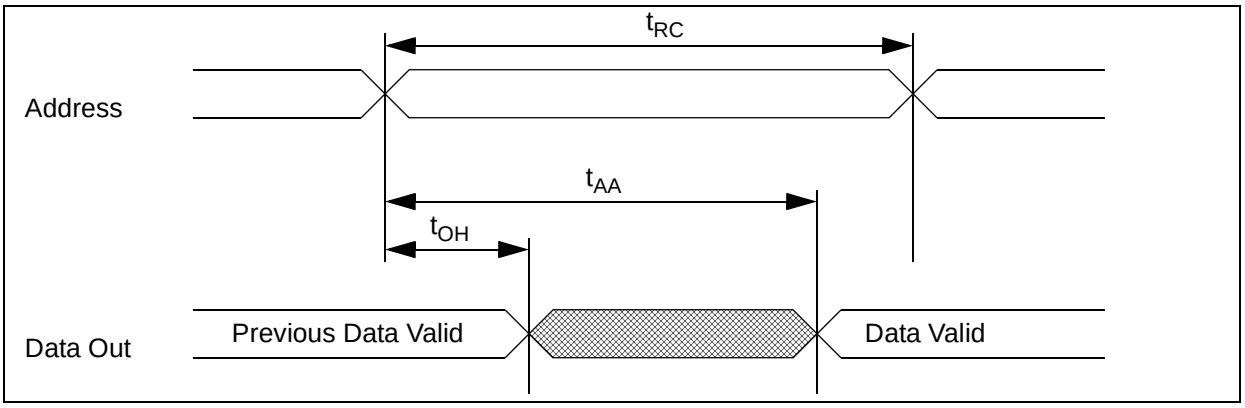


Output Load

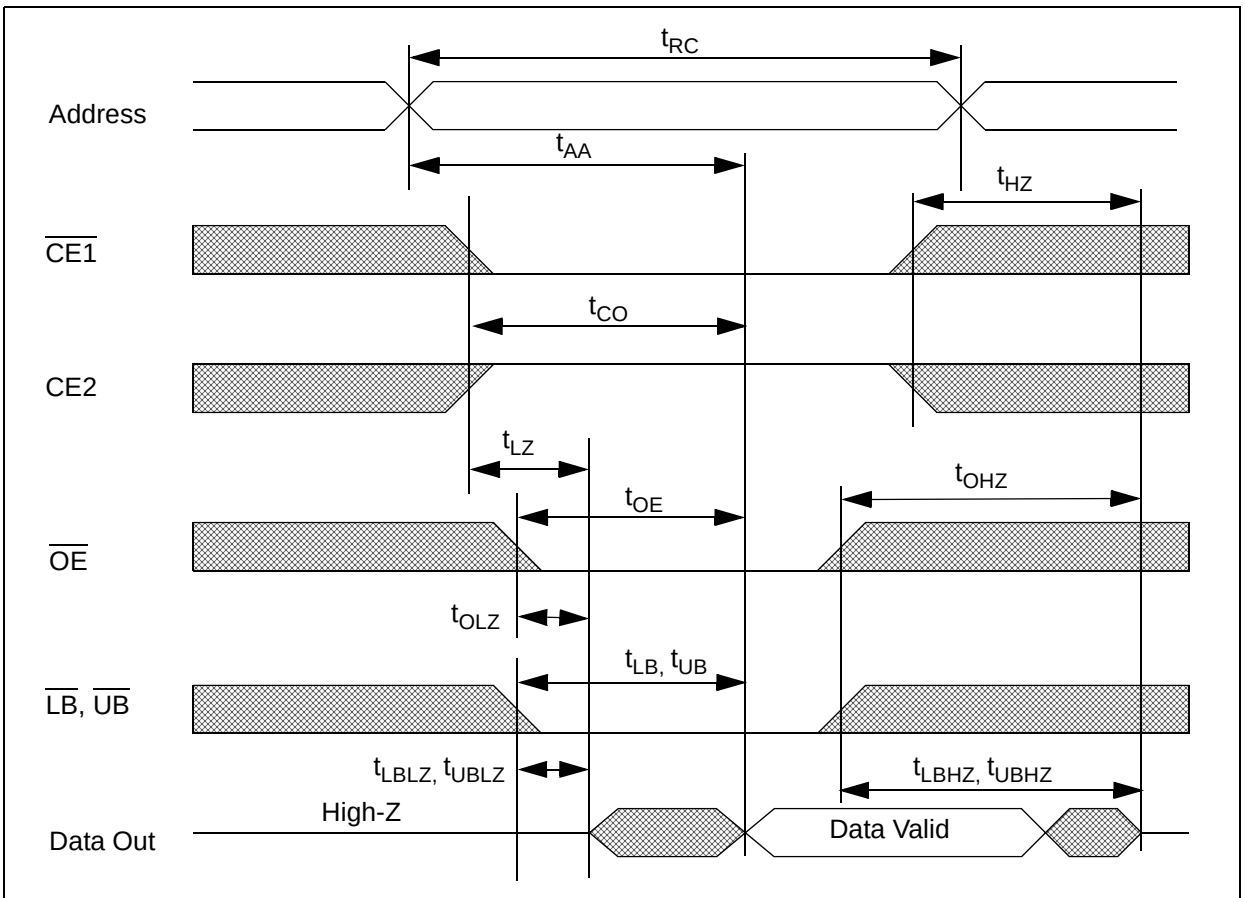
Timings

Item	Symbol	1.8V		2.5V		3.0V		Units
		Min.	Max.	Min.	Max.	Min	Max.	
Read Cycle Time	t_{RC}	85		70		60		ns
Address Access Time	t_{AA}		85		70		60	ns
Chip Enable to Valid Output	t_{CO}		85		70		60	ns
Output Enable to Valid Output	t_{OE}		15		15		15	ns
Byte Select to Valid Output	t_{LB}, t_{UB}		85		70		60	ns
Chip Enable to Low-Z output	t_{LZ}	10		10		10		ns
Output Enable to Low-Z Output	t_{OLZ}	5		5		5		ns
Byte Select to Low-Z Output	t_{LBZ}, t_{UBZ}	10		10		10		ns
Chip Disable to High-Z Output	t_{HZ}	0	20	0	20		20	ns
Output Disable to High-Z Output	t_{OHZ}	0	20	0	20		20	ns
Byte Select Disable to High-Z Output	t_{LBHZ}, t_{UBHZ}	0	20	0	20		20	ns
Output Hold from Address Change	t_{OH}	5		5		5		ns
Write Cycle Time	t_{WC}	85		70		60		ns
Chip Enable to End of Write	t_{CW}	85		70		60		ns
Address Valid to End of Write	t_{AW}	85		70		60		ns
Byte Select to End of Write	t_{LBW}, t_{UBW}	85		70		60		ns
Write Pulse Width	t_{WP}	65	30000	55	30000	45	30000	ns
Write Recovery Time	t_{WR}	0		0		0		ns
Write to High-Z Output	t_{WHZ}		20		20		20	ns
Address Setup Time	t_{AS}	0		0		0		ns
Data to Write Time Overlap	t_{DW}	25		25		25		ns
Data Hold from Write Time	t_{DH}	0		0		0		ns
End Write to Low-Z Output	t_{OW}	5		5		5		ns

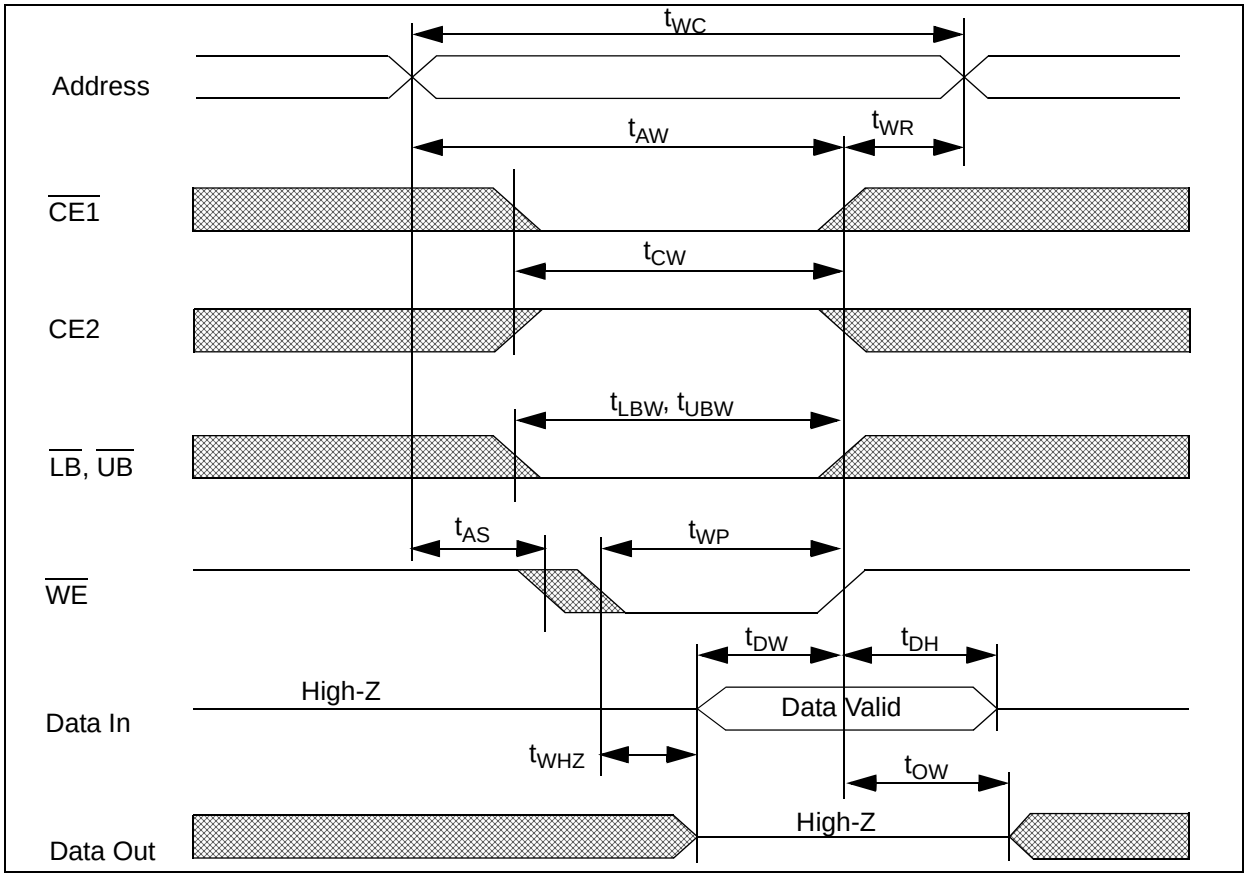
Timing of Read Cycle ($\overline{CE1}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = CE2 = V_{IH})



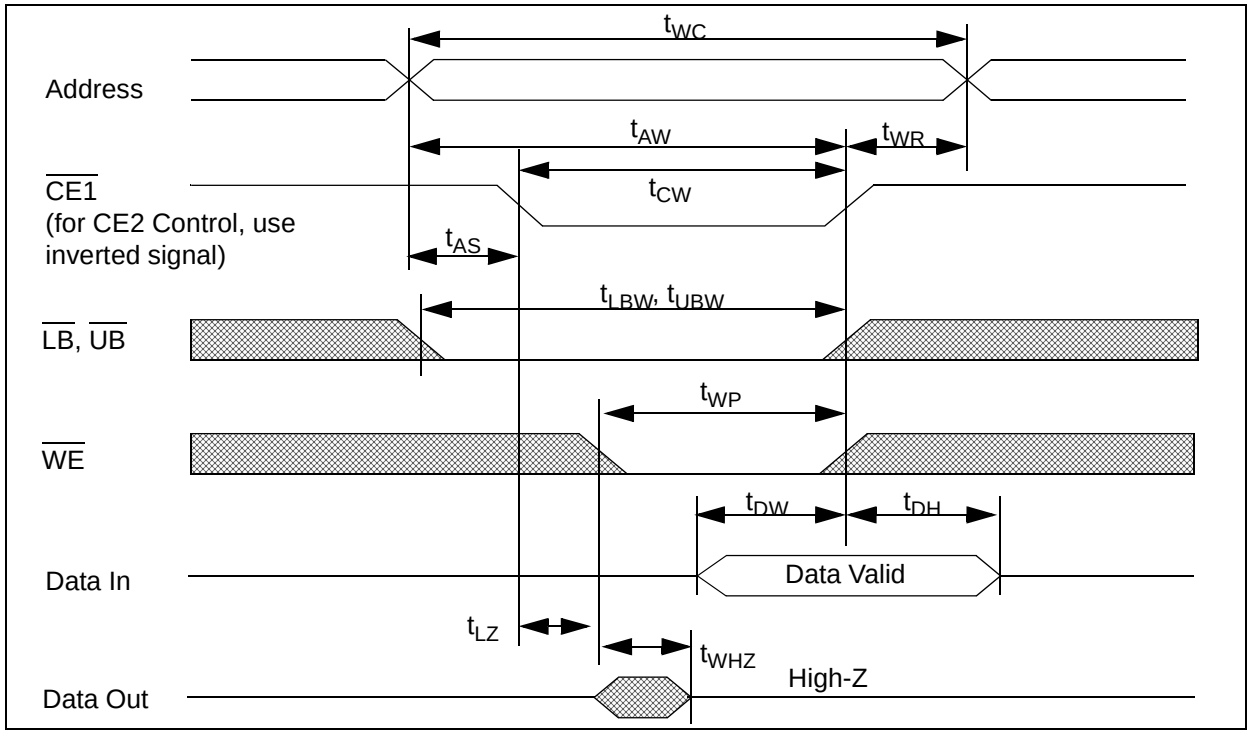
Timing Waveform of Read Cycle ($\overline{WE}$=V_{IH})



Timing Waveform of Write Cycle ($\overline{WE}$ control)



Timing Waveform of Write Cycle ($\overline{CE1}$ Control)



Power Savings Modes

The N16T1625(18/30)C2A has several power savings modes and different device versions incorporate these modes. The three modes are:
Reduced Memory Size
Partial Array Refresh
Deep Sleep Mode

All three modes are available only on the single CE device, which has a $\overline{ZZ}$ (Deep Sleep Mode) input pin.

The operation of the power saving modes is controlled by setting the Variable Address Register (VAR). This VAR is shown in Figure 1 and is used to enable/disable the various low power modes.
The VAR is set by using the timings defined in figure 2. The register must be set in less then 1us after $\overline{ZZ}$ is enabled low.

1) Reduced Memory Size (RMS)

In this mode of operation, the 16Mb PSRAM can be operated as a 4Mb, 8Mb or a 12Mb device. The mode and array size are determined by the settings in the VA register. The VA register is set according to the timings of Figure 2 and the bit setting of Table 3. The RMS mode is enabled at the time of ZZ transitioning high and the mode remains active until the register is updated. To return to the full 16Mb address space, the VA register must be reset using the previously defined procedures.

2) Partial Array Refresh (PAR)

In this mode of operation, the internal refresh operation can be restricted to a 4Mb, 8Mb or 12Mb portion of the array. The mode and array partition to be refreshed are determined by the settings in the VAR register. The VAR register is set according to the timings of Figure 2 and the bit settings of Table 2. In this mode, when $\overline{ZZ}$ is taken low, only the portion of the array that is set in the register is refreshed. The operating mode is only available during standby time and once $\overline{ZZ}$ is returned high, the device resumes full array refresh. All future PAR cycles will use the contents of the VA register To change the address space of the PAR mode, the VA register must be reset using the previously defined procedures.

There are two different device versions that have different default settings for the PAR mode.

In the first version, the default state for the $\overline{ZZ}$ enable/disable register will be $\overline{ZZ}$ enabled where $\overline{ZZ}$ low will initiate a deep sleep mode after 1us. This device is referred to as Deep Sleep Active, or DSA device. In the second version, the default state for the $\overline{ZZ}$ register will be such that $\overline{ZZ}$ low will put the device into PAR mode after 1us and never initiate a deep sleep mode unless appropriate register is updated. This device is referred to as Deep Sleep Inactive, or DSI device. In either device, once the SRAM enters Deep Sleep Mode, the VAR contents are destroyed and the default register settings are reset.

3) Deep Sleep Mode

In this mode of operation, the internal refresh is turned off and all data integrity of the array is lost. Deep Sleep is entered by bringing $\overline{ZZ}$ low. After 1 us, if the VAR register corresponding to A4 is not set to Deep Sleep Disabled, the device will enter Deep Sleep Mode. The device will remain in this mode as long as $\overline{ZZ}$ remains low.

FIGURE 1: Variable Address Register

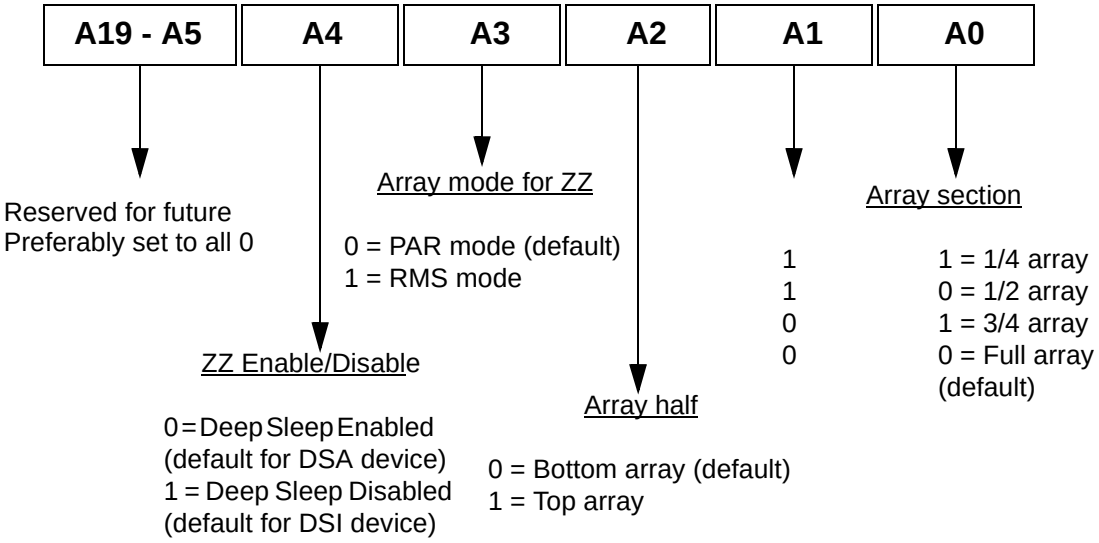
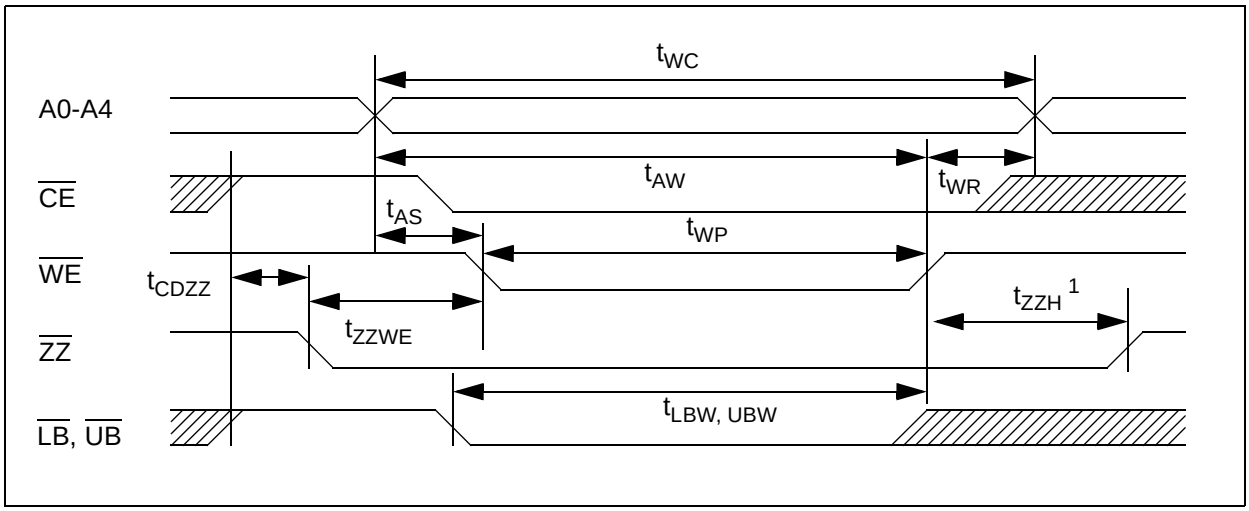


FIGURE 2: Variable Address Register (VAR) Update Timings



1) Applies only for setting the register for RMS mode.

FIGURE 3: Deep Sleep Mode - Entry/Exit Timings

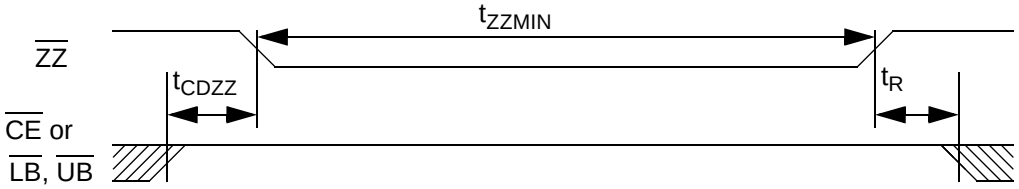


Table 1: VAR Update and Deep Sleep Timings

Item	Symbol	Min	Max	Unit
PAR and RMS $\overline{ZZ}$ low to $\overline{WE}$ low	t_{zzwe}		1000	ns
Chip ($\overline{CE}$, $\overline{UB}$/$\overline{LB}$) deselect to ZZ low	t_{cdzz}	0		ns
$\overline{ZZ}$ low after $\overline{WE}$ high	t_{zzh} [1]	20		ns
Deep Sleep Mode	t_{zzmin}	10		us
Deep Sleep Recovery	t_r	200		us

1) Applies only for setting the register for RMS mode.

TABLE 2: Address Patterns for PAR (A3 = 0, A4 = 1)

A2	A1	A0	Active Section	Address space	Size	Density
0	1	1	One-quarter of die	00000h - 3FFFFh	256Kb x 16	4Mb
0	1	0	One-half of die	00000h - 7FFFFh	512Kb x 16	8Mb
0	0	1	Three-quarters of die	00000h - BFFFFh	768Kb x 16	12Mb
1	1	1	One-quarter of die	C0000h - FFFFh	256Kb x 16	4Mb
1	1	0	One-half of die	80000h - FFFFFh	512Kb x 16	8Mb
1	0	1	Three-quarters of die	40000h - FFFFFh	768Kb x 16	12Mb

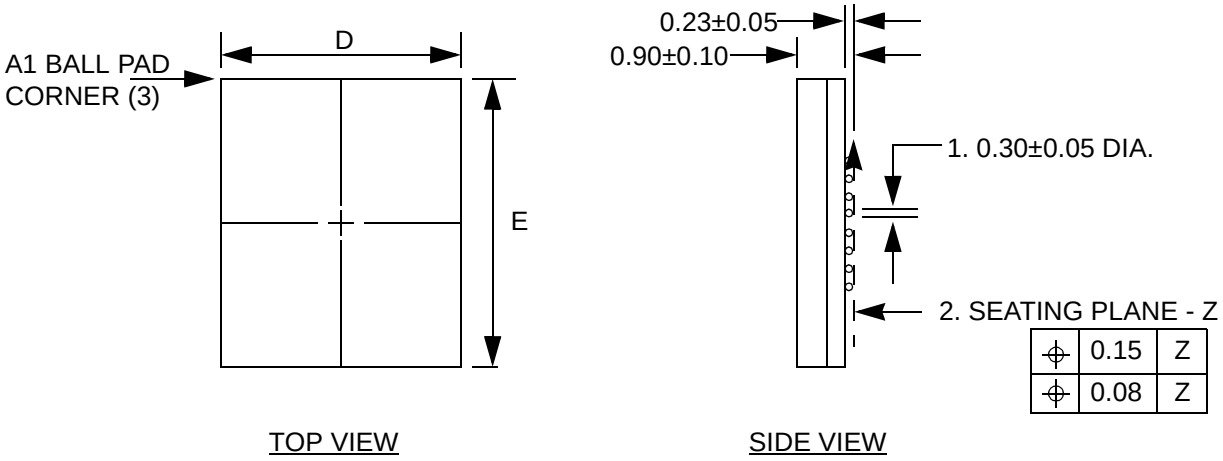
TABLE 3: Address patterns for RMS (A3 = 1, A4 = 1)

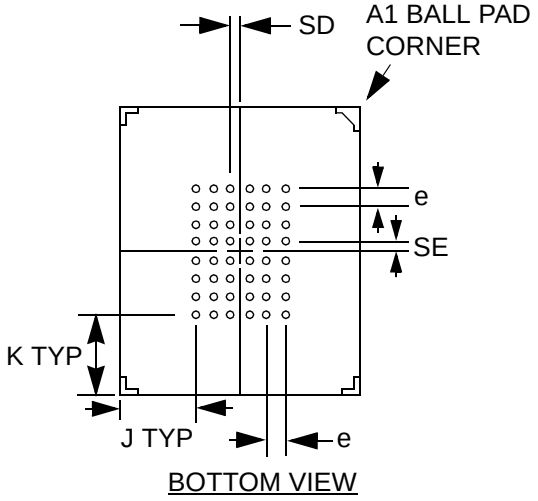
A2	A1	A0	Active Section	Address space	Size	Density
0	1	1	One-quarter of die	00000h - 3FFFFh	256Kb x 16	4Mb
0	1	0	One-half of die	00000h - 7FFFFh	512Kb x 16	8Mb
0	0	1	Three-quarters of die	00000h - BFFFFh	768Kb x 16	12Mb
0	0	0	Full die	00000h - FFFFFh	1Mb x 16	16Mb
1	1	1	One-quarter of die	C0000h - FFFFh	256Kb x 16	4Mb
1	1	0	One-half of die	80000h - FFFFFh	512Kb x 16	8Mb
1	0	1	Three-quarters of die	40000h - FFFFFh	768Kb x 16	12Mb
1	0	0	Full die	00000h - FFFFFh	1Mb x 16	16Mb

TABLE 4: Low Power ICC Characteristics for N16T1625(18/30)C2A

Item	Symbol	Test	Array Partition	Typ	Max	Unit
PAR Mode Standby Current	I_{PAR}	$V_{IN} = V_{CC}$ or 0V, Chip Disabled, $t_A = 85^oC$	1/4 Array		35	uA
			1/2 Array		40	
			3/4 Array		55	
RMS Mode Standby Current	I_{RMSSB}	$V_{IN} = V_{CC}$ or 0V, Chip Disabled, $t_A = 85^oC$	4Mb Device		35	uA
			8Mb Device		40	
			12Mb Device		55	
Deep Sleep Current	I_{ZZ}	$V_{IN} = V_{CC}$ or 0V, Chip in $\overline{ZZ}$ mode, $t_A = 85^oC$			10	uA

Ball Grid Array Packag





1. DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER. PARALLEL TO PRIMARY Z.

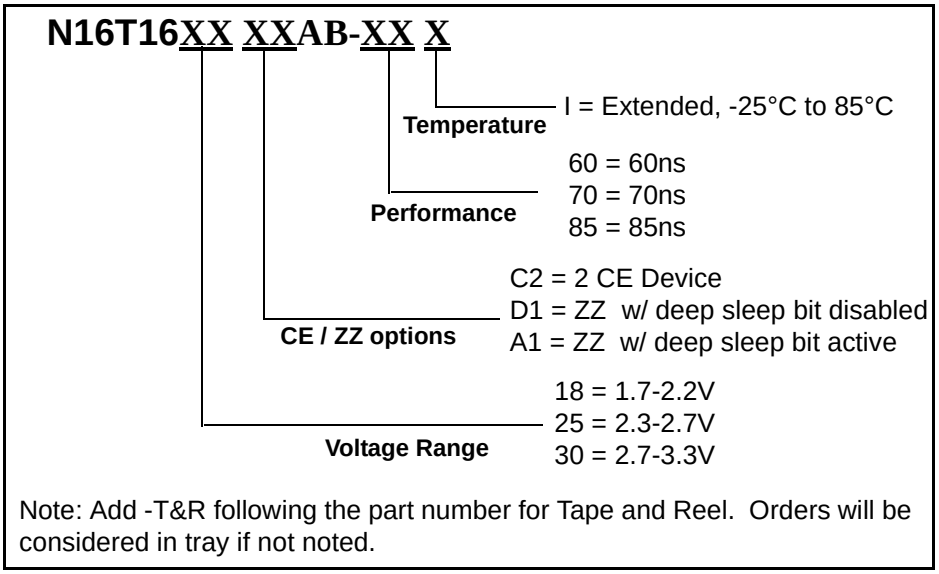
2. PRIMARY DATUM Z AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

3. A1 BALL PAD CORNER I.D. TO BE MARKED BY INK.

Dimensions (mm)

D	E	e = 0.75				BALL MATRIX TYPE
		SD	SE	J	K	
6±0.10	8±0.10	0.375	0.375	1.125	1.375	FULL

Ordering Information



Note: Add -T&R following the part number for Tape and Reel. Orders will be considered in tray if not noted.

Revision History

Revision	Date	Change Description
A	6/20/02	Released under document control (Stock No. 23159)