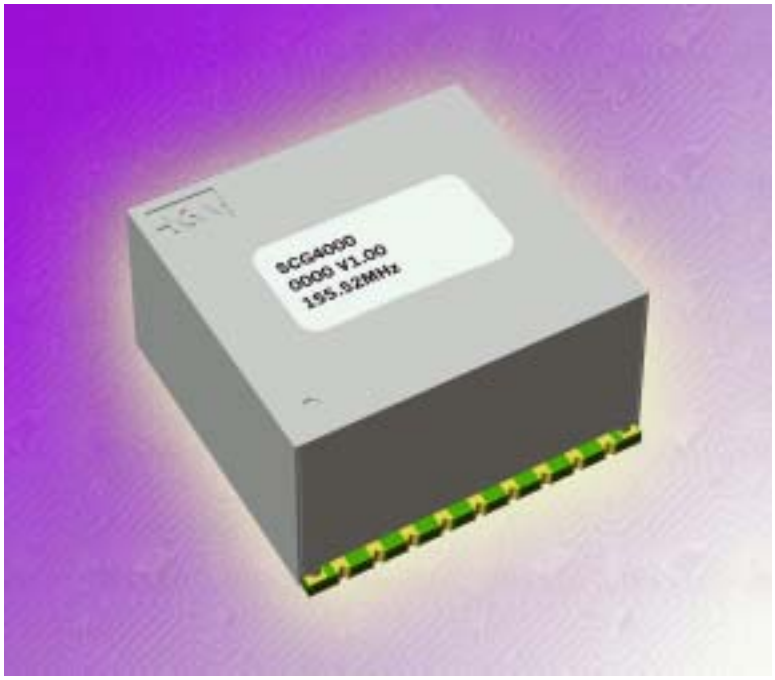
SCG4000 Series Synchronous Clock Generators

PLL

2111 Comprehensive Drive
Aurora, Illinois 60505
Phone: 630-851-4722
Fax: 630-851-5040
www.conwin.com



Application

The Connor-Winfield SCG4000 Series provides high precision phase lock loop frequency translation for the telecommunication applications.

SCG4000 Series is well suited for use in line cards, service termination cards and similar functions to provide reliable reference, phase locked, synchronization for TDM, PDH, SONET and SDH network equipment. The SCG4000 Series provides a jitter filtered, wander following output signal sychronized to a superior Stratum or peer input reference signal.

Features

- 3.3V High Precision PLL
- Tri-State Capability
- Active Alarms
- Guaranteed Free Run ±20ppm
- 1 sec. Acquisition Time

Bulletin	**SG031**
Page	**1 of 12**
Revision	**A04**
Date	**08 JAN 02**
Issued By	**MBatts**

General Description

The SCG4000 Series is a digital phase locked loop generating a LVPECL outputs from an intrinsically low jitter voltage controlled crystal oscillator. The LVPECL outputs may be disabled. The jitter attenuated internal reference, divided down from the output frequency, is also output to a pin.

The SCG4000 Series can lock to one of four possible reference frequencies from 8 to 64 kHz, which is selectable using two input select pins. A filtered reference output signal is available at the same frequency. The unit has an acquisition time of about 1 second and it is tolerant of different reference duty cycles.

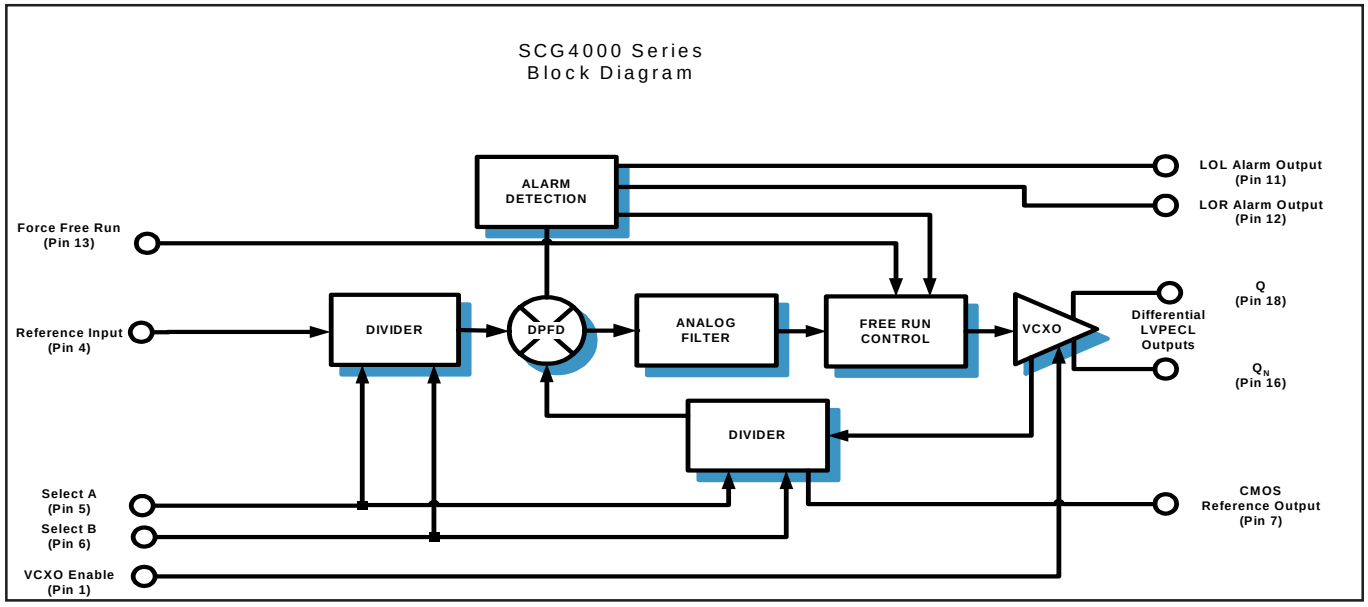
Further features include alarm outputs for Loss-of-Reference (LOR) and Loss-of-Lock (LOL). During the LOR alarm, the SCG4000 will also enter a Free Run state, which will guarantee a 20 ppm accurate output. Additionally the Free Run mode may be entered manually.

The alarms and reference output may be put into the tri-state high impedance condition for external testing purposes.

The package dimensions are 1" x 1.025" x .407" on a 6 layer FR4 board with castellated pins. Parts are assembled using high temperature solder to withstand 63/37 alloy, 180° C surface mount reflow processes.

Functional Block Diagram

Figure 1



Model Comparison Table

Table 1

Model	Input Ref Freq	Max Duty Cycle	CMOS Reference Output (Pin #7)	LVPECL Oscillator Output (Pin #16 & 18)	Notes
SCG4000	8-64 kHz	40/60	= Input Ref Freq.	125.0 MHz, 155.52 MHz	Basic Model
SCG4010	**19.44 MHz**	40/60	**19.44 MHz**	125.0 MHz, 155.52 MHz	
SCG4030	8-64 kHz	**45/55**	= Input Ref Freq.	125.0 MHz, 155.52 MHz	Tighter Duty Cycle

*Features which differentiate a model from the base model (SCG4000) are highlighted in boldface color and in the notes column.

Absolute Maximum Rating

Table 2 — All SCG4000 Models

Symbol	Parameter	Minimum	Nominal	Maximum	Units	Notes
Vcc	Power Supply Voltage	3.0		3.6	Volts	
V1	Input Voltage	-0.5		5.5	Volts	
Ts	Storage Temperature	-65		150	deg. C	

Operating Specifications

Table 3 — All SCG4000 Models

Symbol	Parameter	Minimum	Nominal	Maximum	Units	Notes
V_{cc}	Power Supply Voltage	3.135	3.3	3.465	Volts	1.0
I_{cc}	Power Supply Current	-	230	280	mA	
T_o	Temperature Range	0	-	70	°C	
F_{fr}	Free Run Accuracy	-20	-	20	ppm	
F_{cap}	Capture/pull-in range	-25	-	25	ppm	
F_{bw}	Jitter Filter Bandwidth	-	-	10	Hz	
T_{jtol}	Input Jitter Tolerance	-	-	6.25	µs	
T_{aq}	Acquisition Time	-	1	-	s	2.0
T_{rf}	Output Rise and Fall Time (20% 80%)	100	225	350	ps	3.0

Features

Table 4 — All SCG4000 Models

Parameter	Specifications	Notes
Alarms	LOR, LOL Status on seperate CMOS Outputs	
TDEV	70 ps (typical)	
MTIE	800 ps (typical)	
VCXO Output Logic Type	LVPECL	
Reference Output Logic Type	CMOS	
Package	FR4 SM 1.0" x 1.025" x 0.45"	

CMOS Input And Output Characteristics

Table 5 — All SCG4000 Models

Symbol	Parameter	Minimum	Nominal	Maximum	Units	Notes
V_{IH}	High Level Input Voltage	2		5.5	V	
V_{IL}	Low Level Input Voltage	0		0.8	V	
T_{IO}	I/O to Output Valid			10	nS	
C_O	Output Capacitance			10	pF	
V_{HO}	High Level Output Voltage Ioh = 04mA	2.4				Vcc Min.
V_{IO}	Low Level Output Voltage Io1 = 8mA			0.4		Vcc Max.
T_{IR}	Input Reference Signal Pulse Width	12.5		nS		

NOTES: 1.0: Requires external regulation and filter (22uF, 330 pF)
` 2.0: From a 20 ppm offset in reference frequency
3.0: 50Ω load biased to 1.3V

LVPECL Output Characteristics

Table 6 — All SCG4000 Models

Symbol	Parameter	Minimum	Nominal	Maximum	Units	Notes
V_{OH}	High Level PECL Voltage	2.27	2.34	2.42	V	
V_{OL}	Low Level PECL Voltage	1.49	1.51	1.68	V	
C_L	Output Capacitance			10	pF	
T_{SKEW}	Differential Output Skew		50		ps	

Output Jitter Specifications

Table 7 — All SCG4000 Models

	Jitter BW 10 Hz - 1 MHz		Sonnet Jitter BW 12 kHz - 20 MHz	
Frequency (MHz)	pS (RMS)	m UI	pS (RMS)	m UI
125.0	20(typical)	2.5 (typical)	1 (max), 0.3 (typical)	0.125(max)
155.52	20(typical)	3.1 (typical)	1 (max), 0.4 (typical)	0.156 (max)

Output Programming

Table 8 — All SCG4000 Models

Tristate	Free Run	Output
0	0	Locked to reference selected (default)
1	X	Hi-Z Tristate condition
0	1	Free run at nominal frequency

Alarm Status

Table 9 — All SCG4000 Models

LOL Output	LOR Output	Alarm Output
0	0	No alarm
1	0	Loss-of-Lock
X	1	Loss-of-Reference

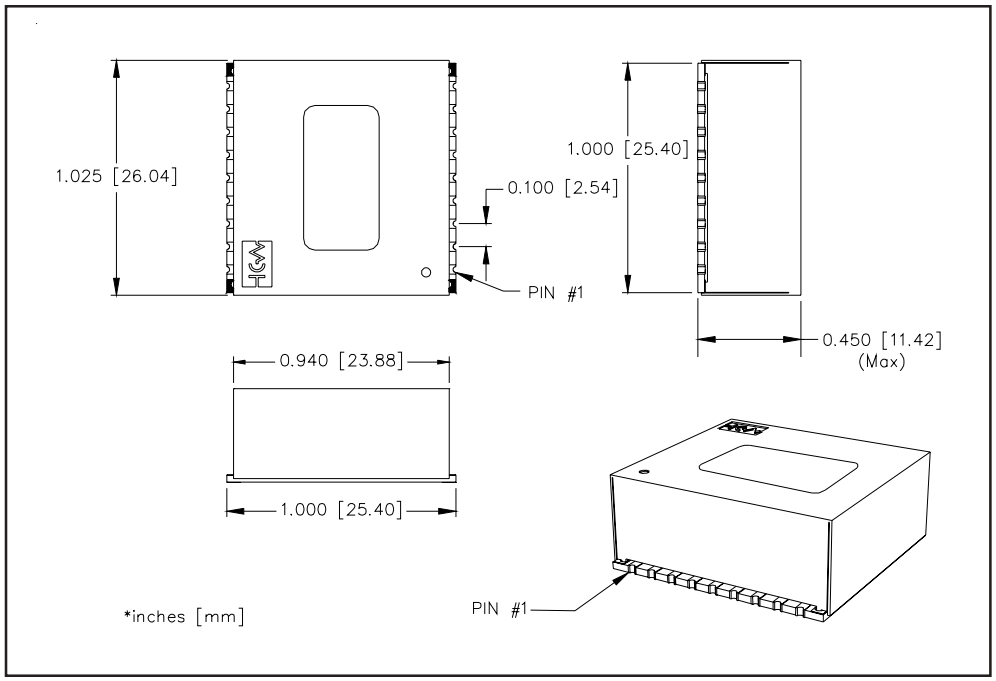
Pin Description

Table 10 — All SCG4000 Models

Pin #	Connection	Description
1	$\overline{\text{Enable}}$/Disable	Enable = 0, Disable = 1 for VCXO Ouputs, Default = 0 (for No Connect)
2	TCK	JTAG pin that is used only by Connor-Winfield for programming. Do not connect
3	TDO	JTAG pin that is used only by Connor-Winfield for programming. Do not connect
4	Reference In	CMOS Reference Frequency Input
5	Select A	Reference Frequency Select Pin, Default = 0 (for No Connect)
6	Select B	Reference Frequency Select Pin, Default = 0 (for No Connect)
7	Reference Out	Filtered Reference Output
8	Ground	Power Ground
9	Tri-State Enable	CMOS Output Tri-State enable (Hi-Z =1, Default = 0)
10	V_{CC}	3.3V Supply Voltage.
11	Loss of Lock	LOL Alarm Output
12	Loss of Reference	LOR Alarm Output
13	Free Run	Force output frequency to Free Run (FR = 1, Default = 0)
14	TDI	JTAG pin that is used only by Connor-Winfield for programming. Do not connect
15	TMS	JTAG pin that is used only by Connor-Winfield for programming. Do not connect
16	$\overline{\text{VCXO Out}}$	VCXO differential LVPECL Output
17	Signal Ground	VCXO output ground (Shield)
18	VCXO Out	VCXO differential LVPECL Output

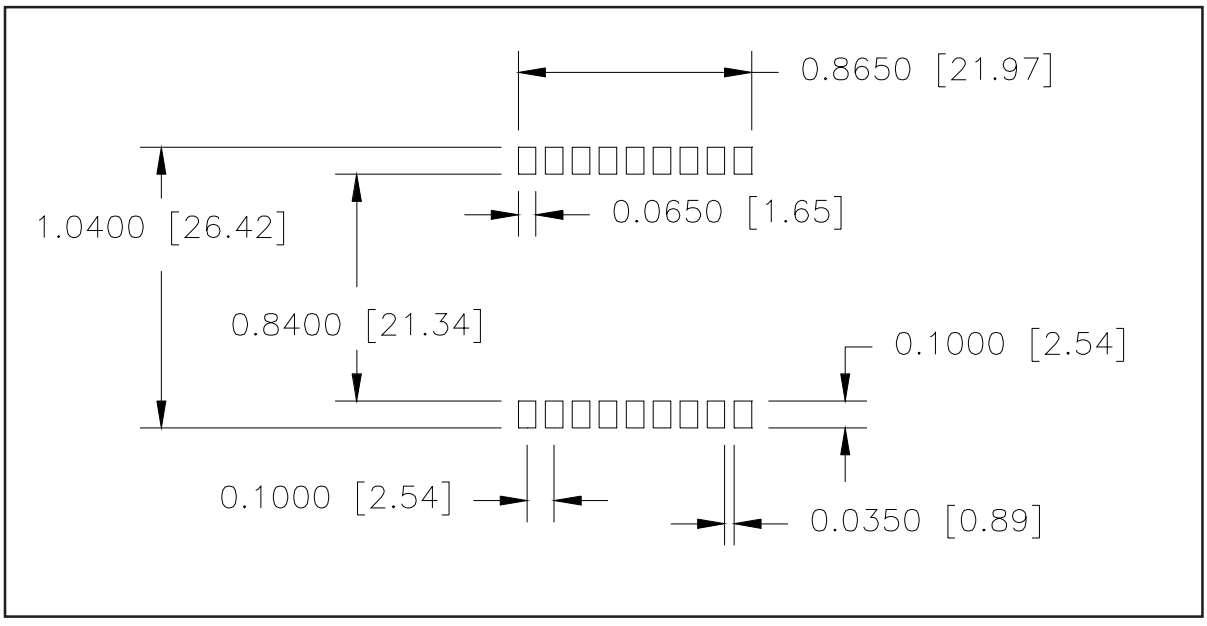
Package Dimensions

Figure 2



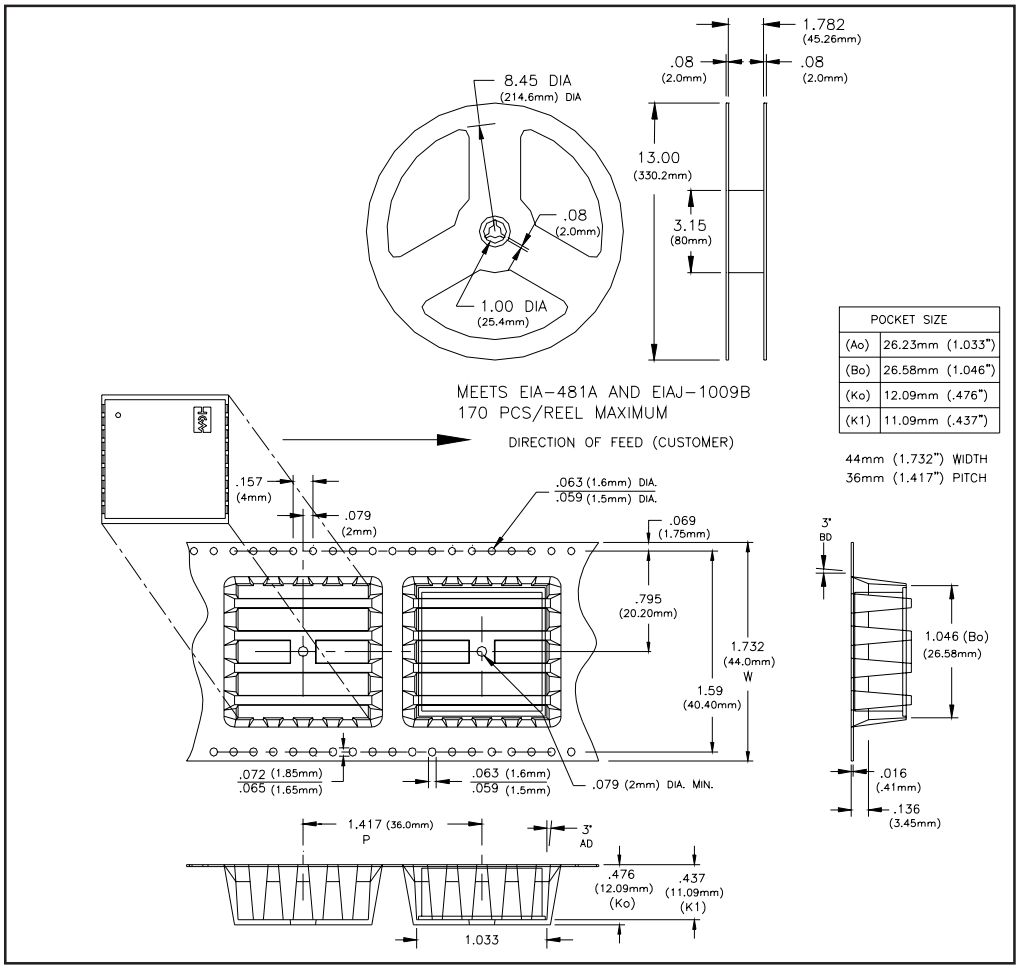
Recommended Footprint Dimensions

Figure 3



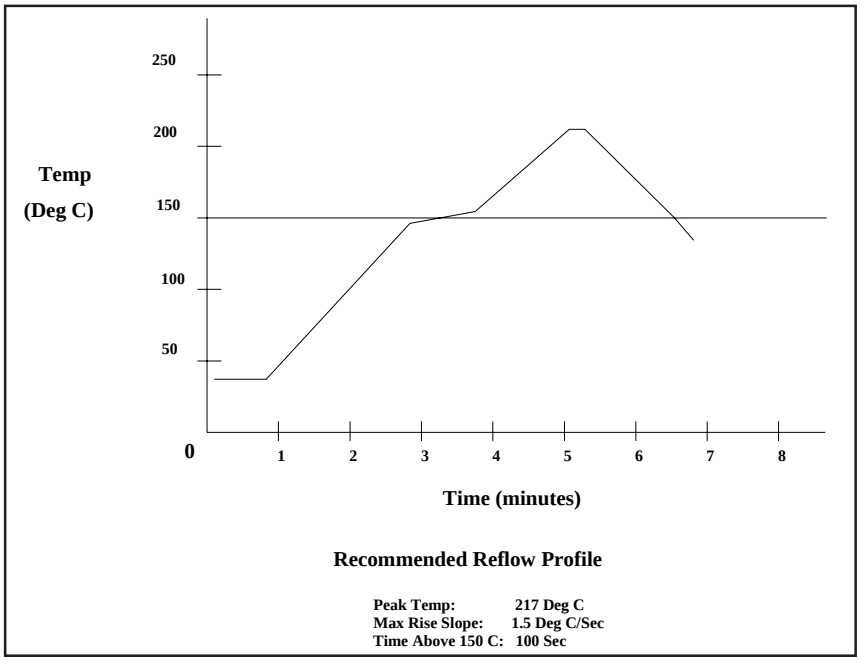
Tape and Reel Dimensions

Figure 4



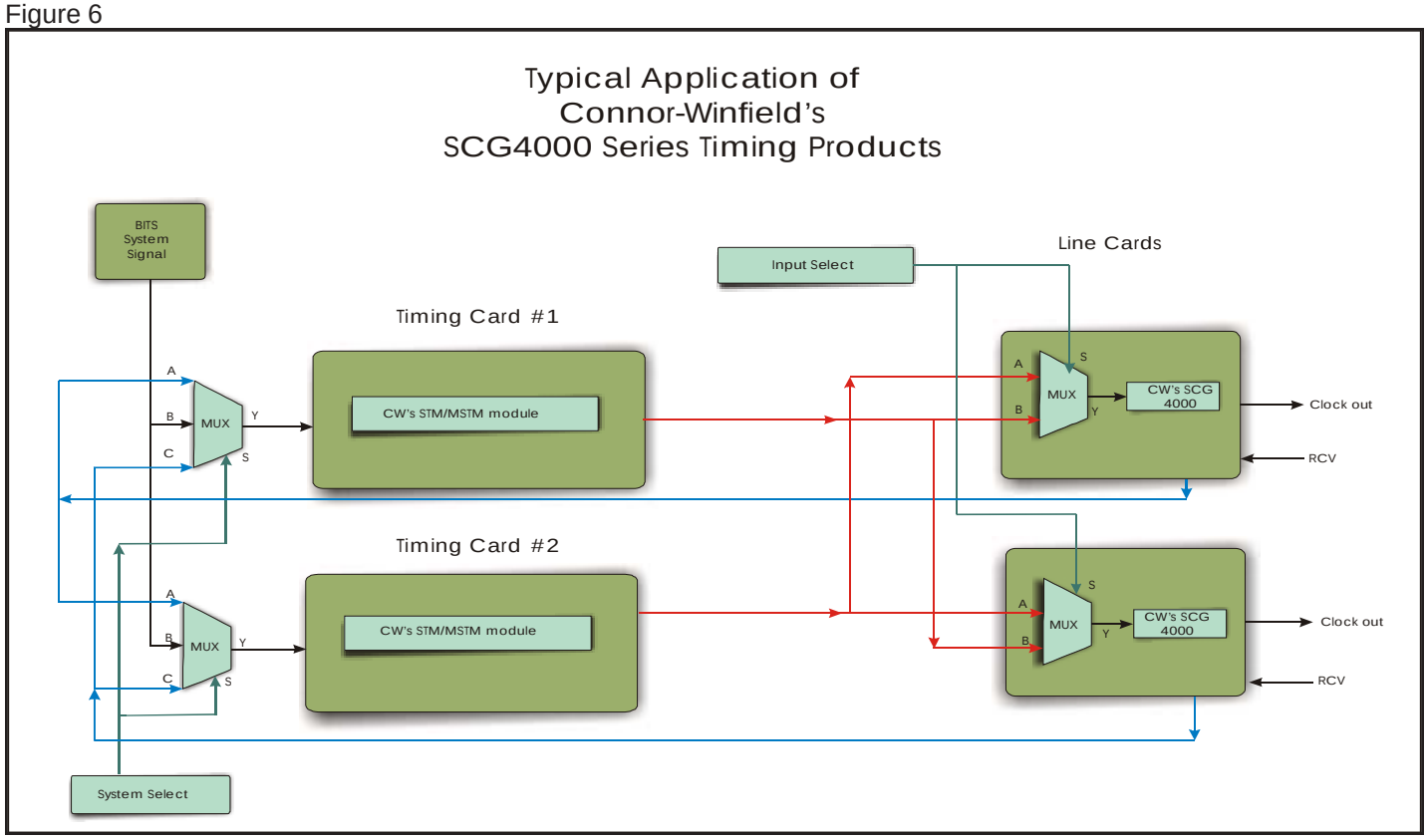
Solder Profile

Figure 5



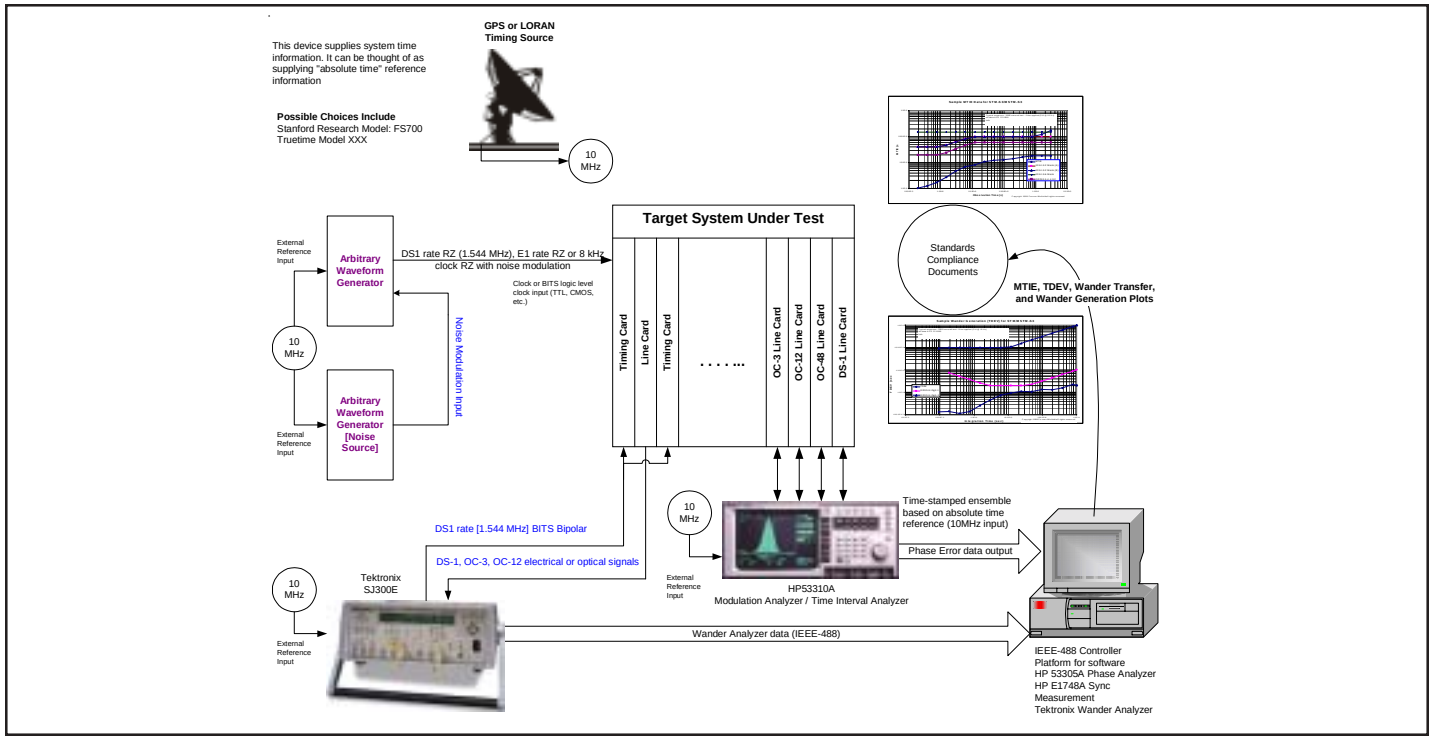
Typical Application

Figure 6



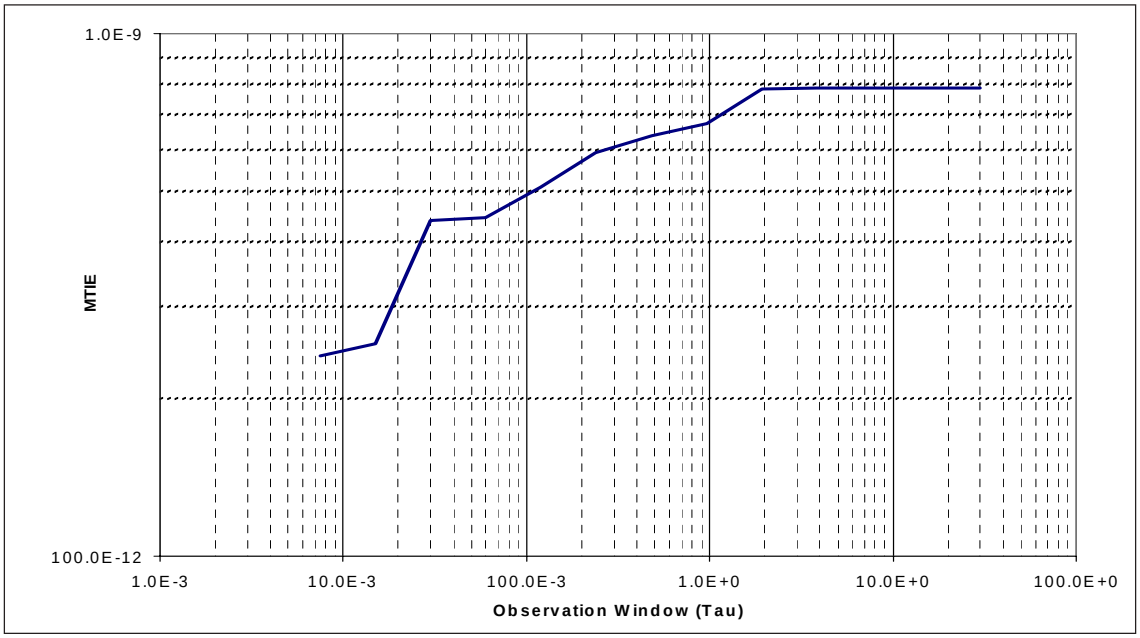
Typical System Test Set-up

Figure 7



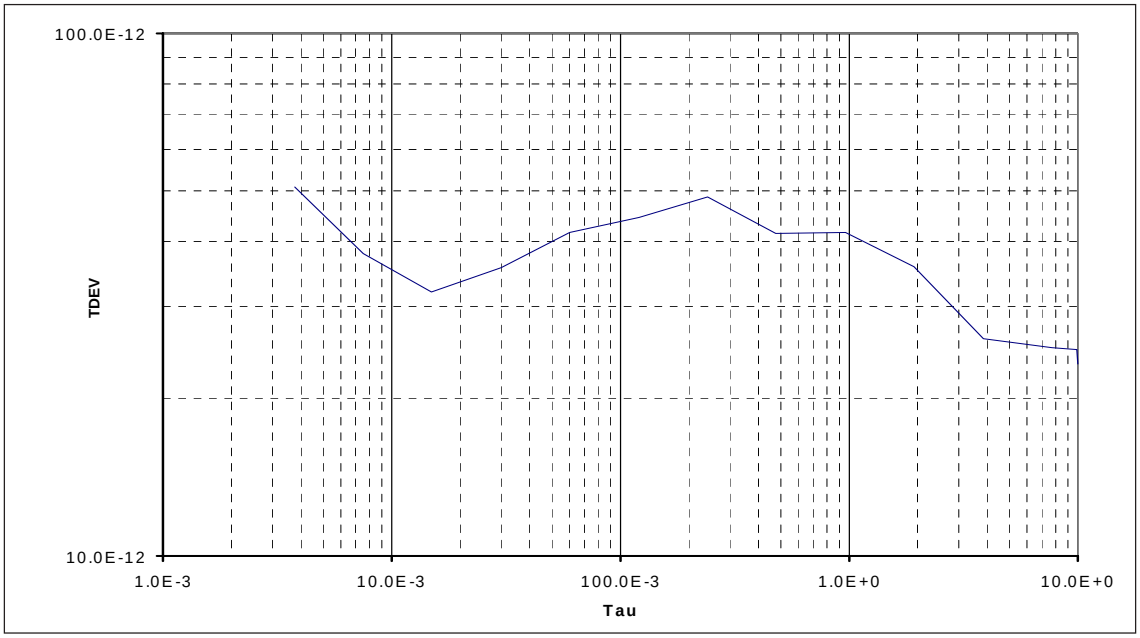
SCG4000 Series Typical MTIE

Figure 8



SCG4000 Series Typical TDEV

Figure 9



SCG4000 Individual Features:

- Four selectable References: 8, 16, 32, and 64 kHz.
- LVPECL Oscillator Output: 125.0 MHz or 155.52 MHz
- CMOS reference output frequency equals input reference frequency.

The SCG4000 is Connor-Winfield's base model for the SCG4000 Series product line. The SCG4000 can lock to one of four input reference frequencies from 8 to 64 kHz which is selectable using two input control pins.

Input Reference Selection

Table 11 SCG4000

Input Sel A (Pin #5)	Input Sel B (Pin #6)	Reference Frequency (Pin #8)
0	0	8 kHz (default)
1	0	16 kHz
0	1	32 kHz
1	1	64 kHz

Reference and Output Availability

Table 12 SCG4000

Input Reference (Pin #4)	LVPECL Oscillator Output (Pin #16 & #18)	CMOS Reference Output (Pin #7)
8 kHz	125.0 MHz	8 kHz
8 kHz 16 kHz 32 kHz 64 kHz	155.52 MHz	8 kHz 16 kHz 32 kHz 64 kHz

Ordering Information

SCG4000-125.0M

SCG4000-155.52M

SCG4010 Individual Features:

- Input Reference: 19.44 MHz
- LVPECL Oscillator Output: 125.0 MHZ or 155.52 MHz
- CMOS Reference Output: 19.44 MHz

The SCG4010 only accepts a 19.44 MHz input while providing a phase locked LVPECL output. Also provided is a phase locked 19.44 MHz CMOS reference output.

Input Reference Selection

Table 13 SCG4010

Input Sel A (Pin #5)	Input Sel B (Pin #6)	Reference Frequency (Pin #8)
X	X	19.44 MHz (default)

Note: X= Don't Care

Reference and Output Availability

Table 14 SCG4010

Input Reference (Pin #4)	LVPECL Oscillator Output (Pin #16 & #18)	CMOS Reference Output (Pin #7)
19.44 MHz	125.0 MHz, 155.52 MHz	19.44 MHz

Ordering Information

SCG4010-125.0M

SCG4010-155.52M

SCG4030 Individual Features:

- Four selectable References: 8, 16, 32, and 64 kHz.
- 45/55 Duty cycle
- LVPECL Oscillator Output: 125.0MHz or 155.52 MHz
- CMOS reference output frequency equals input reference frequency.

The SCG 4030 is similar to the SCG4000 except the SCG4030 offers a duty cycle of 45/55 for applications that require a tighter duty cycle.

The SCG4030 can lock to one of four input reference frequencies from 8 to 64 kHz which is selectable using two input control pins.

Input Reference Selection

Table 17 SCG4030

Input Sel A (Pin #5)	Input Sel B (Pin #6)	Reference Frequency (Pin #8)
0	0	8 kHz (default)
1	0	16 kHz
0	1	32 kHz
1	1	64 kHz

Reference and Output Availability

Table 18 SCG4030

Input Reference (Pin #4)	LVPECL Oscillator Output (Pin #16 & #18)	CMOS Reference Output (Pin #7)
8 kHz	125.0 MHz	8 kHz
8 kHz 16 kHz 32 kHz 64 kHz	155.52 MHz	8 kHz 16 kHz 32 kHz 64 kHz

Ordering Information

SCG4030-125.0M

SCG4030-155.52M

CONNOR WINFIELD

2111 Comprehensive Drive
Aurora, Illinois 60505
Phone: 630-851-4722
Fax: 630-851-5040
www.conwin.com

Revision	Revision DateNote	
A00	05/02/01	Advance informational release
A01	06/15/01	Corrected Table 10
A02	06/20/01	Added the SCG4030 specs
A03	06/27/01	Added the SCG4020 specs
A04	01/08/02	Added 125.0 MHz to all models