Ordering number : ENN6238

CMOS IC

LC895199K

32× CD-ROM Decoder with ATAPI (IDE) Interface

Overview

The LC895199K is a CD-ROM decoder IC that provides subcode read functions and an ATAPI interface integrated on the same chip.

Functions

- CD-ROM ECC function
- Subcode read function
- ATA-PI (IDE) I/F (register block, etc.)
- CAV audio function

Features

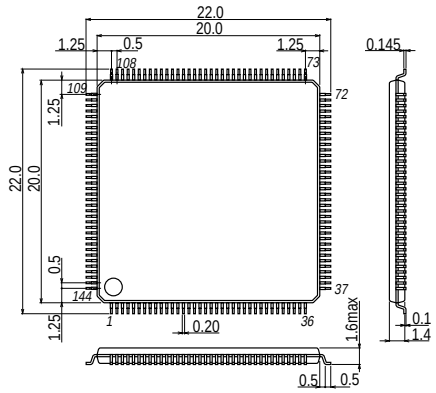
- Built-in ATAPI (IDE) I/F
- 32× speed supported:
  Using EDO-DRAM (×16, 50 ns)
  16.6 Mbytes/s (with IORDY)
  Operating frequency: 33.8688 MHz
- 32× speed supported:
  Using EDO-DRAM (×16, 45 ns)
  16.6 Mbytes/s (without IORDY)
  Operating frequency: 33.8688 MHz
- 24× speed supported:
  Using EDO-DRAM (×16, 50 ns)
  16.6 Mbytes/s (without IORDY)
  Operating frequency: 33.8688 MHz
- 1 Mbits to 4 Mbits of buffer RAM connectable in case of DRAM
- CD main channel, C2 flag, and subcode areas in buffer RAM can be freely set by user
- Built-in batch transfer function (function for sending CD main channel, C2 flag, subcode, etc. at one time)
- Built-in multi-block transfer function (function for automatically sending several blocks at one time)
- Built-in CAV audio function
- Built-in intelligent functions (auto buffering, auto decoding, CD-R support, etc.)
- Built-in subcode P to W buffering function (NO-ECC) and CD-TEXT support
- Package: SQFP-144

Package Dimensions

unit: mm

3214-SQFP144

[LC895199K]



SANYO: SQFP144

SANYO Electric Co.,Ltd. Semiconductor Company
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

Changes from the LC895199

Items changed from the LC895199-MK2

- Revision 4.
- The DVD-ROM and DVD-RAM interface functions have been removed.
- The buffer circuits for the DRAM pins (RAS, CAS0, CAS1, OE, WE, and A0 to A8) have been changed from 8 mA sink to 4 mA sink.
- The buffer circuits for the D/A converter output pins (DSDATA, DLRCK, DBCK) have been changed from 8 mA sink to 4 mA sink.
- The amount of external DRAM supported has been changed from 16M to 4M.
- The MCK3 output has been changed to a 1/1, 1/2, stop output.
- Settings have been added for cases when the PLL circuit is not used. (W register R46 bit 7 (set to 1) and C register R1 (set to 40h))

Specifications

Absolute Maximum Ratings at V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	$V_{DD}5$ max	Ta = 25°C	–0.3 to +6.0	V
	$V_{DD}3$ max	Ta = 25°C	–0.3 to +4.6	V
Input/output voltage	V_I15, V_O5	Ta = 25°C	–0.3 to $V_{DD}5$ + 0.3	V
	V_I13, V_O3	Ta = 25°C	–0.3 to $V_{DD}3$ + 0.3	V
Allowable power dissipation	Pd max	Ta ≤ 70°C	550	mW
Operating temperature	Topr		–30 to +70	°C
Storage temperature	Tstg		–55 to +125	°C
Soldering temperature (pin part only)		10 s	235	°C
Input/output power	I_I, I_O	*	±20	mA

Note: * Per 1 input/output reference cell

Allowable Operating Range at Ta = –30 to +70°C, V_{SS} = 0 V

I_O Cell 5.0 V Supply Voltage

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	V_{DD}		4.5	5.0	5.5	V
Input voltage range	V_{IN}		0		V_{DD}	V

Internal Cell 3.3 V Supply Voltage

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	V_{DD}		3.0	3.3	3.6	V
Input voltage range	V_{IN}		0		V_{DD}	V

DC Characteristics at Ta = –30 to +70°C, V_{SS} = 0 V, V_{DD} = 4.5 to 5.5 V

Parameter	Symbol	Conditions	Applicable pins *1	Ratings			Unit
				min	typ	max	
Input high-level voltage	V_{IH}	TTL levels	(1)	2.2	—	—	V
Input low-level voltage	V_{IL}			—	—	0.8	V
Input high-level voltage	V_{IH}	TTL levels	(10)	2.2	—	—	V
Input low-level voltage	V_{IL}	with pull-down resistor		—	—	0.8	V
Input high-level voltage	V_{IH}	TTL levels	(2), (3), (11)	2.4	—	—	V
Input low-level voltage	V_{IL}	Schmitt		—	—	0.8	V
Output high-level voltage	V_{OH}	I_{OH1} = –4 mA	(4)	V_{DD} – 2.1	—	—	V
Output low-level voltage	V_{OL}	I_{OL1} = 4 mA		—	—	0.4	V
Output high-level voltage	V_{OH}	I_{OH1} = –8 mA	(10), (12)	V_{DD} – 2.1	—	—	V
Output low-level voltage	V_{OL}	I_{OL1} = 8 mA		—	—	0.4	V
Output high-level voltage	V_{OH}	I_{OH1} = –12 mA	(5)	V_{DD} – 2.1	—	—	V
Output low-level voltage	V_{OL}	I_{OL1} = 12 mA		—	—	0.4	V
Output high-level voltage	V_{OH}	I_{OH1} = –12 mA	(5)	V_{DD} – 2.1	—	—	V
Output low-level voltage	V_{OL}	I_{OL1} = 12 mA		—	—	0.4	V
Output high-level voltage	V_{OH}	I_{OH1} = –4 mA	(8), (11)	V_{DD} – 2.1	—	—	V
Output low-level voltage	V_{OL}	I_{OL1} = 24 mA		—	—	0.4	V
Output low-level voltage	V_{OL}	I_{OL1} = 24 mA	(9)	—	—	0.4	V
Output low-level voltage	V_{OL}	I_{OL1} = 8 mA	(6), (7)	—	—	0.4	V
Input leakage current	I_{IL}	V_I = V_{SS}, V_{DD}	(1), (2), (3), (11)	–10		+10	µA
Output leakage current	I_{OZ}	During high-impedance output	(6), (8), (9), (11)	–10		+10	µA
Pull-up resistance	R_{UP}		(10)	40	80	160	kΩ
Pull-up resistance	R_{UP}	ZDMACK *2	(7)	20	40	80	kΩ

Notes:1. The applicable pin sets are as follows.

2. When ZDMACK is reset, internal pull-up resistor is OFF.
When Config-Reg-R46 (PULON)-bit 0 (ZDMACK) = 1, pull-up resistor becomes ON.

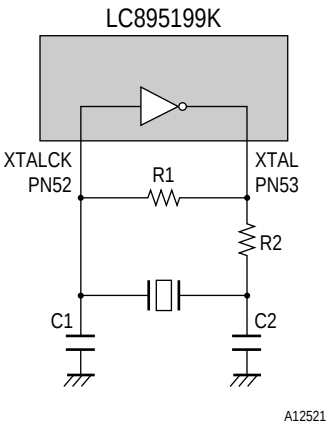
INPUT
(1) ATPINSEL, CSCTRL, SUA0 to SUA6, BCK, C2PO, LRCK, SDATA, SBS0, SCOR, WFCK, TEST0 to TEST1
(2) ZRESET, ZCS, ZRD, ZWR, CSEL
(3) DA0 to DA2, ZCS1FX, ZCS3FX, ZDIOR, ZDIOW, ZDMACK, ZHRST

OUTPUT
(4) RA0 to RA8, ZRAS0, ZCAS0 to ZCAS1, ZUWE, ZLWE, ZOE
(5) MCK, MCK3
(6) ZRSTCPU
(7) ZINT, ZINT1, ZSWAIT
(8) DMARQ, HINTRQ
(9) IORDY, ZIOCS16

INOUT
(10) D0 to D7, IO0 to IO15, HDB0 to HDB7
(11) DD0 to DD15, ZDASP, ZPDIAG
(12) EXCK

Note: Pins XTAL and XTALCK are not included in the DC characteristics.

Recommended Oscillator Circuit



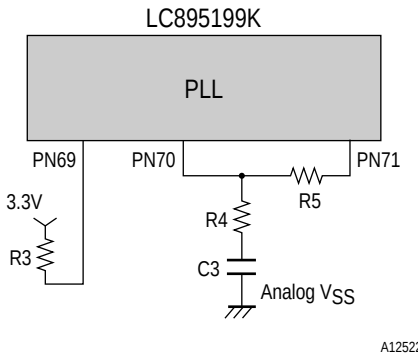
R1 = 1 MΩ
R2 = 47 Ω
C1 = 0
C2 = 47 pF

Ceramic oscillator frequency = 33.8688 MHz.

The 33.8688 MHz frequency in the recommended circuit is the third harmonic.

Since the exact values of these components will vary depending on characteristics of the printed circuit board used and other factors, consult the manufacturer of the oscillator element when designing the oscillator circuit.

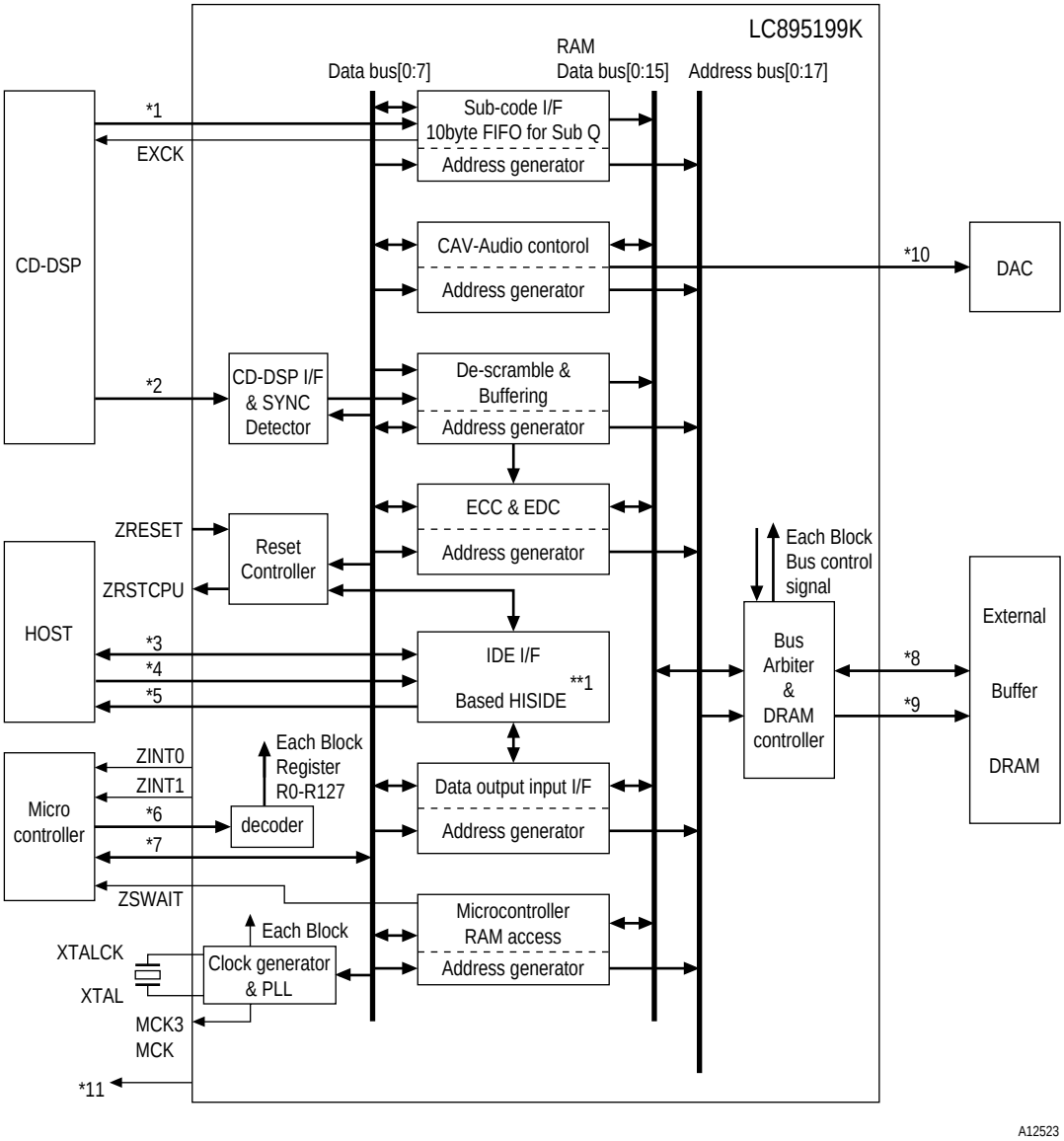
External Circuits for the On-Chip PLL Version (LC895199)



R3 = 5.1 kΩ, R4 = 200 Ω, R5 = 10 kΩ, C3 = 0.1 µF

The analog V_{DD} and V_{SS} must be made completely independent of the logic system power supply. In particular, they must not be affected by fluctuations in the logic system power supply.

Block Diagram



*1 WFCK, SBSO, SCOR
*2 BCK, SDATA, LRCK, C2PO
*3 DD0 to DD15, ZDASP, ZPDIAG
*4 ZCS1FX, ZCS3FX, DA0 to DA2, ZDIOR, ZDIOW, ZDMACK, CSEL
*5 DMARQ, HINTRQ, ZIOCS16, IORDY, ZHRST
*6 ZRD, ZWR, SUA0 to SUA6, ZCS, CSCTRL
*7 D0 to D7
*8 IO0 to IO15
*9 RA0 to RA8, ZRAS0, ZCAS0, ZCAS1, ZOE, ZUWE, ZLWE
*10 DBCK, DLRCK, DSDATA
*11 IOP0 to IOP7
**1 HISIDE(WD25C32) is made by WESTERN DIGITAL

Pin Functions

LC895199K Pin Functions
(When pin 103 (ATPINSEL) is low)

Type					
I	INPUT	B	BIDIRECTION	NC	NOT CONNECT
O	OUTPUT	P	POWER		

Pin No.	Pin name	Type	Pin functions
1	V_{SS0}	P	
2	ZRAS0	O	Buffer DRAM RAS signal output
3	ZCAS0	O	Buffer DRAM CAS signal output 0 (Normally held at 0 (low).)
4	ZCAS1	O	Buffer DRAM CAS signal output 1
5	V_{SS0}	P	
6	ZOE	O	Buffer DRAM output enable
7	ZUWE	O	Buffer DRAM upper write enable
8	ZLWE	O	Buffer DRAM lower write enable
9	V_{SS0}	P	
10	RA0	O	Data buffer DRAM address signal outputs
11	RA1	O	
12	RA2	O	
13	RA3	O	
14	RA4	O	
15	RA5	O	
16	RA6	O	
17	RA7	O	
18	V_{DD0}	P	5.0 V
19	V_{SS0}	P	
20	RA8	O	Data buffer DRAM address signal output
21	IO0	B	Data buffer DRAM data input and output These pins have built-in pull-up resistors.
22	IO1	B	
23	IO2	B	
24	IO3	B	
25	IO4	B	
26	IO5	B	
27	V_{SS0}	P	
28	IO6	B	Data buffer DRAM data input and output These pins have built-in pull-up resistors.
29	IO7	B	
30	IO8	B	
31	IO9	B	
32	IO10	B	
33	IO11	B	
34	IO12	B	
35	IO13	B	
36	V_{SS0}	P	
37	V_{DD1}	P	3.3 V
38	IO14	B	Data buffer DRAM data input and output These pins have built-in pull-up resistors.
39	IO15	B	
40		NC	
41	V_{SS0}	P	
42	IOP0	B	General-purpose input and output ports
43	IOP1	B	
44	IOP2	B	
45	IOP3	B	
46	IOP4	B	
47	IOP5	B	
48	IOP6	B	
49	IOP7	B	
50		NC	
51	TEST0	I	Test pin. This pin must be connected to V_{SS} in normal operation.
52	XTALCK	I	Crystal oscillator circuit input

Continued on next page.

Continued from preceding page.

Pin No.	Pin	I/O	Function
53	XTAL	O	Crystal oscillator circuit output
54	V_{DD0}	P	5.0 V
55	V_{SS0}	P	
56	MCK	O	XTALCLK 1/1, 1/2, and stop output
57	TEST1	I	Test pin. This pin must be connected to V_{SS} in normal operation.
58	DSDATA	O	D/A converter outputs
59	DLRCK	O	
60	DBCK	O	
61	C2PO	I	CD DSP interface
62	SDATA	I	
63	BCK	I	
64	LRCK	I	
65	EXCK	O	Subcode input and output
66	WFCK	I	
67	SBSO	I	
68	SCOR	I	
69	PLL1		PLL circuit connections
70	PLL2		
71	PLL3		
72	V_{SS0}	P	(This is an analog V_{SS} pin in the LC895199 built-in PLL version.)
73	V_{DD1}	P	3.3 V (This is an analog V_{DD} pin in the LC895199 built-in PLL version.)
74	ZRESET	I	IC reset
75	MCK3	O	XTALCLK 1/1, 1/5, 2/5, 1/512, and stop output
76	CSCTRL	I	Microcontroller CS pin active low/active high selection
77	ZRD	I	Microcontroller data read signal input
78	ZWR	I	Microcontroller data write signal input
79	ZCS	I	Register chip select input from the microcontroller
80	SUA0	I	Microcontroller register selection signals
81	SUA1	I	
82	SUA2	I	
83	SUA3	I	
84	SUA4	I	
85	SUA5	I	
86	SUA6	I	
87	D0	B	Microcontroller data signals These pins have built-in pull-up resistors.
88	D1	B	
89	D2	B	
90	V_{DD0}	P	5.0 V
91	V_{SS0}	P	
92	D3	B	Microcontroller data signals These pins have built-in pull-up resistors.
93	D4	B	
94	D5	B	
95	D6	B	
96	D7	B	
97	ZINT0	O	Interrupt request signal output to the microcontroller
98	ZINT1	O	
99	ZSWAIT	O	Wait signal output to the microcontroller
100	ZRSTCPU	O	CPU reset signal
101	CSEL	I	ATAPI control signals
102	ZHRST	I	
103	ATPINSEL	I	ATAPI pin layout selection. (This pin must be connected to V_{SS0}.)
104	ZDASP	B	
105	ZCS3FX	I	
106	ZCS1FX	I	
107	DA2	I	

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Pin No.	Pin	I/O	Function
108	V_{SS1}	P	
109	V_{DD1}	P	3.3 V
110	DA0	I	ATAPI control signals
111	ZPDIAG	B	
112	DA1	I	
113	ZIOCS16	O	
114	HINTRQ	O	
115	ZDMACK	I	
116	V_{SS1}	P	
117	IORDY	O	ATAPI control signals
118	ZDIOR	I	
119	ZDIOW	I	
120	DMARQ	O	
121	V_{SS1}	P	
122	DD15	B	ATAPI data bus
123	DD0	B	
124	DD14	B	
125	DD1	B	
126	V_{DD0}	P	5.0 V
127	V_{SS1}	P	
128	DD13	B	ATAPI data bus
129	DD2	B	
130	DD12	B	
131	DD3	B	
132	V_{SS1}	P	
133	DD11	B	ATAPI data bus
134	DD4	B	
135	DD10	B	
136	V_{SS1}	P	
137	V_{DD0}	P	5.0 V
138	DD5	B	ATAPI data bus
139	DD9	B	
140	DD6	B	
141	V_{SS1}	P	
142	DD8	B	ATAPI data bus
143	DD7	B	
144	V_{DD1}	P	3.3 V

Unused (“NC”) pins must be left open.
Pins whose name begin with Z operate with inverted (negative) logic.
V_{SS0} is the logic system ground and V_{SS1} is the IDE interface driver ground.
Applications must supply 5.0 V for V_{DD0} and 3.3 V for V_{DD1}.

Pin Functions

LC895199K Pin Functions
(When pin 103 (ATPINSEL) is high)

Type					
I	INPUT	B	BIDIRECTION	NC	NOT CONNECT
O	OUTPUT	P	POWER		

Pin No.	Pin name	Type	Pin functions
1	V_{SS0}	P	
2	ZRAS0	O	Buffer DRAM RAS signal output
3	ZCAS0	O	Buffer DRAM CAS signal output 0 (Normally held fixed at 0 (low).)
4	ZCAS1	O	Buffer DRAM CAS signal output 1
5	V_{SS0}	P	
6	ZOE	O	Buffer DRAM output enable
7	ZUWE	O	Buffer DRAM upper write enable
8	ZLWE	O	Buffer DRAM lower write enable
9	V_{SS0}	P	
10	RA0	O	Data buffer DRAM address signal outputs
11	RA1	O	
12	RA2	O	
13	RA3	O	
14	RA4	O	
15	RA5	O	
16	RA6	O	
17	RA7	O	
18	V_{DD0}	P	5.0 V
19	V_{SS0}	P	
20	RA8	O	Data buffer DRAM address signal output
21	IO0	B	Data buffer DRAM data input and output These pins have built-in pull-up resistors.
22	IO1	B	
23	IO2	B	
24	IO3	B	
25	IO4	B	
26	IO5	B	
27	V_{SS0}	P	
28	IO6	B	Data buffer DRAM data input and output These pins have built-in pull-up resistors.
29	IO7	B	
30	IO8	B	
31	IO9	B	
32	IO10	B	
33	IO11	B	
34	IO12	B	
35	IO13	B	
36	V_{SS0}	P	
37	V_{DD1}	P	3.3 V
38	IO14	B	Data buffer DRAM data input and output These pins have built-in pull-up resistors.
39	IO15	B	
40		NC	
41	V_{SS0}	P	
42	IOP0	B	General-purpose input and output ports
43	IOP1	B	
44	IOP2	B	
45	IOP3	B	
46	IOP4	B	
47	IOP5	B	
48	IOP6	B	
49	IOP7	B	
50		NC	
51	TEST0	I	Test pin. This pin must be connected to V_{SS} in normal operation.
52	XTALCK	I	Crystal oscillator circuit input

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Pin No.	Pin	I/O	Function
53	XTAL	O	Crystal oscillator circuit output
54	V_{DD}	P	5.0 V
55	V_{SS0}	P	
56	MCK	O	XTALCLK 1/1, 1/2, and stop output
57	TEST1	I	Test pin. This pin must be connected to V_{SS} in normal operation.
58	DSDATA	O	D/A converter outputs
59	DLRCK	O	
60	DBCK	O	
61	C2PO	I	CD DSP interface
62	SDATA	I	
63	BCK	I	
64	LRCK	I	
65	EXCK	O	Subcode input and output
66	WFCK	I	
67	SBSO	I	
68	SCOR	I	
69	PLL1		PLL circuit connections
70	PLL2		
71	PLL3		
72	V_{SS0}	P	(This is an analog V_{SS} pin in the LC895199 built-in PLL version.)
73	V_{DD1}	P	3.3 V (This is an analog V_{DD} pin in the LC895199 built-in PLL version.)
74	ZRESET	I	IC reset
75	MCK3	O	XTALCLK 1/1, 1/5, 2/5, 1/512, and stop output
76	CSCTRL	I	Microcontroller CS pin active low/active high selection
77	ZRD	I	Microcontroller data read signal input
78	ZWR	I	Microcontroller data write signal input
79	ZCS	I	Register chip select input from the microcontroller
80	SUA0	I	Microcontroller register selection signals
81	SUA1	I	
82	SUA2	I	
83	SUA3	I	
84	SUA4	I	
85	SUA5	I	
86	SUA6	I	
87	D0	B	Microcontroller data signals These pins have built-in pull-up resistors.
88	D1	B	
89	D2	B	
90	V_{DD0}	P	5.0 V
91	V_{SS0}	P	
92	D3	B	Microcontroller data signals These pins have built-in pull-up resistors.
93	D4	B	
94	D5	B	
95	D6	B	
96	D7	B	
97	ZINT0	O	Interrupt request signal output to the microcontroller
98	ZINT1	O	
99	ZSWAIT	O	Wait signal output to the microcontroller
100	ZRSTCPU	O	CPU reset signal
101	CSEL	I	ATAPI control signal
102	DD7	B	ATAPI data bus
103	ATPINSEL	I	ATAPI pin layout selection. (This pin must be connected to V_{DD0}.)
104	DD8	B	ATAPI data bus
105	DD6	B	
106	DD9	B	
107	DD5	B	

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Pin No.	Pin	I/O	Function
108	V_{SS1}	P	
109	V_{DD1}	P	3.3 V
110	DD10	B	ATAPI data bus
111	DD4	B	
112	DD11	B	
113	DD3	B	
114	DD12	B	
115	DD2	B	
116	V_{SS1}	P	
117	DD13	B	ATAPI data bus
118	DD1	B	
119	DD14	B	
120	DD0	B	
121	V_{SS1}	P	
122	DD15	B	ATAPI data bus
123	DMARQ	O	ATAPI control signal
124	ZDIOW	I	
125	ZDIOR	I	
126	V_{DD0}	P	5.0 V
127	V_{SS1}	P	
128	IORDY	O	ATAPI control signal
129	ZDMACK	I	
130	HINTRQ	O	
131	ZIOCS16	O	
132	V_{SS1}	P	
133	DA1	I	ATAPI control signal
134	ZPDIAG	B	
135	DA0	I	
136	V_{SS1}	P	
137	V_{DD0}	P	5.0 V
138	DA2	I	ATAPI control signal
139	ZCS1FX	I	
140	ZCS3FX	I	
141	V_{SS1}	P	
142	ZDASP	B	
143	ZHRST	I	
144	V_{DD1}	P	3.3 V

Unused (“NC”) pins must be left open.
Pins whose name begin with Z operate with inverted (negative) logic.
V_{SS0} is the logic system ground and V_{SS1} is the IDE interface driver ground.
Applications must supply 5.0 V for V_{DD0} and 3.3 V for V_{DD1}.