Preliminary Specification

CMOS LSI

LE28FV4101T,H-40T/50T/70T
LE28FW4101T,H-45T/55T/70T
LE28FU4101T,H-70T/85T/10T
4M(512K×8bits, 256K×16bits) Flash EEPROM

Features

CMOS Flash EEPROM Technology
Single Voltage Read and Write Operations
- **LE28FV4101 : 3.0V~3.6V**
- **LE28FW4101 : 2.7V~3.6V**
- **LE28FU4101 : 2.3V~3.6V**

Sector Erase Capability: 1kWord per sector
: (2kByte per sector)
Block Erase Capability: 32kWord per Block
: (64kByte per Block)
Fast Access Time
- **LE28FV4101T,H-40T :40ns(Max.)**
- **LE28FV4101T,H-50T :50ns(Max.)**
- **LE28FV4101T,H-70T :70ns(Max.)**

- **LE28FW4101T,H-45T :45ns(Max.)**
- **LE28FW4101T,H-55T :55ns(Max.)**
- **LE28FW4101T,H-70T :70ns(Max.)**

- **LE28FU4101T,H-70T :70ns(Max.)**
- **LE28FU4101T,H-85T :85ns(Max.)**
- **LE28FU4101T,H-10T :100ns(Max.)**

Low Power Consumption
- **Active Current (Read) : 40 mA (Max.)**
- **Standby Current : 40μA (Max.)**

High Read/Write Reliability
- **Sector-write Endurance Cycles: 10^4**
- **10 Years Data Retention**

Latched Address and Data
Self-timed Erase and Programming
Word Programming
- **LE28FV/FW4101 : 20μs (Max.)**
- **LE28FU4101 : 30μs (Max.)**

End of Write Detection :Toggle Bit , DATA# Polling
:RD/BY#
Hardware/Software Data Protection
Protected cell area :
Top Block(16K-Bytes from the top address)
Whole chip(512K-Bytes)
Packages Available :
- **LE28FV,FW,FU4101T :TSOP-48 (12mm x 20mm)**
- **LE28FV,FW,FU4101H :FLGA-52 (6mm x 6mm)**

Product Description

The LE28FV4101/LE28FW4101/LE28FU4101 is a 256K ×16 or 512K ×8 CMOS sector erase, Word(Byte) program EEPROM.
The LE28FV4101/LE28FW4101/LE28FU4101 is manufactured using SANYO's proprietary, high performance CMOS Flash EEPROM technology. Breakthroughs in EEPROM cell design and process architecture attain better reliability and manufacturability compared with conventional approaches.
LE28FV4101/LE28FW4101/LE28FU4101 erases and programs with single power supply.
LE28FV4101/LE28FW4101/LE28FU4101 is offered in FLGA52 (6mm x 6mm) packages and TSOP48(12mm x 20mm) package.

Featuring high performance programming, LE28FV4101/LE28FW4101/LE28FU4101 programs in 20μs/30μs(max). The LE28FV4101/LE28FW4101/LE28FU4101 sector (1k Words) erases in 25ms(Max.). Both program and erase times can be optimized using interface feature such as Toggle bit, DATA# Polling or RD/BY# to indicate the completion of the write cycle. To protect against an inadvertent write, the LE28FV4101/LE28FW4101/LE28FU4101 has on chip hardware and software data protection schemes. Designed, manufactured, and tested for a wide spectrum of applications, LE28FV4101/LE28FW4101/LE28FU4101 is offered with a guaranteed sector write endurance of 10^4 cycles. Data retention is rated greater than 10 years.

Device Operation

The LE28FV4101/LE28FW4101/LE28FU4101 operates random read, Word(Byte)-program, sector or block or Chip-erase flash memory.
The Self-Power Conservation feature automatically puts the LE28FV4101/LE28FW4101/LE28FU4101 in a low power mode after data has been accessed with a valid read operation. This reduces the I_{DD} active read current from 40mA(Max) to 300μA(Typ.). The device exits the Self Power Conservation mode with any address transition or control signal transition used to initiate another read cycle, with no access time penalty.

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Standby

Standby mode reduces current consumption greatly with the Output pins in High-Impedance state. By setting both of CE# and RESET# to VDD ±0.3V ,otherwise RESET# to VSS ±0.3V, device enter the standby mode.

Standby mode cannot be set when the device is not in read mode.(i.e Erase or Program mode)

Read

The read operation is controlled by CE# and OE#, a chip enable and output enable both have to be low for the system to obtain data from the outputs. When CE# is high, the chip is deselected. OE# is the output control and is used to gate data from the output pins. The data bus is in high impedance state when OE# is high. Refer to the timing waveforms for further details (Figure 3~4).

Write

All write operations are initiated by the JEDEC approved Software Data Protect (SDP) entry sequence, for Chip_Erase, Block_Erase, Sector_Erase and Program. Program and all erase commands have a fixed duration, that will not vary over the life of the device, i.e., are independent of the number of erase/program cycles endured.

The device is always in the Software Data Protected mode for all Write operations. Write operations are controlled by toggling of WE# or CE#. The address bus is latched on the falling edge of WE# or CE#, whichever occurs last. The data bus is latched on the rising edge of WE# or CE#, whichever occurs first. After SDP sequence, the device enter the selected mode automatically. When the wrong address or data are offered, the device interrupt the SDP mode at once and go back to read mode. See Figure 5~8 for the timing waveform.

Program

The program operation consists of issuing the SDP program command.

Its command can be to program value to one address in memory cell array at a time. The command require 4-bus cycle operation, the final write operation latches the address and data in the internal state machine. Programming operation starts with either the rising of WE#, CE#, whichever occurs first. The Program operation, once initiated, will be completed within 20μs(30μs).

See Figure 17~20 program cycle timing waveform, Table 3 for the command sequence, and Figure 33 for a Flowchart.

Note that the Program command cannot change a bit set at "0" back to "1". One of the Erase command must be used to the all bit in sector ,Block or in the whole memory from "0" to "1".

Chip-Erase

The LE28FV4101/LE28FW4101/LE28FU4101 provides a chip-erase mode, which allows the user to clear the Flash array to the "1" state. This is useful when the entire device must be quickly erased.

The chip erase mode is initiated by issuing the specific six-Word loading sequence, as in the Software Data Protection operation. After the loading cycle, the device enters into an internally timed cycle. See Table 3 for specific codes, Figure 13~16 for the timing waveform, and Figure 32 for a flowchart.

Block-Erase

The LE28FV4101/LE28FW4101/LE28FU4101 provides a block-erase mode.

Block-Erase mode is based on uniform Block size of 32KWord(64kByte), which allows the user to clear any block in the Flash array to the "1" state.

The block-erase mode is initiated by issuing the specific six-Word loading sequence, as in the Software Data Protect operation. After the loading cycle, the device enters into an internally timed erase cycle. See Table 3 for specific codes, Figure 13~16 for the timing waveform, and Figure 31 for a flowchart.

Sector-Erase

The LE28FV4101/LE28FW4101/LE28FU4101 provides a sector-erase mode

Sector-Erase mode is based on uniform sector size of 1kWord(2kByte), which allows the user to clear any sector in the Flash array to the "1" state.

The sector-erase mode is initiated by issuing the specific six-Word loading sequence, as in the Software Data Protect operation. After the loading cycle, the device enters into an internally timed erase cycle. See Table 3 for specific codes, Figure 13~16 for the timing waveform, and Figure 30 for a flowchart.

Chip Protection , Block Protection / Un-protection

Chip Protection and Block Protection disables both program and erase operation.

Chip Protection defends from inadvertent write in the whole memory, and consists of issuing the SDP command.

Block Protection defends 8kWord(16kByte) Top Block from inadvertent write, and consists of issuing the SDP command.

Un-protection can be canceling both Chip Protection and Block Protection, and consists of issuing the SDP command.

See Table 3 for specific codes, Figure 21~22 for the timing waveform.

Protect Verification

Protect Verification mode indicate Chip Protection or Block Protection status, consists of issuing the SDP command. See Table 3 for specific codes.
To verify which protect mode the device is in, read following addresses and the data shows the protect mode. i.e.
Address(0004H:Byte mode,0002H Word mode) ,
Data(01H:Byte mode,0001H: Word mode) shows sector protect.
Address(0004H:Byte mode,0002H: Word mode),
Data(00H:Byte mode,0000H: Word mode) shows unprotect.
Address(0006H:Byte mode,0003H Word mode),
Data(01H:Byte mode,0001H Word mode) shows chip protect.
Address(0006H:Byte mode,0003H: Word mode),
Data(00H:Byte mode,0000H Word mode) shows unprotect.

In order to return to the standard read mode, the Protect Verification mode must be exited. Exit is accomplished by issuing the Read/Reset command, which returns the device to normal operation.

Write Operation Status Detection

The LE28FV4101/LE28FW4101/LE28FU4101 provides two software means to detect the completion of write cycle, in order to optimize the system write cycle time. The software detection includes two status bits: DATA# Polling (DQ_7) and Toggle Bit (DQ_6). The end of write detection mode is enabled after the rising edge of WE#, which initiates the internal write, erase, or program cycle.

The actual completion of the nonvolatile write is asynchronous with the system; therefore, either a DATA# Polling or Toggle Bit read may be simultaneous with the completion of the write cycle. If this occurs, the system will possibly get an erroneous result, i.e. valid data may appear to conflict with either DQ_7 or DQ_6. In order to prevent spurious device rejection, if an erroneous result occurs, the software routine should include a loop to read the accessed location an additional two (2) times. If both reads are valid, then the device has completed the write cycle, otherwise the rejection is valid.

DATA# Polling (DQ_7)

When the LE28FV4101/LE28FW4101/LE28FU4101 is in the internal Flash write cycle, any attempt to read DQ_7 of the last Word loaded during the Flash Word-load cycle will receive the complement of the true data. Once the write cycle is completed, DQ_7 will show true data. The device is then ready for the next operation. See Figure 28 for Flash DATA# Polling timing waveforms.

Toggle Bit (DQ_6)

During the Flash internal write cycle, any consecutive attempts to read DQ_6 will produce alternating 0's and 1's, i.e. toggling between 0 and 1. When the write cycle is completed, the toggling will stop. The device is then ready for the next operation. See Figure 29 for Flash Toggle Bit timing waveforms.

RD/BY#

LE28FV4101/LE28FW4101/LE28FU4101 has RD/BY# pin to be able to detect the completion of a Write cycle. Output form of RD/BY# pin is internally connected to the open drained transistor. When the pin is at "L", the device is busy for a write cycle. When the pin is at "High-Z", the device is ready for accepting commands. Because of RD/BY# pin being open drain, User needs to connect a pull up resistor between RD/BY# pin and VDD. If User use a number of Flash memories, User may as well connect the pull up resistor to the memories in parallel.
See Figure 26~27 for RD/BY# timing waveforms.

Data Protection

The LE28FV4101/LE28FW4101/LE28FU4101 provides both hardware and software features to protect nonvolatile data from inadvertent writes.

Hardware Data Protection

Write Inhibit Mode: Forcing OE# low, CE# high, or WE# high will inhibit the write operation.
Noise/Glitch Protection: A WE# pulse of less than 5 ns will not initiate a write cycle.
VDD Power Up/Down Detection: Immediately after the power-up, the device is in read mode. The write operation is inhibited when VDD is less than 1.5 volts. This prevents inadvertent writes during power-up or power-down.

Software Data Protection (SDP)

The LE28FV4101/LE28FW4101/LE28FU4101 provide the JEDEC approved software data protection scheme as a requirement for initiating a Write, Erase, or Program operation. With this scheme, any write operation requires the inclusion of a series of three Cycle-load operations to precede the Word program operation. The three Cycle-load sequence is used to initiate the program cycle, providing optimal protection from inadvertent write operations, e.g., during the system power-up or power-down. The six-Cycle Sequence is required to initiate any chip, block, or sector erase operation.

The requirements for JEDEC compliant SDP are in Byte formats. The LE28FV4101/LE28FW4101/LE28FU4101 are organized by Word; therefore, the contents of DQ_8 to DQ_{15} are "Don't care" during any SDP (3-Cycle or 6-Cycle) command sequence.

During the SDP load command sequence, the SDP load cycle is suspended when WE# is high. This means a read may occur during the SDP load sequence.

Hardware RESET

To quit the Erase or Program operation, LE28FV4101/ LE28FW4101/ LE28FU4101 can be reset by forcing RESET# pin into low. After receiving RESET# pulse, the device begins Reset operation and terminates the Reset operation 10μs(max) later. After the hardware reset operation, all output pins are in high-impedance state when RESET# is "L", or device is in read mode after the period of tRST by setting RESET# pin "H".

Product Identification

The product identification mode identifies the device manufacturer as SANYO. Users may wish to use the device ID operation to identify the write algorithm requirements. For details, see Table 3 for software operation and Figures 23~24 for timing waveforms.

Read/RESET

In order to return to the standard read mode, the Product Identification mode must be exited. Exit is accomplished by issuing the Read/Reset command, which returns the device to normal operation. This command may also be used to reset the device to the read mode after any inadvertent transient condition that apparently causes the device to behave abnormally, e.g., not read correctly.
Immediately after the power-up, device should be set to read mode without using READ/RESET command. For details, see Table 3 for software operation and Figures 9~12 for timing waveforms.

Decoupling Capacitors

Ceramic capacitor (0.1μF) must be added between V_{DD} and V_{SS} for each device to assure stable flash memory operation.

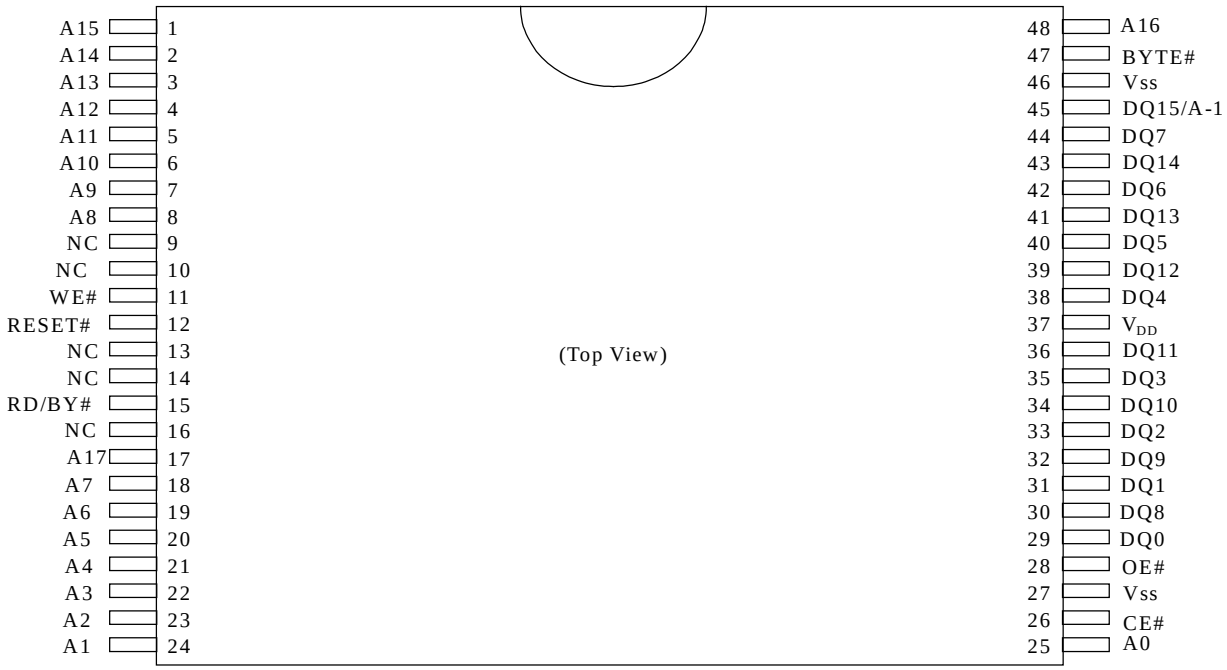
The attention to the usage of this LSI

For the reasons of using ATD (Address Transition Detector) Circuit, the output data of this LSI directly after supplying voltage, program operation or erase operation are invalid. The valid data would be offered after the transition of at least one of CE# or address signals under the stable voltage.

In case of power on, We recommend to input "RESET#" signal in order to do initial the internal circuit.

Figure1: Pin Connection

TSOP-48(12mm x 20mm)



FLGA-52(6mm x 6mm) Top View (Land facing down)

H	G	F	E	D	C	B	A	
NC	A7	NC	NC	RESET#	NC	A9	NC	1
A5	A6	A17	NC	WP#	A8	A10	A11	2
A3	A4		RD/BY#	NC		A12	A13	3
A1	A2	NC			NC	A14	A15	4
A0	CE#	NC			NC	BYTE#	A16	5
VSS	OE#		DQ10	DQ12		DQ15	VSS	6
DQ0	DQ8	DQ9	DQ3	DQ4	DQ13	DQ14	DQ7	7
NC	DQ1	DQ2	DQ11	VDD	DQ5	DQ6	NC	8

Figure2: Functional Block Diagram

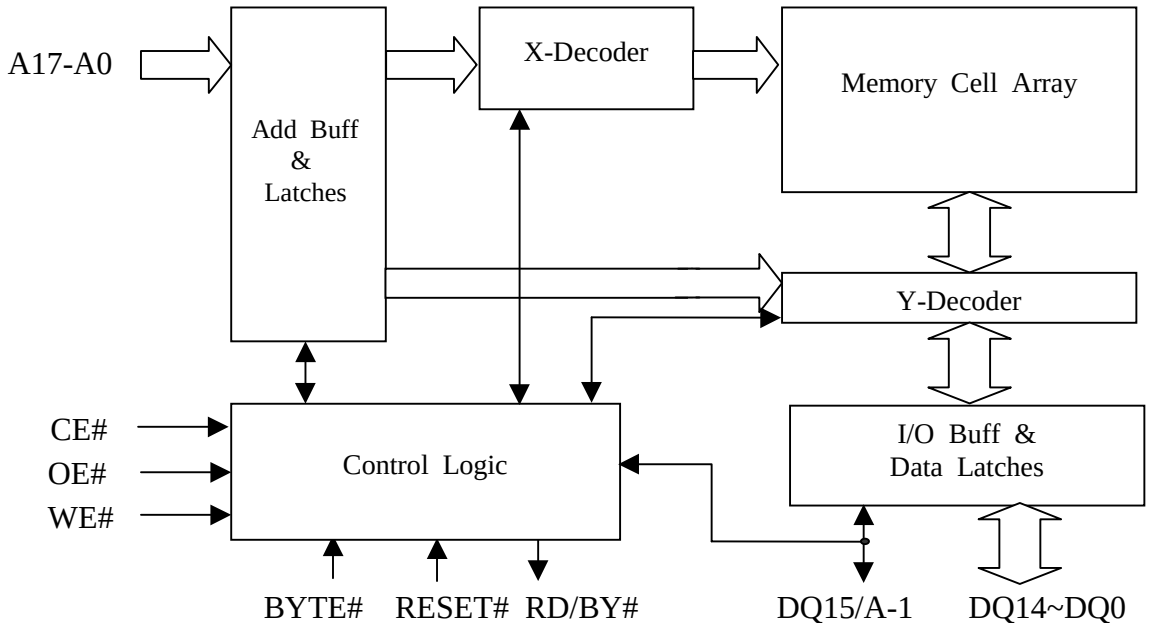


Table1: Pin Description

Symbol	Pin Name	Functions
A17-A0	Address Inputs	To provide memory address. Addresses are internally latched during write cycle.
DQ14-DQ0	Data Input/Output	To output data during read cycle and receive input data during write cycles. Data is internally latched during a write cycle. The outputs are in high-Impedance when OE# or CE# is high.
DQ15/A-1	Data Input/Output or address Input	When BYTE# is High (WORD mode), This pin is DQ15 Input/Output. When BYTE# is Low (BYTE mode), This pin behaves as an address input.
CE#	Chip Enable	To activate the device when CE# is low. Deselects and puts the device to standby, when CE# is high.
OE#	Output Enable	To activate the data output buffers. OE# is active low.
WE#	Write Enable	To activate the write operation. WE# is active low.
BYTE#	Select BYTE/WORD	Device operates in the BYTE mode, When BYTE# is low. Device operates in the WORD mode, When BYTE# is high.
RESET#	Hardware Reset Input	Hardware method to reset the device for reading array data. RESET# is active low.
RD/BY#	Ready / Busy	When output is low, The device is actively erasing or programming.
VDD	Power Supply	To provide 3.0V~3.6V-Volt supply (LE28FV4101) To provide 2.7V~3.6V-Volt supply (LE28FW4101) To provide 2.3V~3.6V-Volt supply (LE28FU4101)
V_{SS}	Ground	
NC	No Connection	Unconnected Pins

Table 2: Operation Modes Selection

Byte Mode (BYTE#="L")

Mode	CE#	OE#	WE#	RESET#	Address	DQ7-0	DQ14-8	DQ15/A-1
Read	VIL	VIL	VIH	VIH	AIN	DOUT	High-Z	AIN
Write	VIL	VIH	VIL	VIH	AIN	DIN	High-Z	AIN
Standby / Write Inhibit	VIH	X	X	VIH	X	High-Z	High-Z	X
Write Inhibit	X	VIL	X	VIH	X	High-Z/DOUT	High-Z	X
	X	X	VIH	VIH	X	High-Z/DOUT	High-Z	X
Reset	X	X	X	VIL	X	High-Z	High-Z	X

Word Mode (BYTE#="H")

Mode	CE#	OE#	WE#	RESET#	Address	DQ7-0	DQ14-8	DQ15/A-1
Read	VIL	VIL	VIH	VIH	AIN	DOUT		
Write	VIL	VIH	VIL	VIH	AIN	DIN		
Standby / Write Inhibit	VIH	X	X	VIH	X	High-Z		
Write Inhibit	X	VIL	X	VIH	X	High-Z/DOUT		
	X	X	VIH	VIH	X	High-Z/DOUT		
Reset	X	X	X	VIL	X	High-Z		

Table3: Command Summary

Byte Mode (BYTE#="L")

Command	Required Cycle	Bus Write Cycle											
		1st		2nd		3rd		4th		5th		6th	
		Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data
		Note 1	Note 2	Note 1	Note 2	Note 1	Note 2	Note 1	Note 2	Note 1	Note 2	Note 1	Note 2
Read / Reset	1	XXX	F0										
	3	AAA	AA	555	55	AAA	F0	RA	RD	Note5			
Software ID Entry / Protect Verify	3	AAA	AA	555	55	AAA	90	Note3,4	Note3,4				
Byte Program	4	AAA	AA	555	55	AAA	A0	PA	PD	Note5			
Sector Erase	6	AAA	AA	555	55	AAA	80	AAA	AA	555	55	Note5 SA	30
Block Erase	6	AAA	AA	555	55	AAA	80	AAA	AA	555	55	Note5 BA	50
Chip Erase	6	AAA	AA	555	55	AAA	80	AAA	AA	555	55	AAA	10
Block Protection	4	AAA	AA	555	55	AAA	E0	XXX	00				
Chip Protection	4	AAA	AA	555	55	AAA	D0	XXX	00				
Un-protection	4	AAA	AA	555	55	AAA	E0	XXX	01				

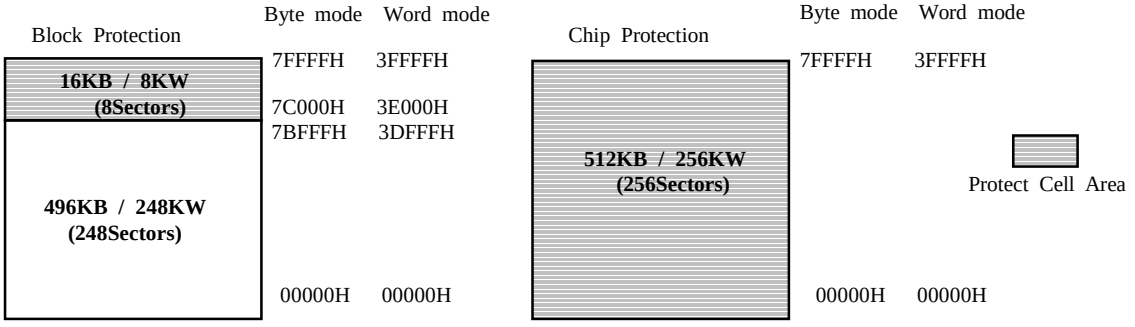
Word Mode (BYTE#="H")

Command	Required Cycle	Bus Write Cycle											
		1st		2nd		3rd		4th		5th		6th	
		Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data
		Note 1	Note 2	Note 1	Note 2	Note 1	Note 2	Note 1	Note 2	Note 1	Note 2	Note 1	Note 2
Read / Reset	1	XXX	F0										
	3	555	AA	2AA	55	555	F0	RA	RD	Note5			
Software ID Entry / Protect Verify	3	555	AA	2AA	55	555	90	Note3,4	Note3,4				
Word Program	4	555	AA	2AA	55	555	A0	PA	PD	Note5			
Sector Erase	6	555	AA	2AA	55	555	80	555	AA	2AA	55	Note5 SA	30
Block Erase	6	555	AA	2AA	55	555	80	555	AA	2AA	55	Note5 BA	50
Chip Erase	6	555	AA	2AA	55	555	80	555	AA	2AA	55	555	10
Block Protection	4	555	AA	2AA	55	555	E0	XXX	00				
Chip Protection	4	555	AA	2AA	55	555	D0	XXX	00				
Un-protection	4	555	AA	2AA	55	555	E0	XXX	01				

Note 1. Address Format: A10~A-1(Byte mode),A11~A0(Word mode). All Value in the table is in hexadecimal.
A17~A11,A-1(Byte mode) and A17~A11(Word mode) are don't cares for unlock cycle and command cycles
Note 2. Data Format: DQ7~DQ0 are in hexadecimal. DQ15~DQ8 are don't cares for unlock cycle and command cycles
Note 3. When Power supply voltage is down, Device is exit Software ID Read and Protect Verification.
Note 4. Software ID Read and Data Protection status. A10~A2,A-1 are VIL(Byte mode), A11~A2 are VIL(Word mode).
- A1,A0=0,0, Manufactures code is "62H" in Byte mode, It is "0062H" in Word mode.
- A1,A0=0,1, Device Code is "02H" in Byte mode, It is "0002H" in Word mode.
- A1,A0=1,0, Block Protection: Data are "01H" in Byte mode or Data are "0001H" in Word mode
  Block Unprotection: Data are "00H" in Byte mode or Data are "0000H" in Word mode
- A1,A0=1,1, Chip Protection: Data are "01H" in Byte mode or Data are "0001H" in Word mode
  Chip Unprotection: Data are "00H" in Byte mode or Data are "0000H" in Word mode

Note 5, RA:Read Address, RD:Read Data, PA:Program Address, PD:Program Data,
SA:Sector Address(A17~A10), BA:Block Address(A17~A15)

Protected Cell Area



Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit	Note
Power Supply Voltage	V_{DD}	-0.5~+4.6	V	1
Input Voltage	V_{IN}	-0.5~V_{DD}+0.5	V	1,2
Input/Output Voltage	V_{DQ}	-0.5~V_{DD}+0.5	V	1,2
Power Dissipation	Pdmax	0.7	W	1,3
Ambient Temperature	Topr	-25~+85	ºC	1
Storage Temperature(TSOP48)	Tstg1	-65~+150	ºC	1
Storage Temperature(FLGA52)	Tstg2	-55~+125	ºC	1

Note1: Stress above those listed under "Absolute Maximum Rating" may cause permanent damage to the device.
Note2: –1.0V to VDD+2.0V for the pulse less than 20ns.
Note3: Ta=25ºC

DC Operating Range 1 / Ta=-25~+85ºC

Parameter		Symbol	Min	max	Unit
Power Supply Voltage	LE28FV4101	V_{DD}	3.0	3.6	V
	LE28FW4101	V_{DD}	2.7	3.6	V
	LE28FU4101	V_{DD}	2.3	3.6	V
Input Low Voltage		V_{IL}	-	V_{DD} x0.2	V
		$V_{IL(CMOS)}$	-	0.3	V
Input High Voltage		V_{IH}	V_{DD} x0.7	-	V
		$V_{IH(CMOS)}$	V_{DD}-0.3	-	V

DC Operating Characteristics

Ta=-25~+85ºC, VDD=3.0V~3.6V :LE28FV4101, VDD=2.7V~3.6V :LE28FW4101, VDD=2.3V~3.6V:LE28FU4101

Symbol	Parameter	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
ICCR	Power Supply Current (Read)	-	-	40	mA	CE# = OE# =V_{IL}, WE# = V_{IH}, all DQs open Address inputs = V_{IH} / V_{IL}, at f=1/tRC VDD=VDDMax
				25	mA	CE# = OE# = V_{IL}, WE# = V_{IH}, all DQs open Address inputs = V_{IH} / V_{IL}, at f=10MHz VDD=VDDMax
ICCW	Power Supply Current (Write)	-	-	40	mA	CE# = WE# = VIL, OE# = VIH, VDD=VDDMax
ISB1	Standby Power Supply Current (TTL Input)	-	-	3	mA	CE# = RESET# = VIH, VDD=VDDMax
		-	-	3	mA	RESET# = VIL, VDD=VDDMax
ISB2	Standby Power Supply Current (CMOS Input)	-	-	40	µA	CE# = RESET# = VDD-0.3V, VDD = VDDMax
		-	-	40	µA	RESET# = VSS+0.3V, VDD = VDDMax
ILI	Input Leakage Current	-	-	10	µA	VIN = VSS ~ VDD, VDD=VDDMax
ILO	Output Leakage Current	-	-	10	µA	VIN = VSS ~ VDD, VDD=VDDMax
VOL	Output Low Voltage	-	-	V_{DD} x 0.15	V	DQL = 2.0mA, VDD=VDDMin
		-	-	0.2V	V	DQL = 100µA, VDD=VDDMin
VOH	Output High Voltage	V_{DD} x 0.85	-	-	V	DQH =-2.0mA, VDD=VDDMin
		V_{DD}-0.2V	-	-	V	DQH =-100µA, VDD=VDDMin

Capacitance (Ta=25ºC, f=1MHz)

Parameter	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	-	-	6	pF
DQ Pin Capacitance	C_{DQ}	V_{DQ}=0V	-	-	12	pF

Note: Sampled only, not 100% tested.

Power-up Timing

Parameter	Symbol	Limit (Min.)	Unit
Power-up to Read Operation	tPU_READ	200	µs
Power-up to Write Operation	tPU_WRITE	200	µs

AC Characteristics

Read Cycle Timing Parameters 1 / Ta=-25~+85ºC VDD=3.0V~3.6V: LE28FV4101

Symbol	Parameter	LE28FV4101						Unit
		-40T		-50T		-70T		
		Min.	Max.	Min.	Max.	Min.	Max.	
TRC	Read Cycle Time	40	-	50	-	70	-	ns
TCE	CE# Access Time	-	40	-	50	-	70	ns
TAA	Address Access Time	-	40	-	50	-	70	ns
TOE	OE# Access Time	-	30	-	35	-	35	ns
TCLZ	CE# Low to Active Output (Note1)	0	-	0	-	0	-	ns
TOLZ	OE# Low to Active Output (Note1)	0	-	0	-	0	-	ns
TCHZ	CE# High to High-Z Output (Note1)	-	20	-	25	-	30	ns
TOHZ	OE# High to High-Z Output (Note1)	-	20	-	25	-	30	ns
TOH	Output Hold Time	0	-	0	-	0	-	ns

Read Cycle Timing Parameters 2 / Ta=-25~+85ºC VDD=2.7V~3.6V: LE28FW4101

Symbol	Parameter	LE28FW4101						Unit
		-45T		-55T		-70T		
		Min.	Max.	Min.	Max.	Min.	Max.	
TRC	Read Cycle Time	45	-	55	-	70	-	ns
TCE	CE# Access Time	-	45	-	55	-	70	ns
TAA	Address Access Time	-	45	-	55	-	70	ns
TOE	OE# Access Time	-	35	-	40	-	40	ns
TCLZ	CE# Low to Active Output (Note1)	0	-	0	-	0	-	ns
TOLZ	OE# Low to Active Output (Note1)	0	-	0	-	0	-	ns
TCHZ	CE# High to High-Z Output (Note1)	-	20	-	25	-	30	ns
TOHZ	OE# High to High-Z Output (Note1)	-	20	-	25	-	30	ns
TOH	Output Hold Time	0	-	0	-	0	-	ns

Note1: This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

Read Cycle Timing Parameters 2 / Ta=-25~+85°C VDD=2.3~3.6V: LE28FU4101

Symbol	Parameter	LE28FU4101						Unit
		-70T		-85T		-10T		
		Min.	Max.	Min.	Max.	Min.	Max.	
TRC	Read Cycle Time	70	-	85	-	100	-	ns
TCE	CE# Access Time	-	70	-	85	-	100	ns
TAA	Address Access Time	-	70	-	85	-	100	ns
TOE	OE# Access Time	-	40	-	45	-	50	ns
TCLZ	CE# Low to Active Output (Note1)	0	-	0	-	0	-	ns
TOLZ	OE# Low to Active Output (Note1)	0	-	0	-	0	-	ns
TCHZ	CE# High to High-Z Output (Note1)	-	30	-	35	-	40	ns
TOHZ	OE# High to High-Z Output (Note1)	-	30	-	35	-	40	ns
TOH	Output Hold Time	0	-	0	-	0	-	ns

Note1: This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

Erase/Program Cycle Timing Parameters 1
/Ta=-25~+85°C,VDD=3.0~3.6V: LE28FV4101 / VDD=2.7~3.6V: LE28FW4101

Symbol	Parameter	LE28FV/FW4101						Unit
		-40T/-45T		-50T/-55T		-70T/-70T		
		Min.	Max.	Min.	Max.	Min.	Max.	
TSE	Sector Erase Cycle Time	-	25	-	25	-	25	ms
TBKE	Block Erase Cycle Time	-	25	-	25	-	25	ms
TCHE	Chip Erase Cycle Time	-	100	-	100	-	100	ms
TBP	Byte Program Cycle Time	-	20	-	20	-	20	µs
TWDP	Word Program Cycle Time	-	20	-	20	-	20	µs
TAS	Address Setup Time	0	-	0	-	0	-	ns
TAH	Address Hold Time	45	-	45	-	45	-	ns
TCES	Chip Enable Setup Time	0	-	0	-	0	-	ns
TCEH	Chip Enable Hold Time	0	-	0	-	0	-	ns
TWES	Write Enable Setup Time	0	-	0	-	0	-	ns
TWEH	Write Enable Hold Time	0	-	0	-	0	-	ns
TOES	Output Enable Setup Time	0	-	0	-	0	-	ns
TOEH	Output Enable Hold Time	0	-	0	-	0	-	ns
TCP	CE# Write Pulse Width	50	-	50	-	50	-	ns
TWP	WE# Write Pulse Width	50	-	50	-	50	-	ns
TDS	Data Setup Time	30	-	30	-	30	-	ns
TDH	Data Hold Time	0	-	0	-	0	-	ns
TCPH	CE# High Pulse Width	30	-	30	-	30	-	ns
TWPH	WE# High Pulse Width	30	-	30	-	30	-	ns
TRP	RESET# Pulse Width	500	-	500	-	500	-	ns
TRST	RESET# Recovery Time	-	10	-	10	-	10	µs
TBYE	Busy Enable Setup Time	-	100	-	100	-	100	ns
TBYH	Busy Enable Hold Time	50	-	50	-	50	-	ns
TBPE	Block Protection Enable Time	-	20	-	20	-	20	µs
TCPE	Chip Protection Enable Time	-	20	-	20	-	20	µs
TPD	Unprotection Enable Time	-	25	-	25	-	25	ms
TRH	Read Enable Time	100	-	100	-	100	-	ns

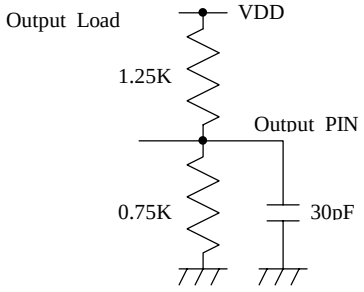
Erase/Program Cycle Timing Parameters 2 /Ta=-25~+85ºC,VDD=2.3~3.6V: LE28FU4101

Symbol	Parameter	LE28FU4101						Unit
		-70T		-85T		-10T		
		Min.	Max.	Min.	Max.	Min.	Max.	
TSE	Sector Erase Cycle Time	-	25	-	25	-	25	ms
TBKE	Block Erase Cycle Time	-	25	-	25	-	25	ms
TCHE	Chip Erase Cycle Time	-	100	-	100	-	100	ms
TBP	Byte Program Cycle Time	-	30	-	30	-	30	µs
TWDP	Word Program Cycle Time	-	30	-	30	-	30	µs
TAS	Address Setup Time	0	-	0	-	0	-	ns
TAH	Address Hold Time	60	-	60	-	60	-	ns
TCES	Chip Enable Setup Time	0	-	0	-	0	-	ns
TCEH	Chip Enable Hold Time	0	-	0	-	0	-	ns
TWES	Write Enable Setup Time	0	-	0	-	0	-	ns
TWEH	Write Enable Hold Time	0	-	0	-	0	-	ns
TOES	Output Enable Setup Time	0	-	0	-	0	-	ns
TOEH	Output Enable Hold Time	0	-	0	-	0	-	ns
TCP	CE# Write Pulse Width	65	-	65	-	65	-	ns
TWP	WE# Write Pulse Width	65	-	65	-	65	-	ns
TDS	Data Setup Time	50	-	50	-	50	-	ns
TDH	Data Hold Time	0	-	0	-	0	-	ns
TCPH	CE# High Pulse Width	35	-	35	-	35	-	ns
TWPH	WE# High Pulse Width	35	-	35	-	35	-	ns
TRP	RESET# Pulse Width	500	-	500	-	500	-	ns
TRST	RESET# Recovery Time	-	10	-	10	-	10	µs
TBYE	Busy Enable Setup Time	-	150	-	150	-	150	ns
TBYH	Busy Enable Hold Time	70	-	70	-	70	-	ns
TBPE	Block Protection Enable Time	-	30	-	30	-	30	µs
TCPE	Chip Protection Enable Time	-	30	-	30	-	30	µs
TPD	Unprotection Enable Time	-	25	-	25	-	25	ms
TRH	Read Enable Time	150	-	150	-	150	-	ns

Note) All the effective input levels are should be kept during above setup or hold time.

AC Test Condition

Input Pulse Levels VIL=VDD x0.1 / VIH=VDD x0.9
Input Rise/Fall Time 5ns
Input and Output timing Reference Levels 1/2 x VDD



Timing Diagram

Figure 3: Read Cycle (Byte Mode: BYTE#="L")

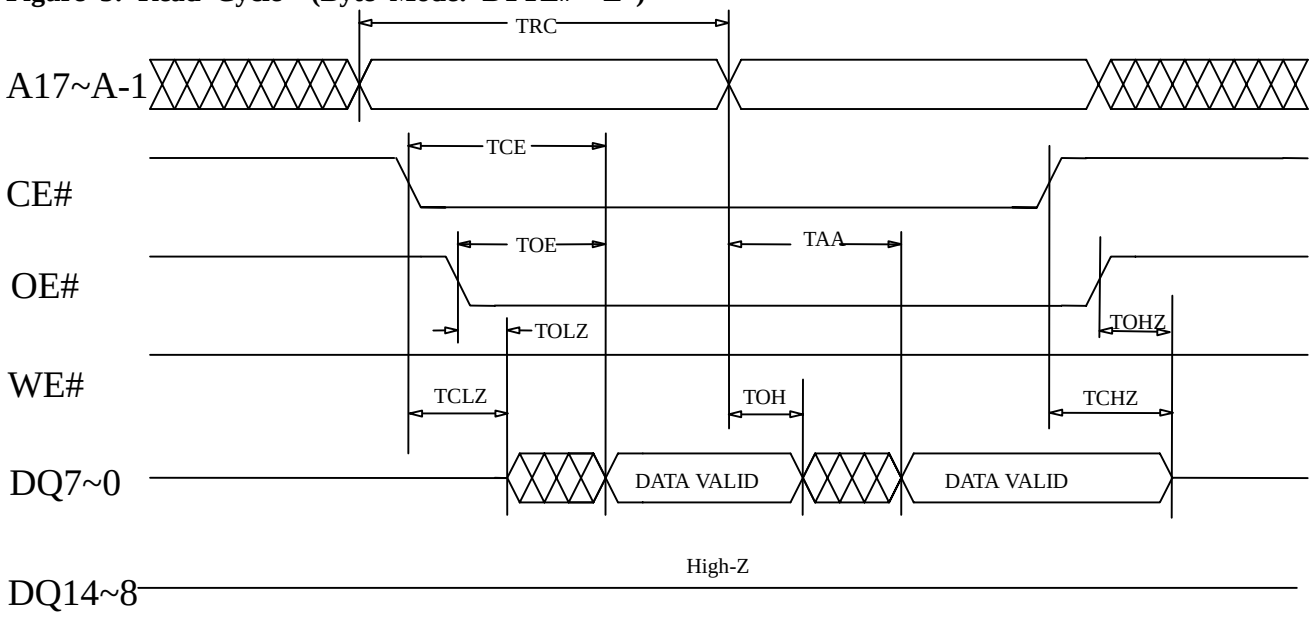


Figure 4: Read Cycle (Word Mode: BYTE#="H")

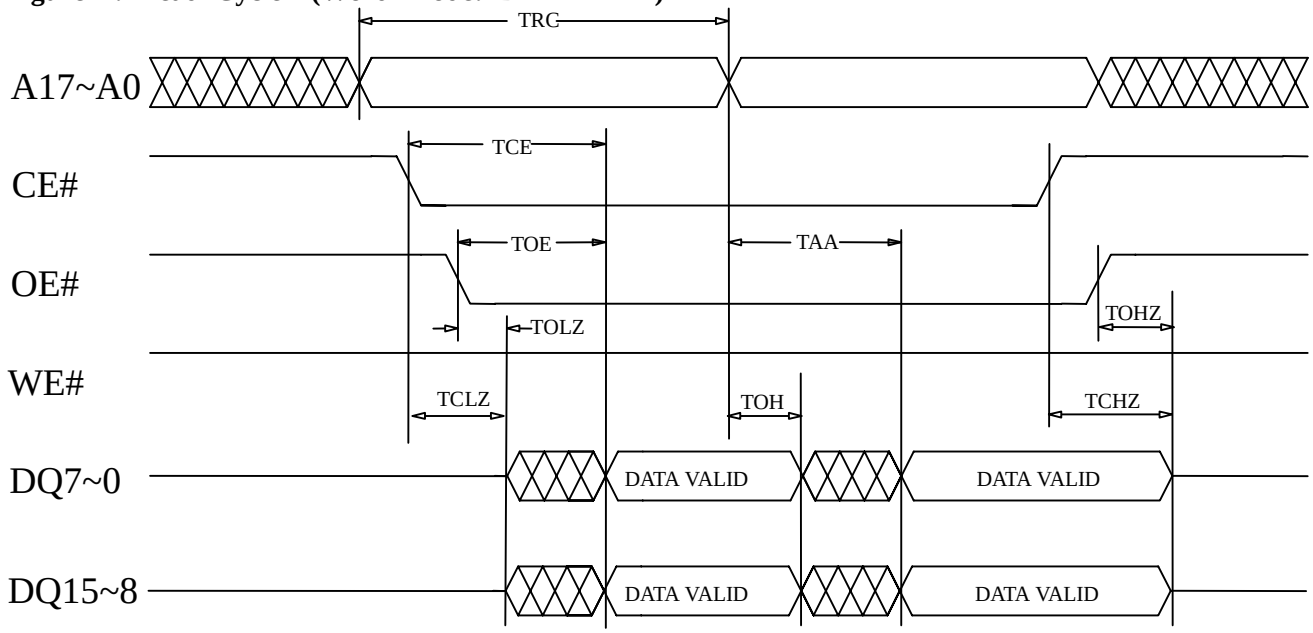


Figure 5: CE# Controlled Write Timing (Byte Mode: BYTE#="L")

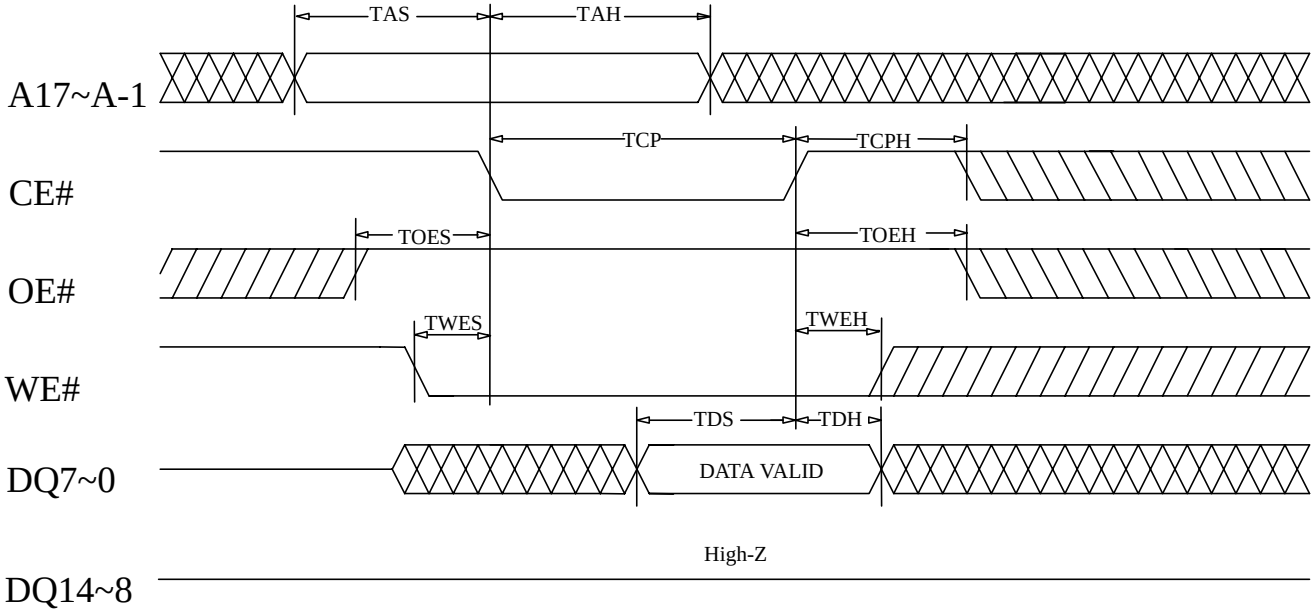


Figure 6: CE# Controlled Write Timing (Word Mode: BYTE#="H")

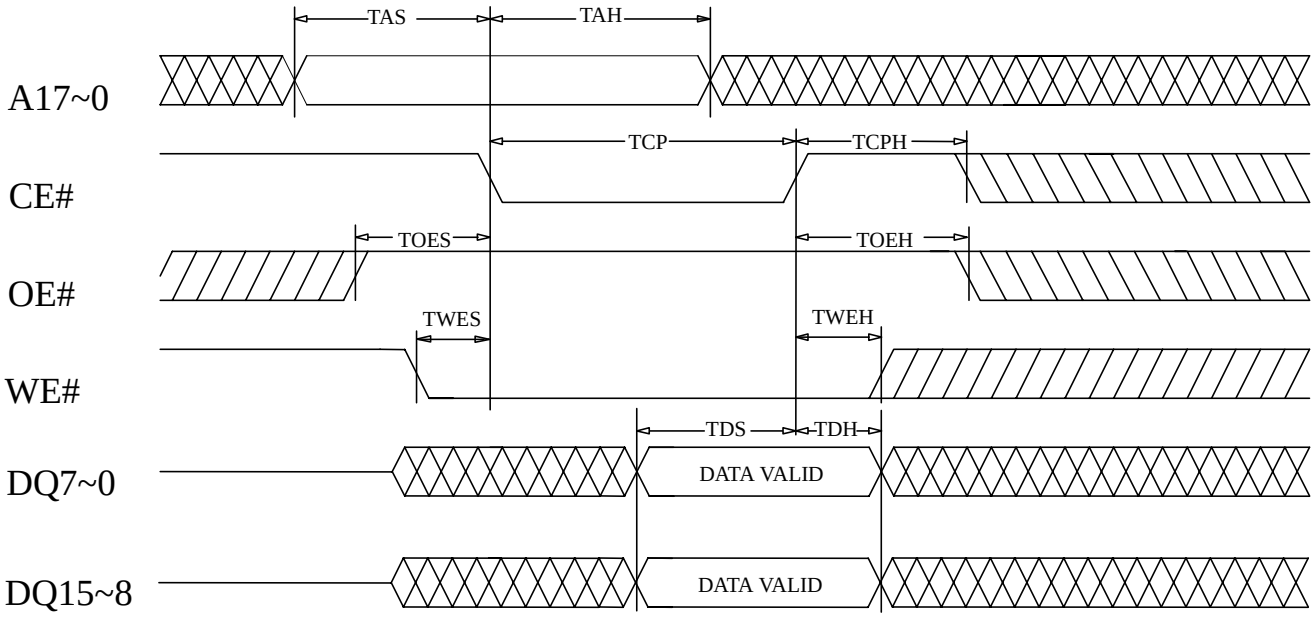


Figure 7: WE# Controlled Write Timing (Byte Mode: BYTE#="L")

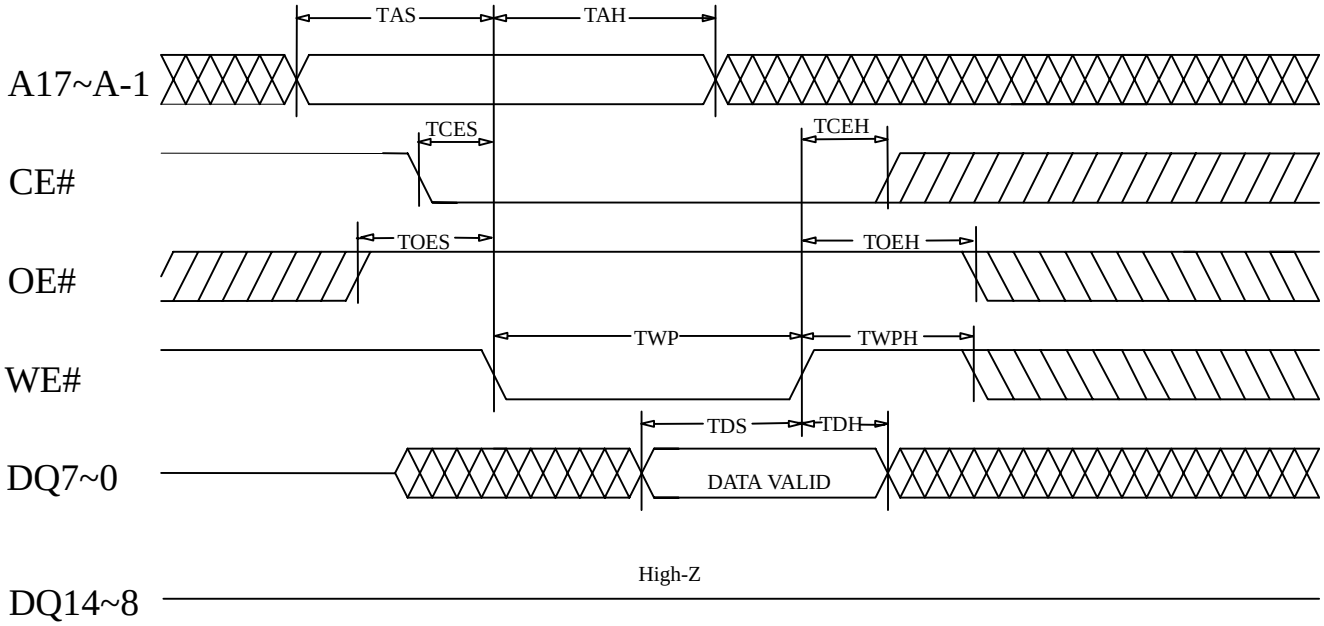


Figure 8: WE# Controlled Write Timing (Word Mode: BYTE#="H")

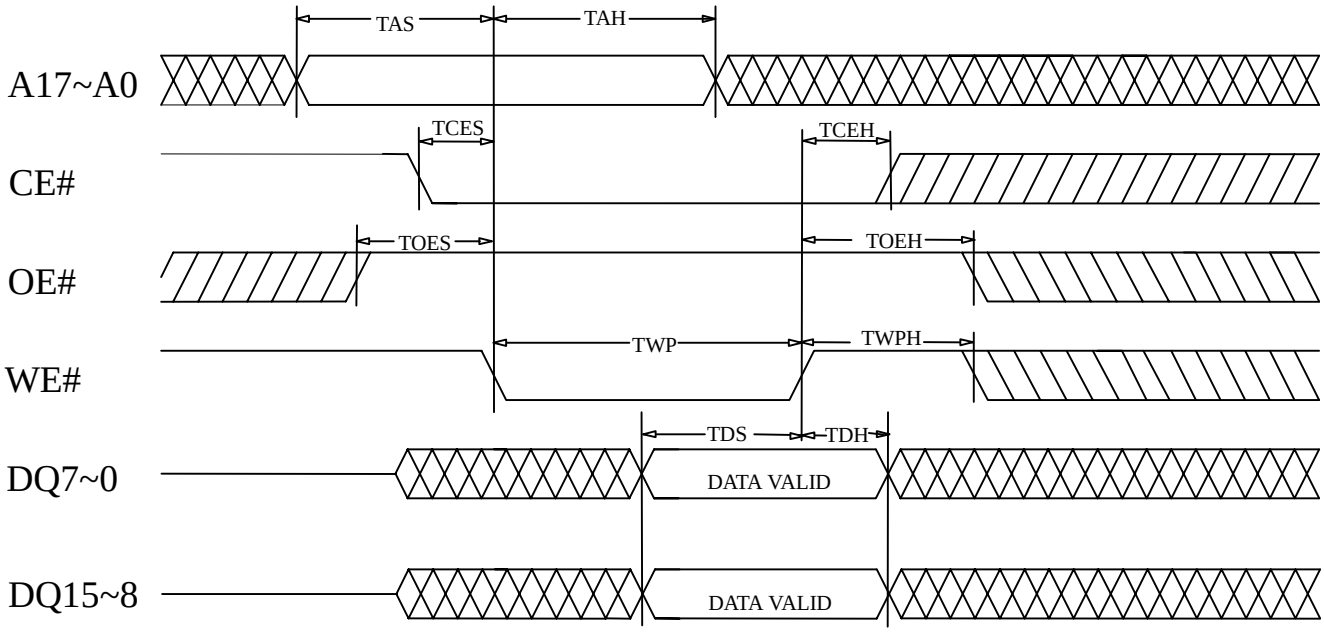


Figure 9: Read / Reset 1 (Byte Mode: BYTE#="L")

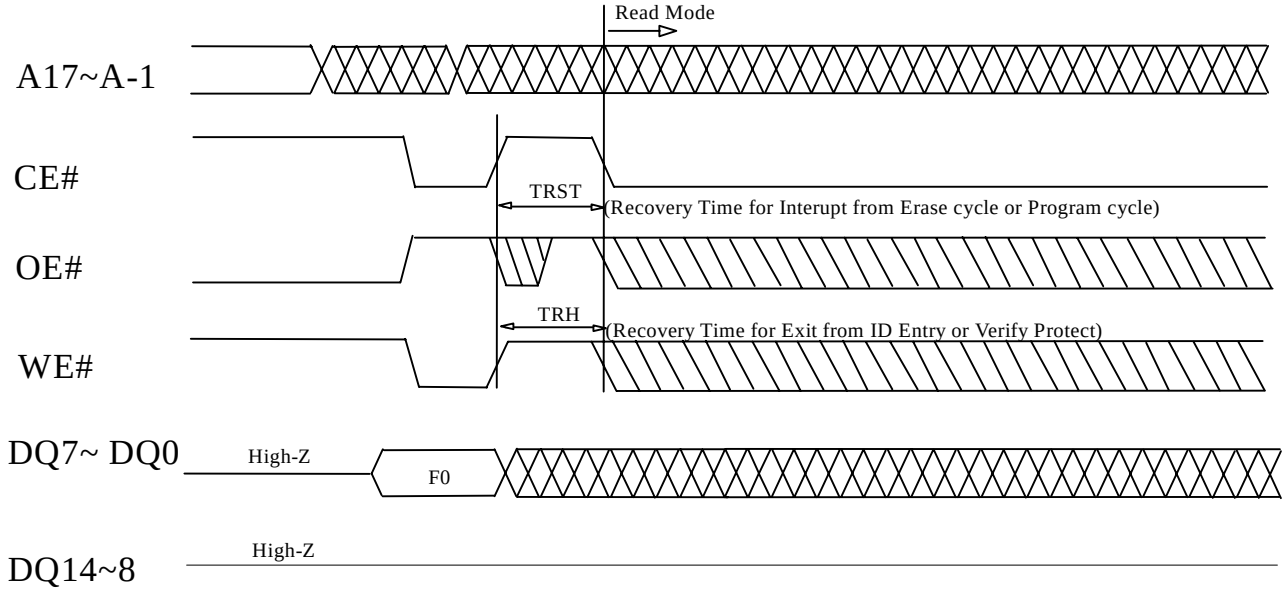


Figure 10: Read / Reset 1 (Word Mode: BYTE#="H")

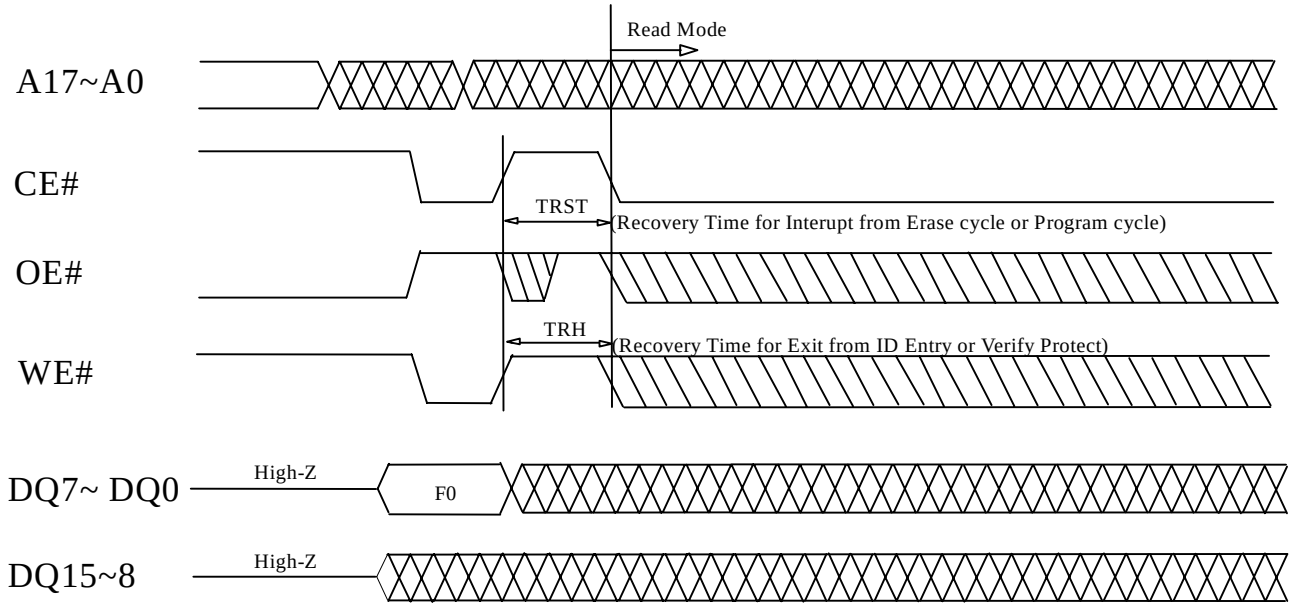


Figure 11: Read / Reset 2 (Byte Mode: BYTE#="L")

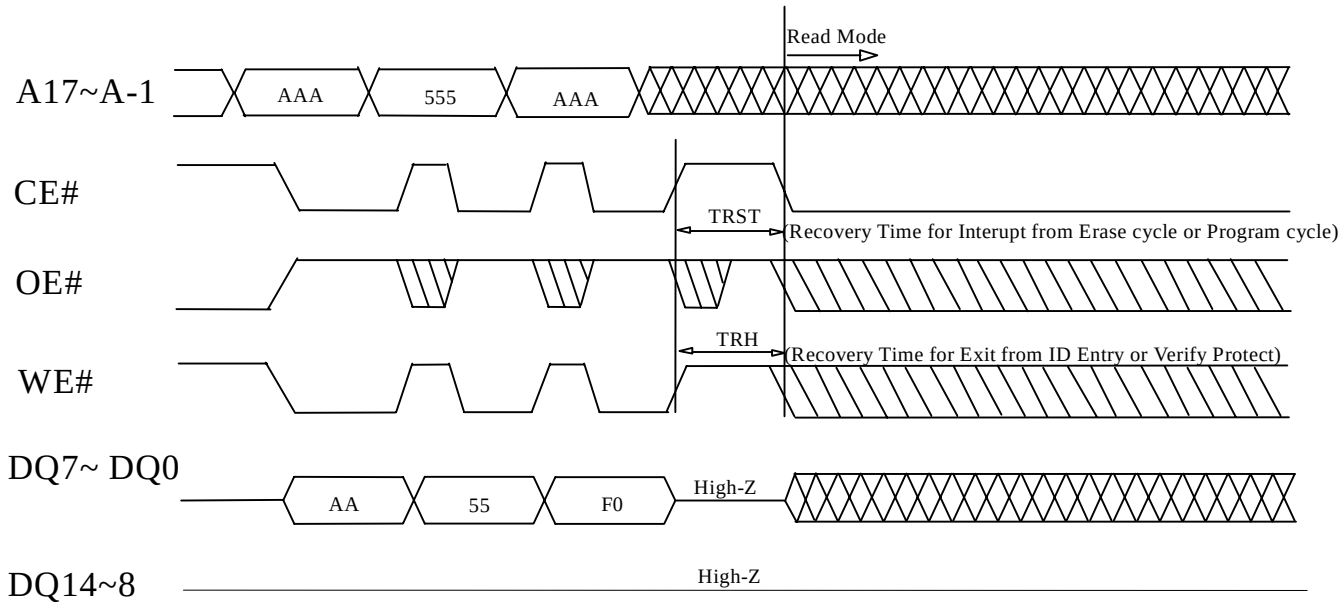


Figure 12: Read / Reset 2 (Word Mode: BYTE#="H")

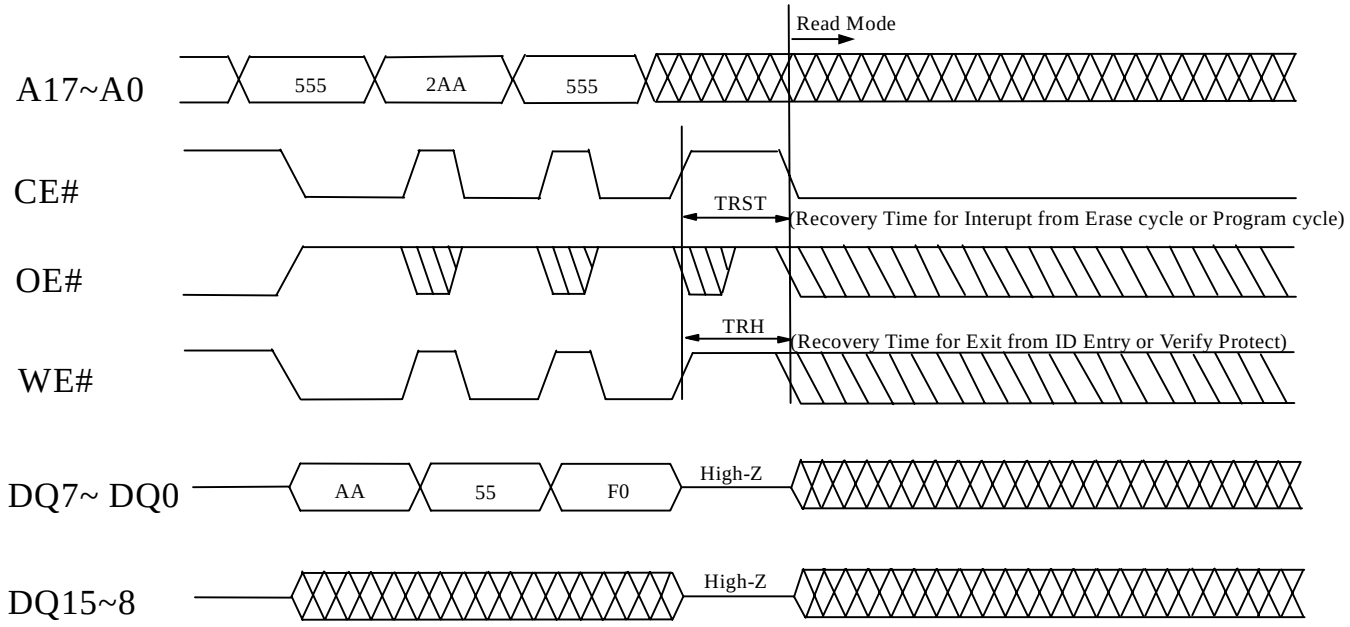


Figure 13: Erase Command Sequence of WE# Control (Byte Mode: BYTE#="L")

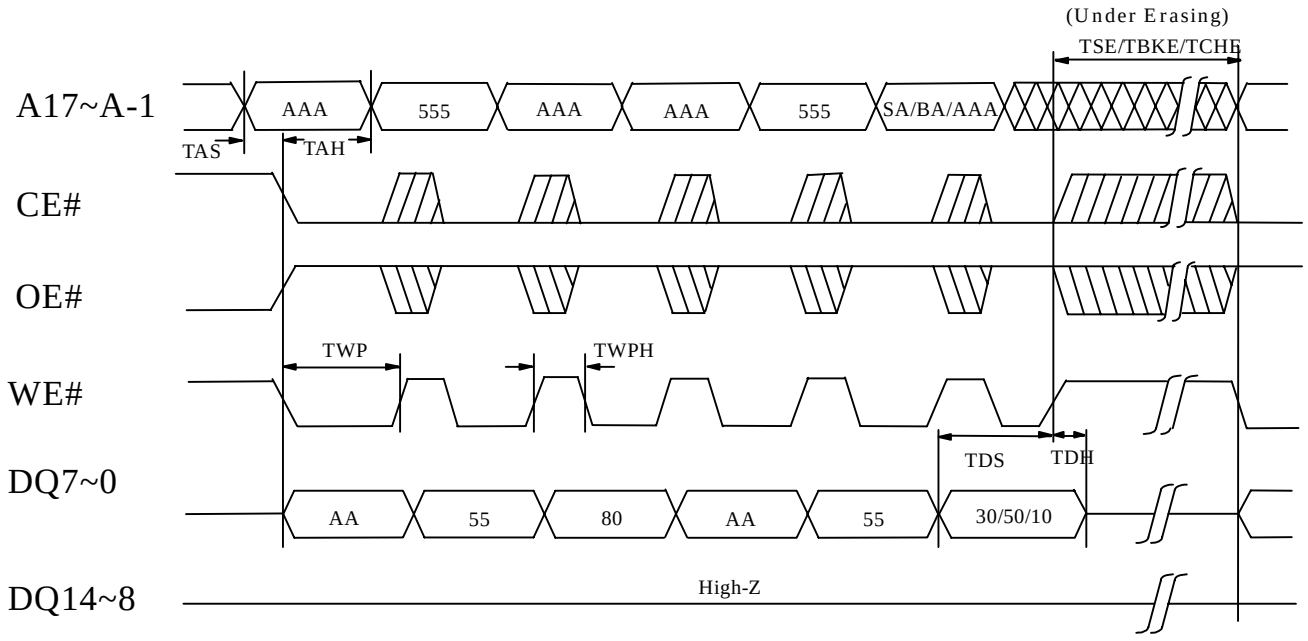


Figure 14: Erase Command Sequence of WE# Control (Word Mode: BYTE#="H")

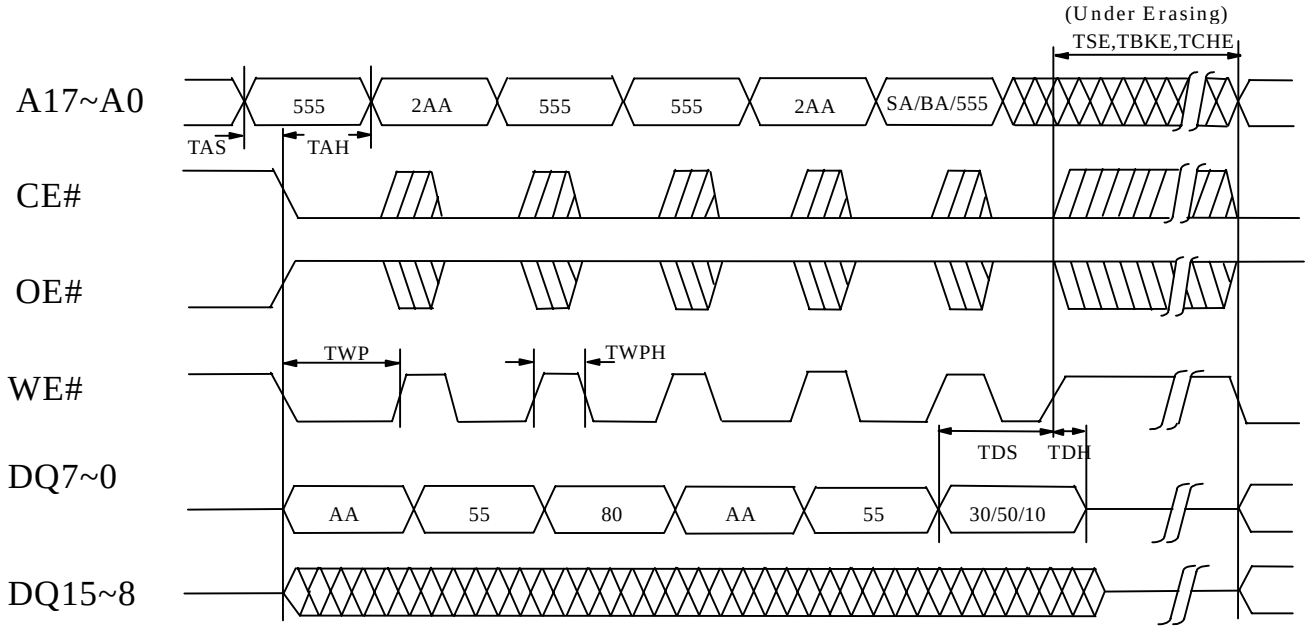


Figure 15: Erase Command Sequence of CE# Control (Byte Mode: BYTE#="L")

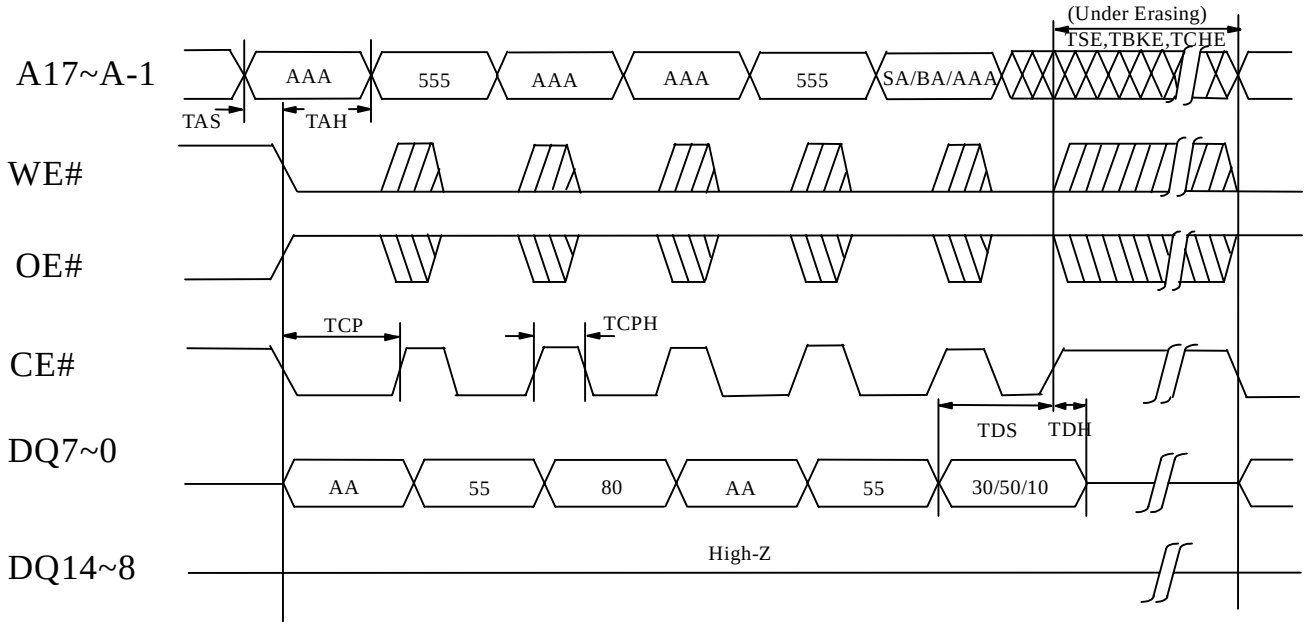


Figure 16: Erase Command Sequence of CE# Control (Word Mode: BYTE#="H")

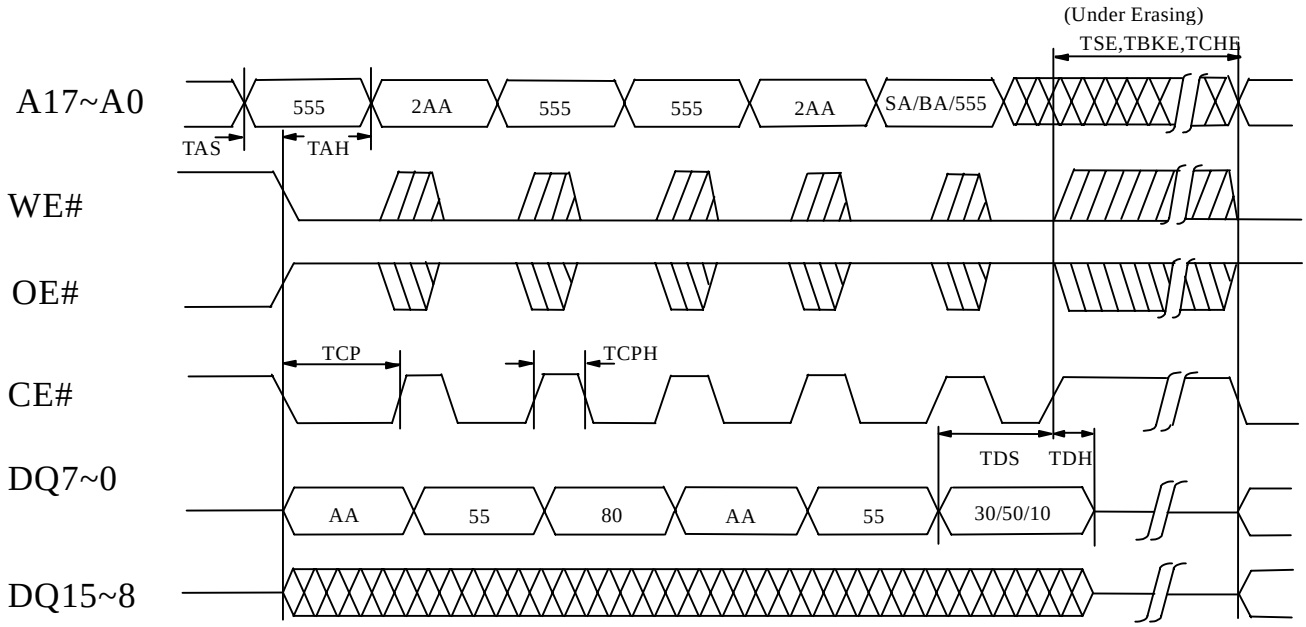


Figure 17: Program Command Sequence of CE# Control (Byte Mode: BYTE#="L")

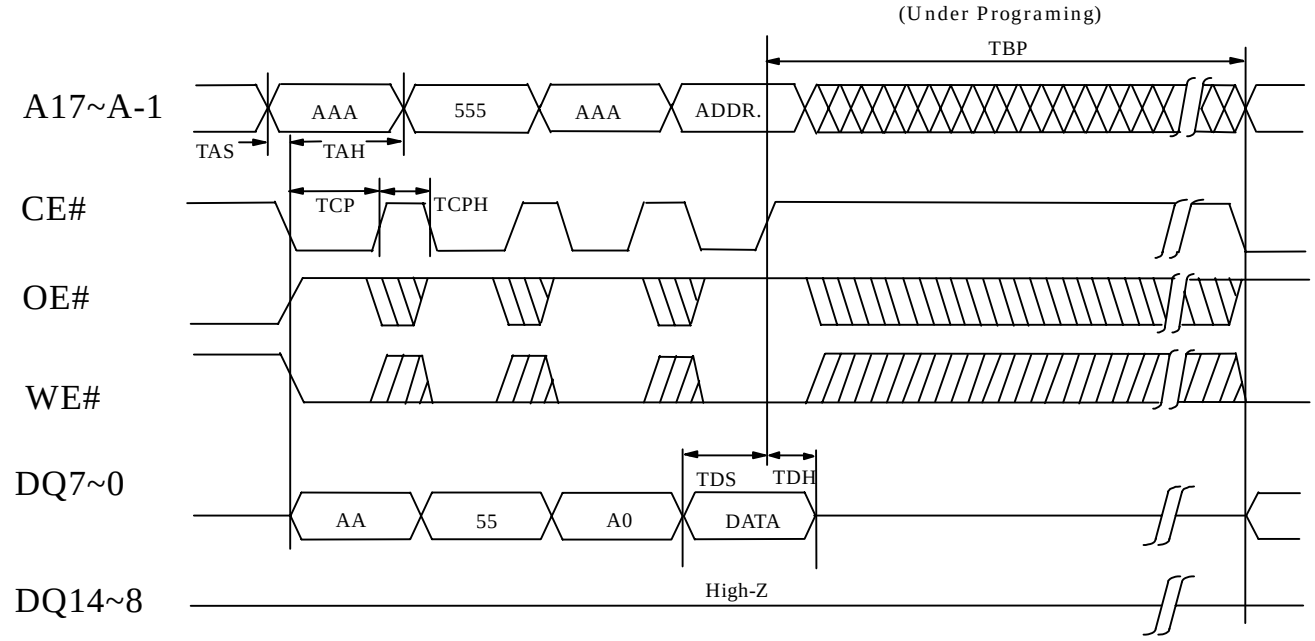


Figure 18: Program Command Sequence of CE# Control (Word Mode: BYTE#="H")

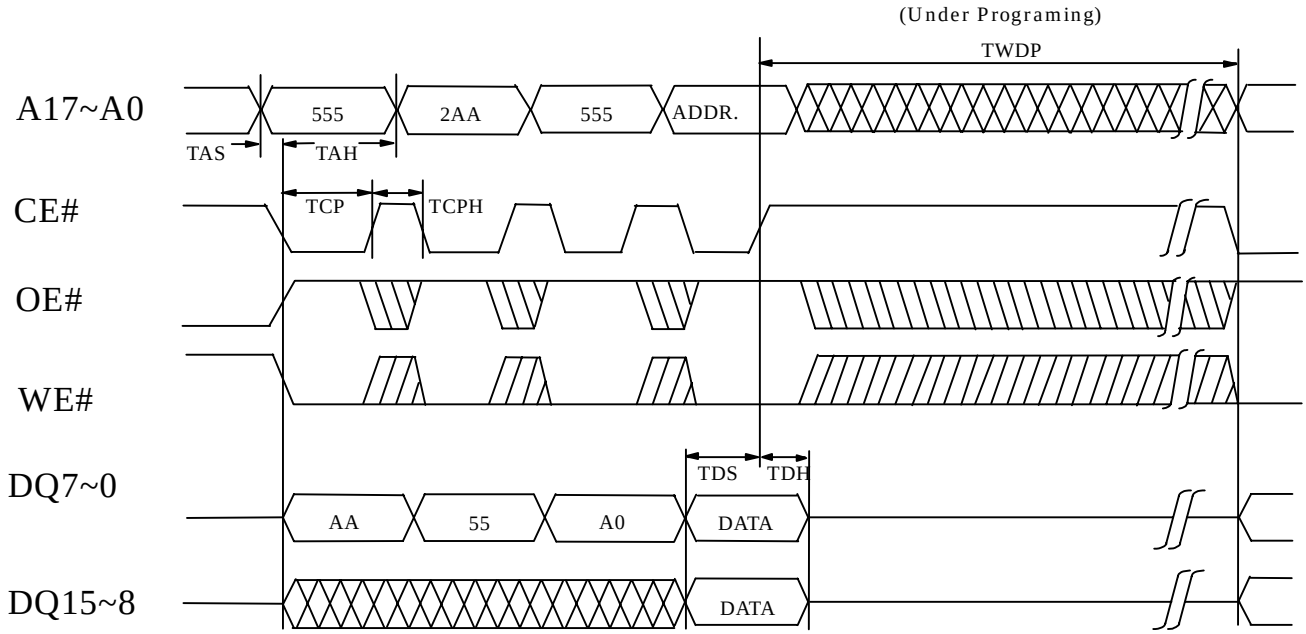


Figure 19: Program Command Sequence of WE# Control (Byte Mode: BYTE#="L")

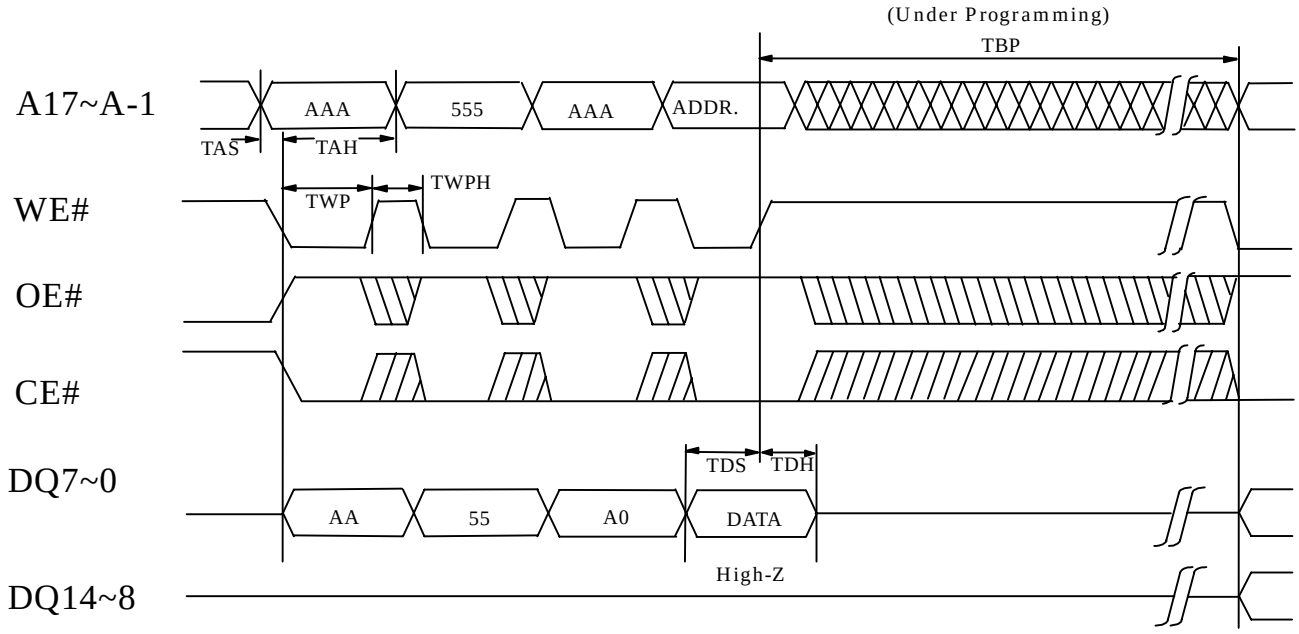


Figure 20: Program Command Sequence of WE# Control (Word Mode: BYTE#="H")

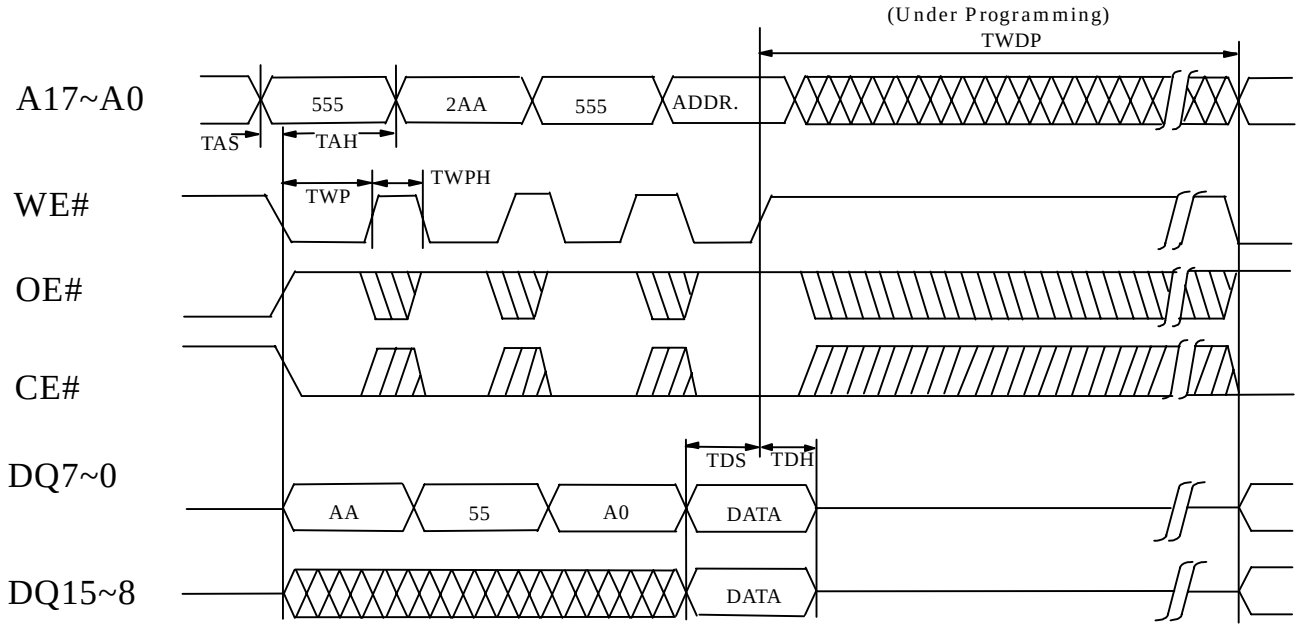


Figure 21: Write Protect / Unprotect Sequence (Byte Mode: BYTE#="L")

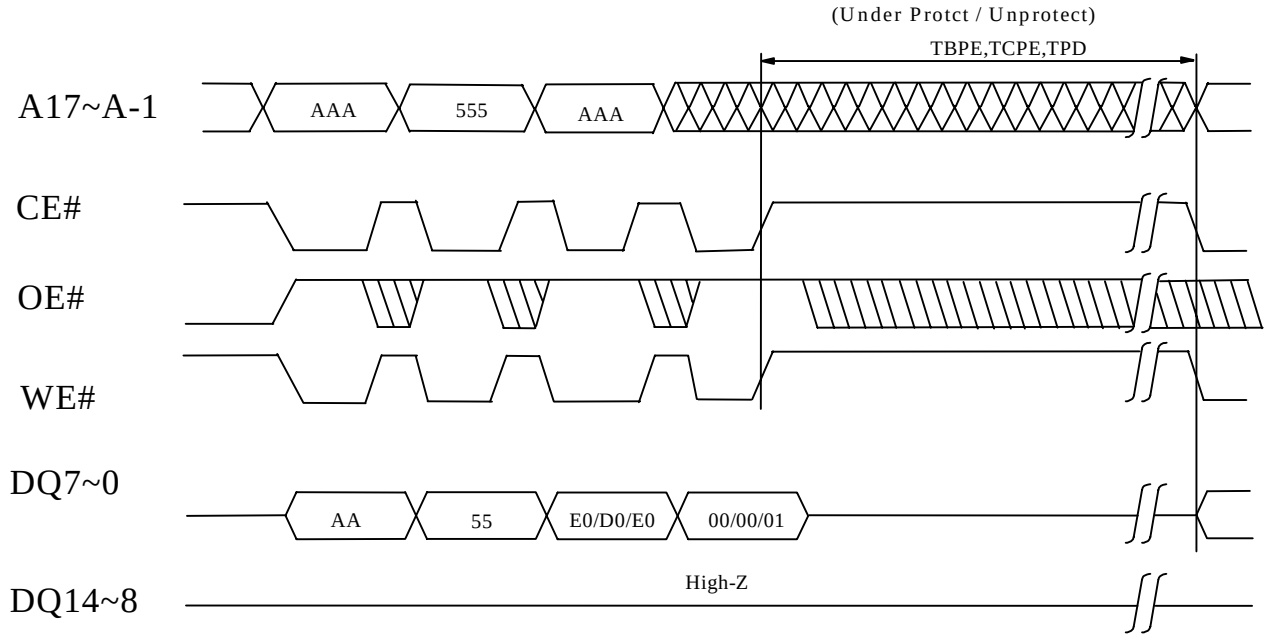


Figure 22: Write Protect / Unprotect Sequence (Word Mode: BYTE#="H")

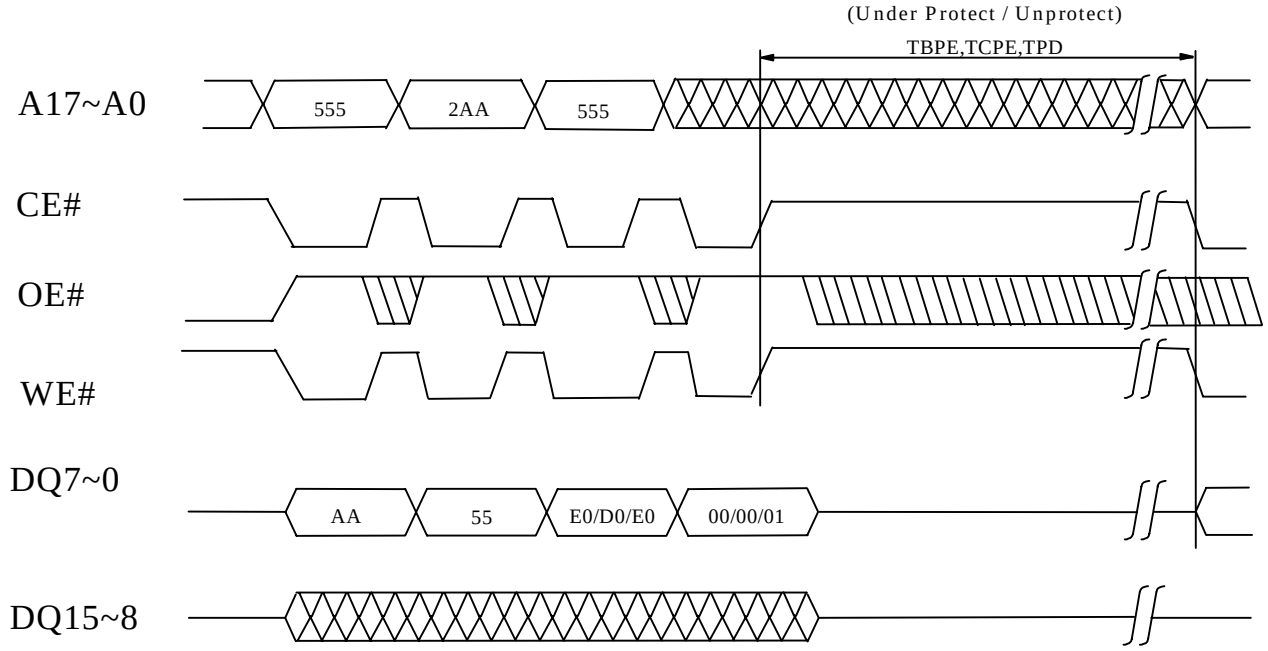


Figure 23: Software ID / Protect Verify Sequence (Byte Mode: BYTE#="L")

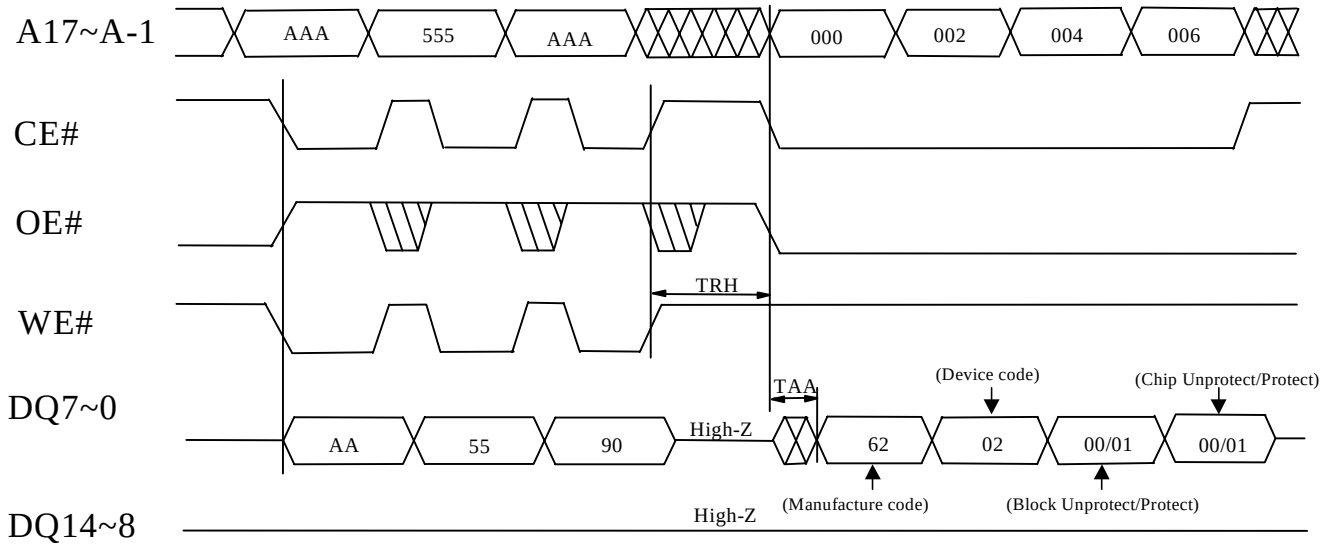


Figure 24: Software ID / Protect Verify Sequence (Word Mode: BYTE#="H")

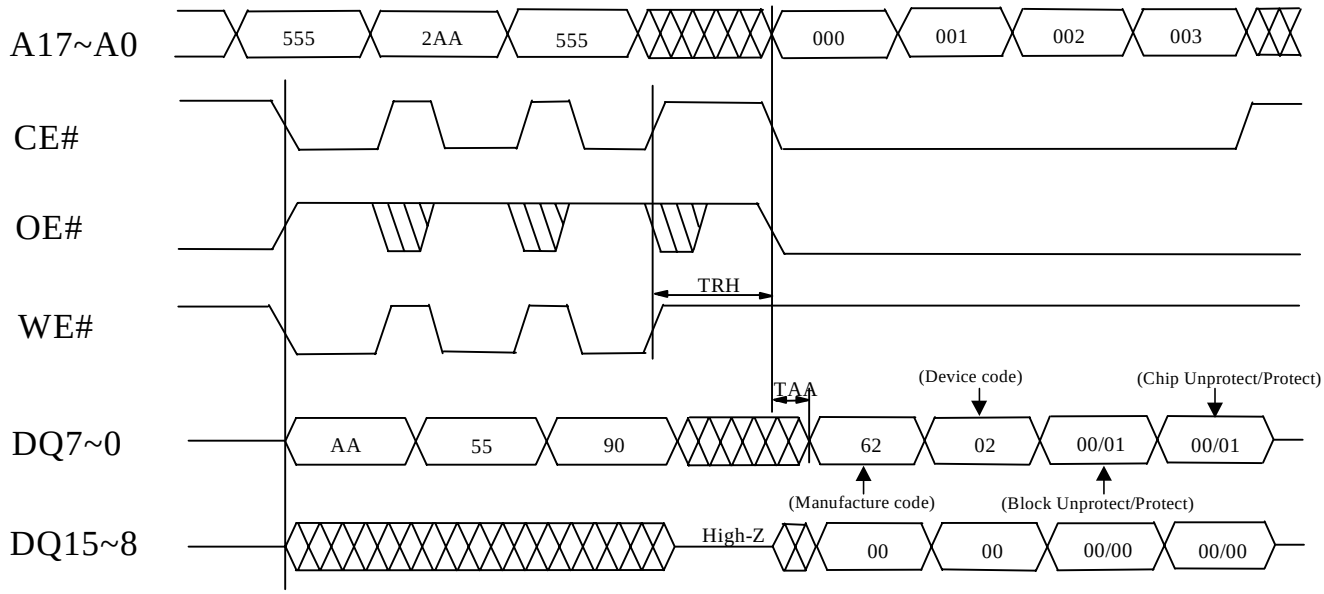
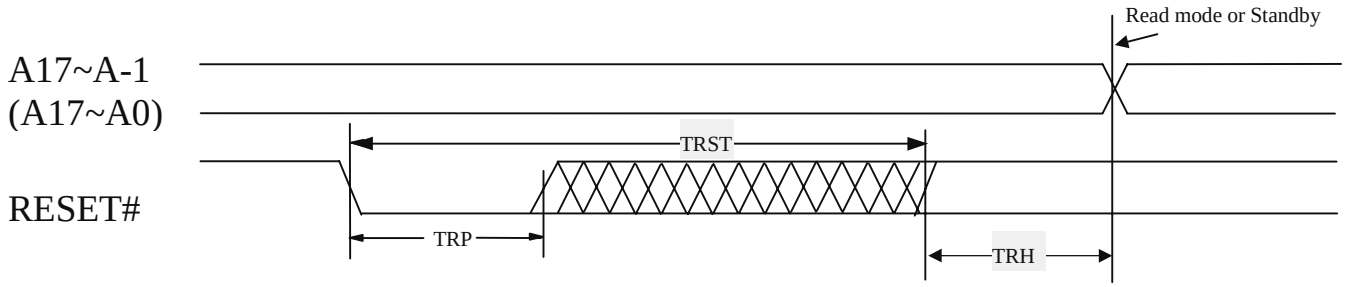


Figure 25: Hardware Reset Timing



Note: Device is in standby mode when RESET# is "L"

Figure 26: RD/BY# Timing(Write to Read)

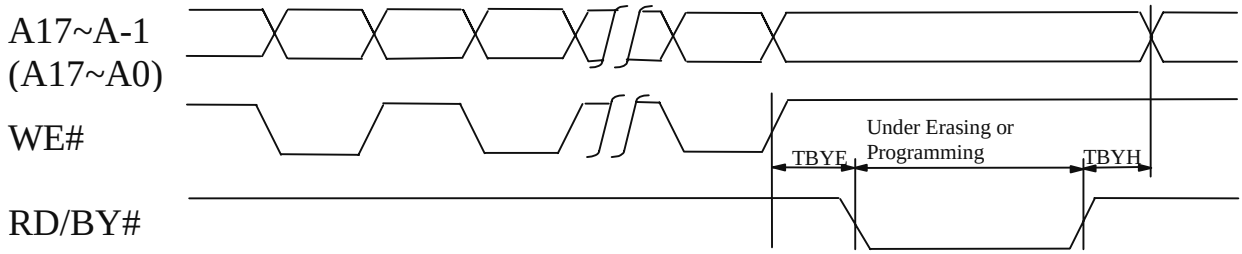


Figure 27: RD/BY# Timing(Write to Write)

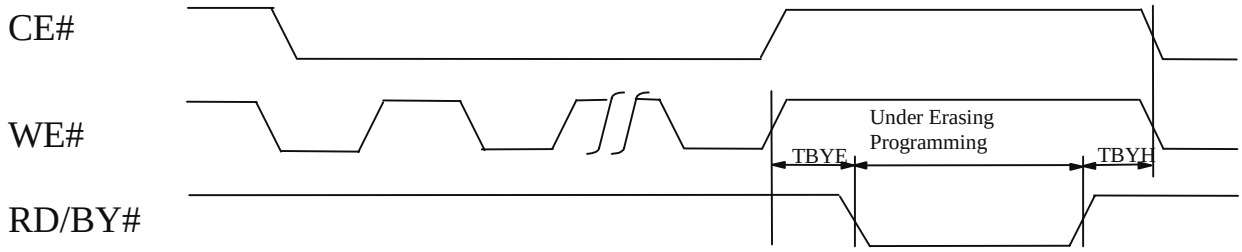


Figure 28: DATA# Polling Timing(DQ7)

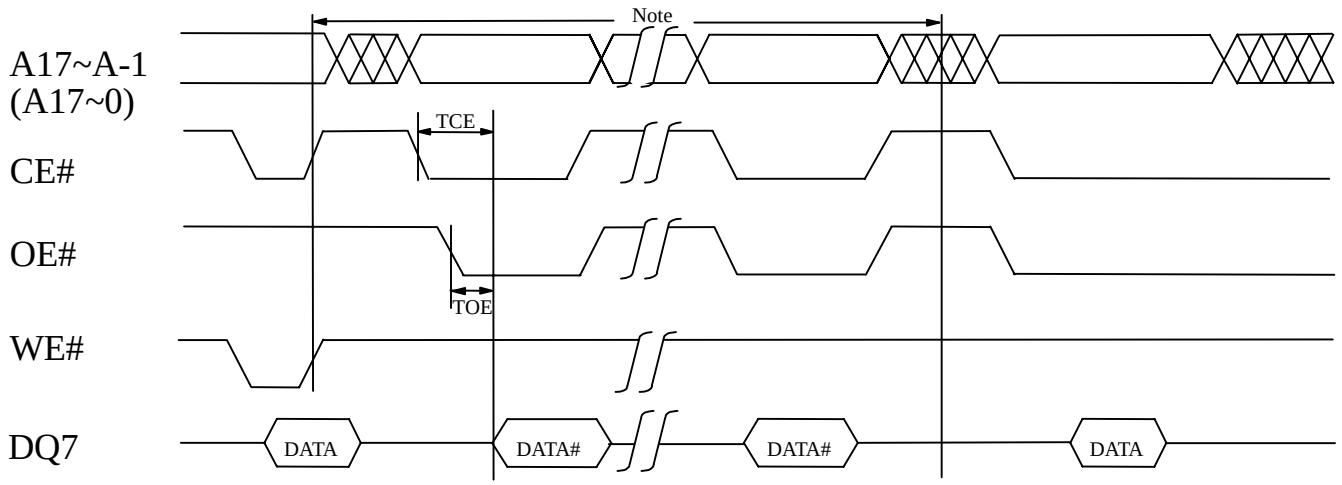
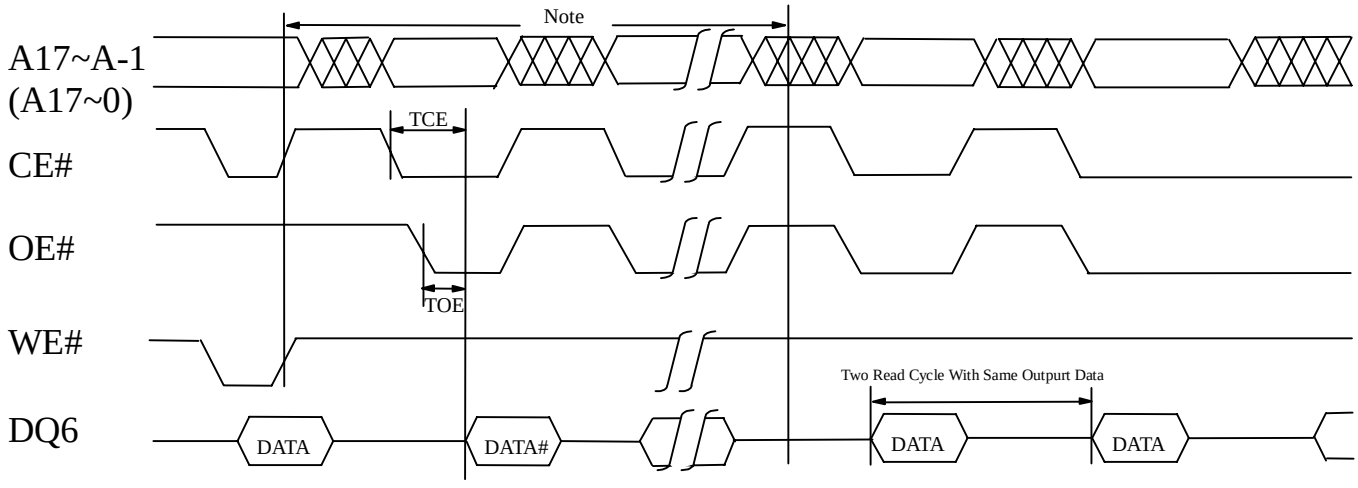


Figure 29: Toggle Bit Timing(DQ6)



Note: This time interval signal can be TBP, TWDP, TSE, TBKE, TCPE depending upon the selected operation mode.

Flowchart

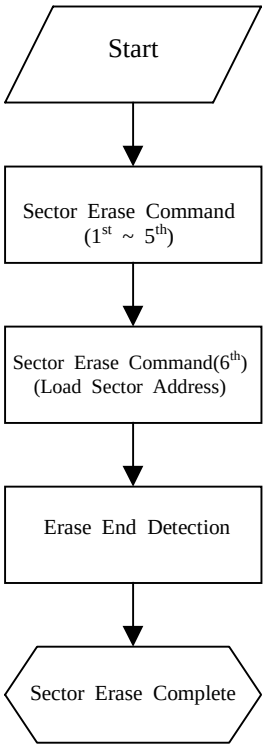


Figure 30: Sector Erase Flowchart

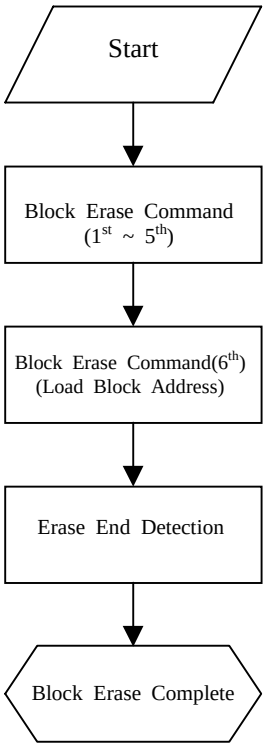


Figure 31: Block Erase Flowchart

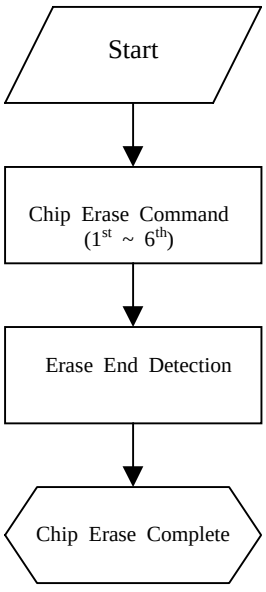


Figure 32: Chip Erase Flowchart

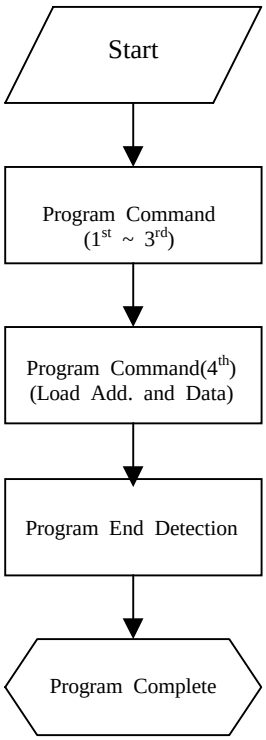


Figure 33: Byte/Word Program Flowchart

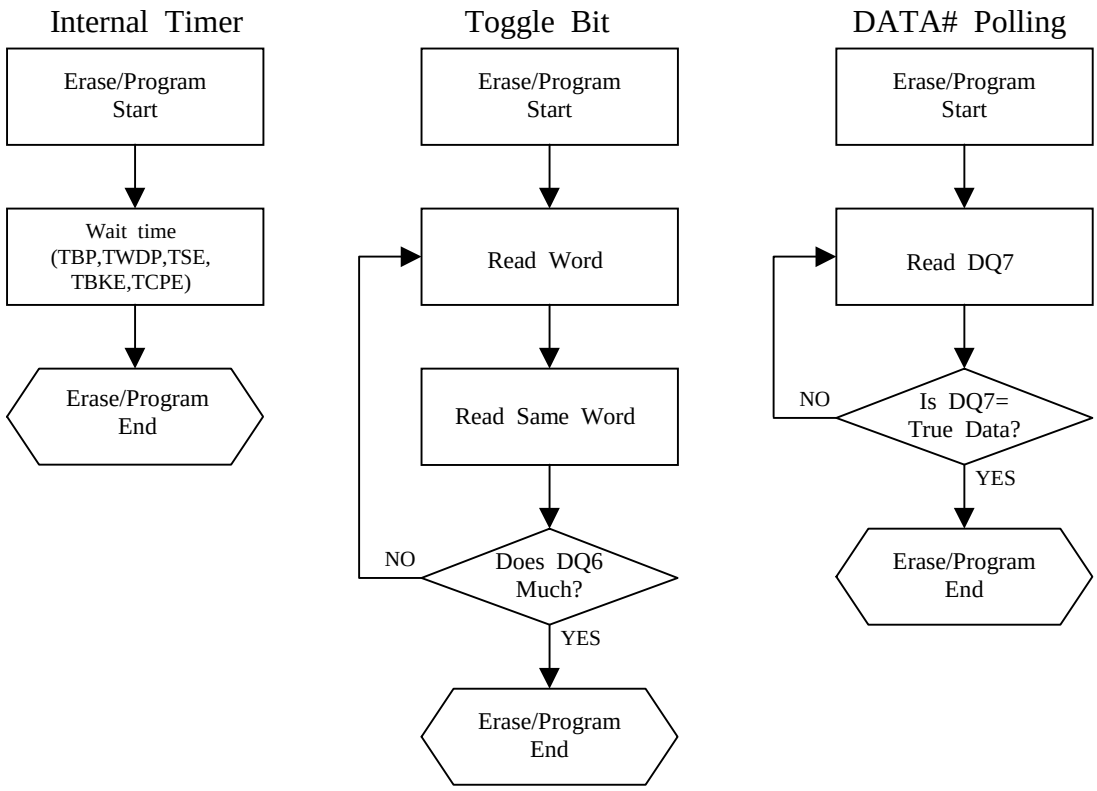


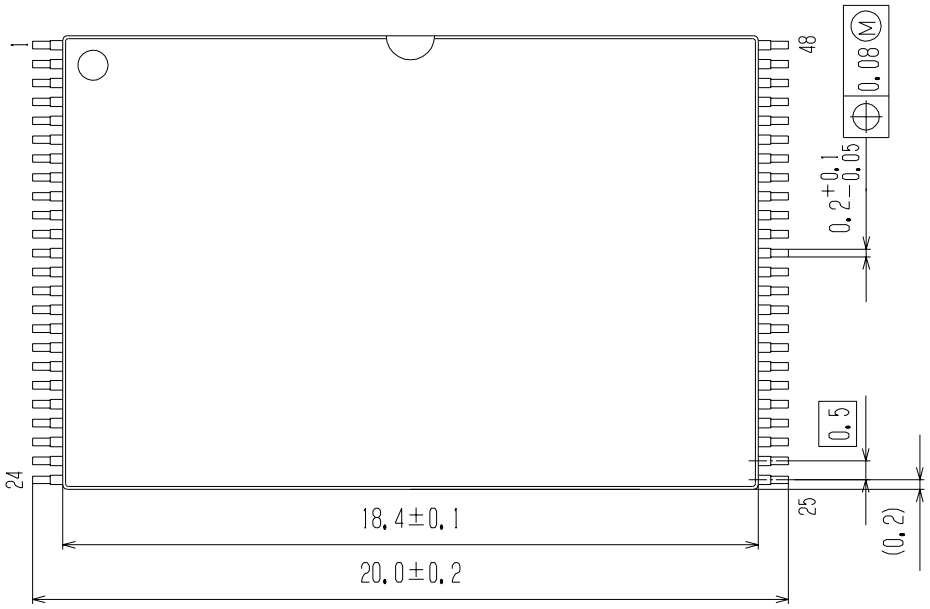
Figure 34: Erase/Program End Detection Flowchart

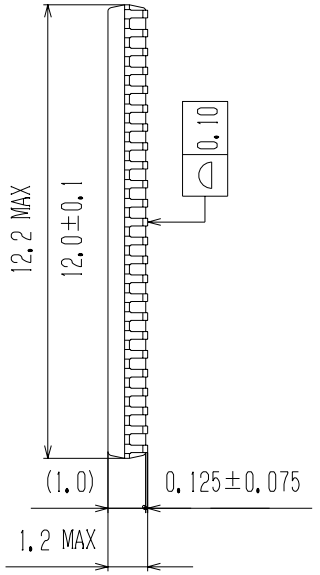
OUTLINE DRAWING

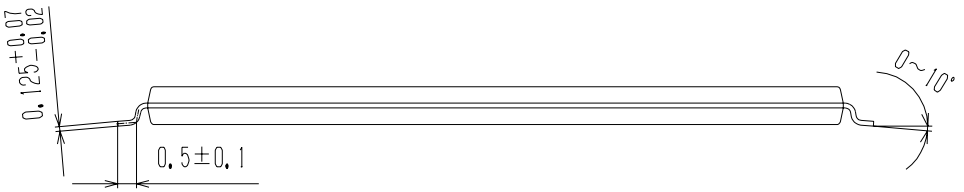
SANYO

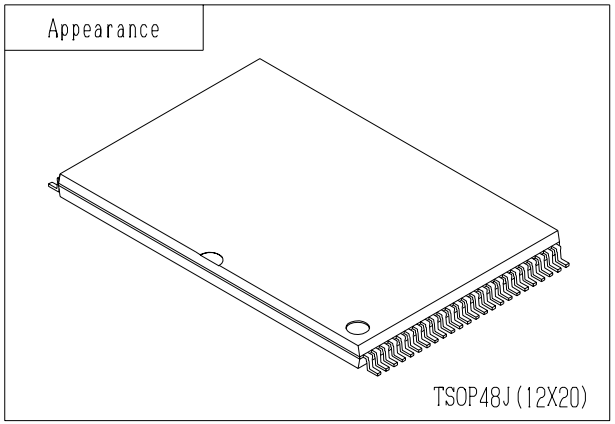
SANYO Package Code	EIAJ Package Code	JEDEC Package Code	TYPE NUMBER	ENACT No.	Mass(g)
TSOP48J(12X20)	———	———	———	S−251	0.55

Measure	Unit
5/1	mm









REVISION : 1

SANYO : Thin Small Outline Package 48Pin Plastic

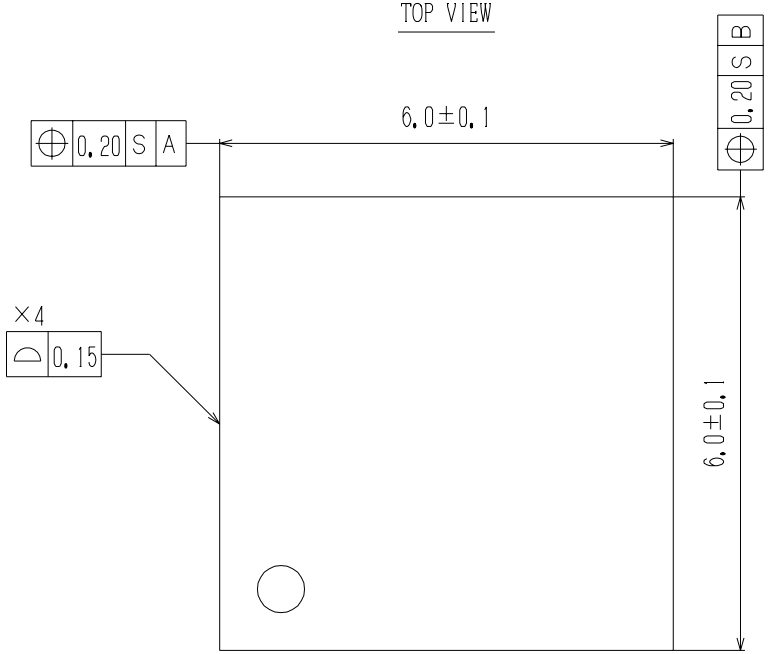
OUTLINE DRAWING

SANYO

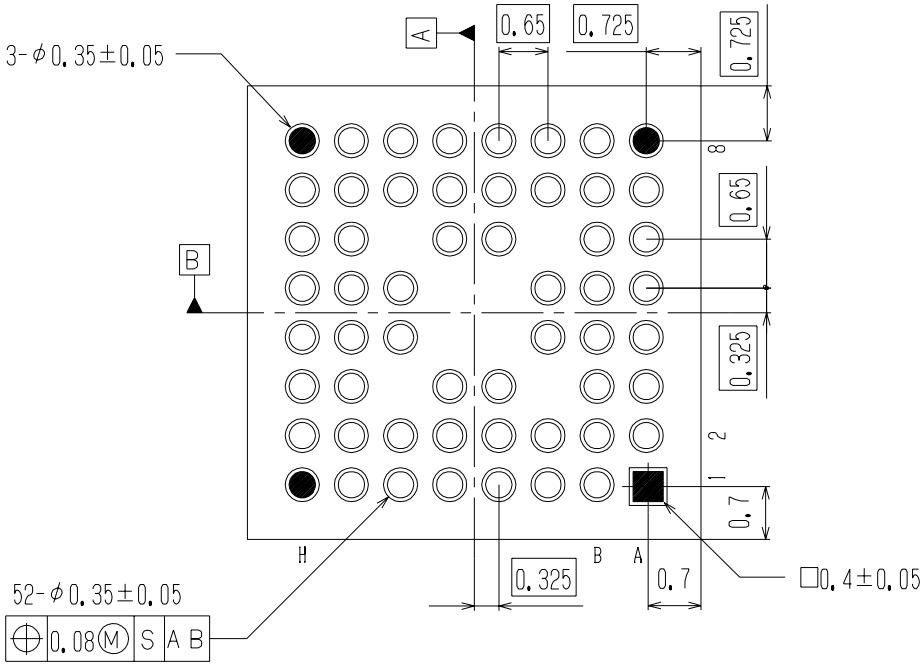
SANYO Package Code	EIAJ Package Code	JEDEC Package Code	TYPE NUMBER	ENACT No.	Mass(g)
FLGA52(6.0X6.0)	———	———	———	S−238	0.08

Measure	Unit
10/1	mm

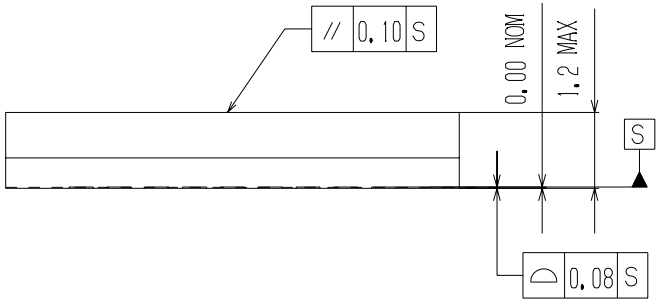
TOP VIEW



BOTTOM VIEW

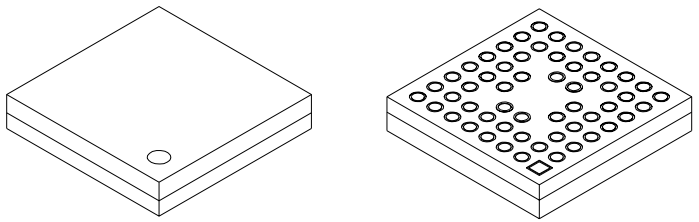


SIDE VIEW



Note : A1, A8 and H1, H8 are Dummy Land.

Appearance



FLGA52(6.0X6.0)

REVISION : 3

SANYO : Fine-pitch Land Grid Array Package 52pin Plastic