

## 8-BIT SINGLE-CHIP MICROCONTROLLER

## ★ DESCRIPTION

The  $\mu$ PD78011FY, 78012FY, 78013FY, 78014FY, 78015FY, 78016FY, and 78018FY are the products in the  $\mu$ PD78018FY subseries within the 78K/0 series, and the products which is added the I<sup>2</sup>C bus control function to the  $\mu$ PD78018F subseries.

A one-time PROM or EPROM product  $\mu$ PD78P018FY capable of operating in the same power supply voltage as of the mask ROM product and other development tools are also provided.

Functions are described in detail in the following User's Manual, which should be read when carrying out design work.

$\mu$ PD78018F, 78018FY Subseries User's Manual : U10659E  
78K/0 Series Users Manual – Instruction : U12326E

## FEATURES

- Serial interface : 2 channels (I<sup>2</sup>C bus mode : 1 channel)
- Large on-chip ROM & RAM

Item Product Name	Program Memory (ROM)	Data Memory			Package
		Internal High-Speed RAM	Internal Expanded RAM	Buffer RAM	
$\mu$ PD78011FY	8K bytes	512 bytes	–	32 bytes	<ul style="list-style-type: none"> <li>• 64-pin plastic shrink DIP (750 mil)</li> <li>• 64-pin plastic QFP (14 × 14 mm)</li> </ul>
$\mu$ PD78012FY	16K bytes				
$\mu$ PD78013FY	24K bytes	1024 bytes	512 bytes		
$\mu$ PD78014FY	32K bytes				
$\mu$ PD78015FY	40K bytes				
$\mu$ PD78016FY	48K bytes				
★ $\mu$ PD78018FY	60K bytes	1024 bytes			

- External memory expansion space : 64K bytes
- Minimum instruction execution time can be varied from high-speed (0.4  $\mu$ s) to ultra-low-speed (122  $\mu$ s)
- I/O ports: 53 (N-ch open-drain : 4)
- 8-bit resolution A/D converter : 8 channels
- Timer : 5 channels
- Supply voltage : V<sub>DD</sub> = 1.8 to 5.5 V

## APPLICATION FIELDS

Cellular phone, pager, VCR, audio, camera, home appliances, etc

The information in this document is subject to change without notice.

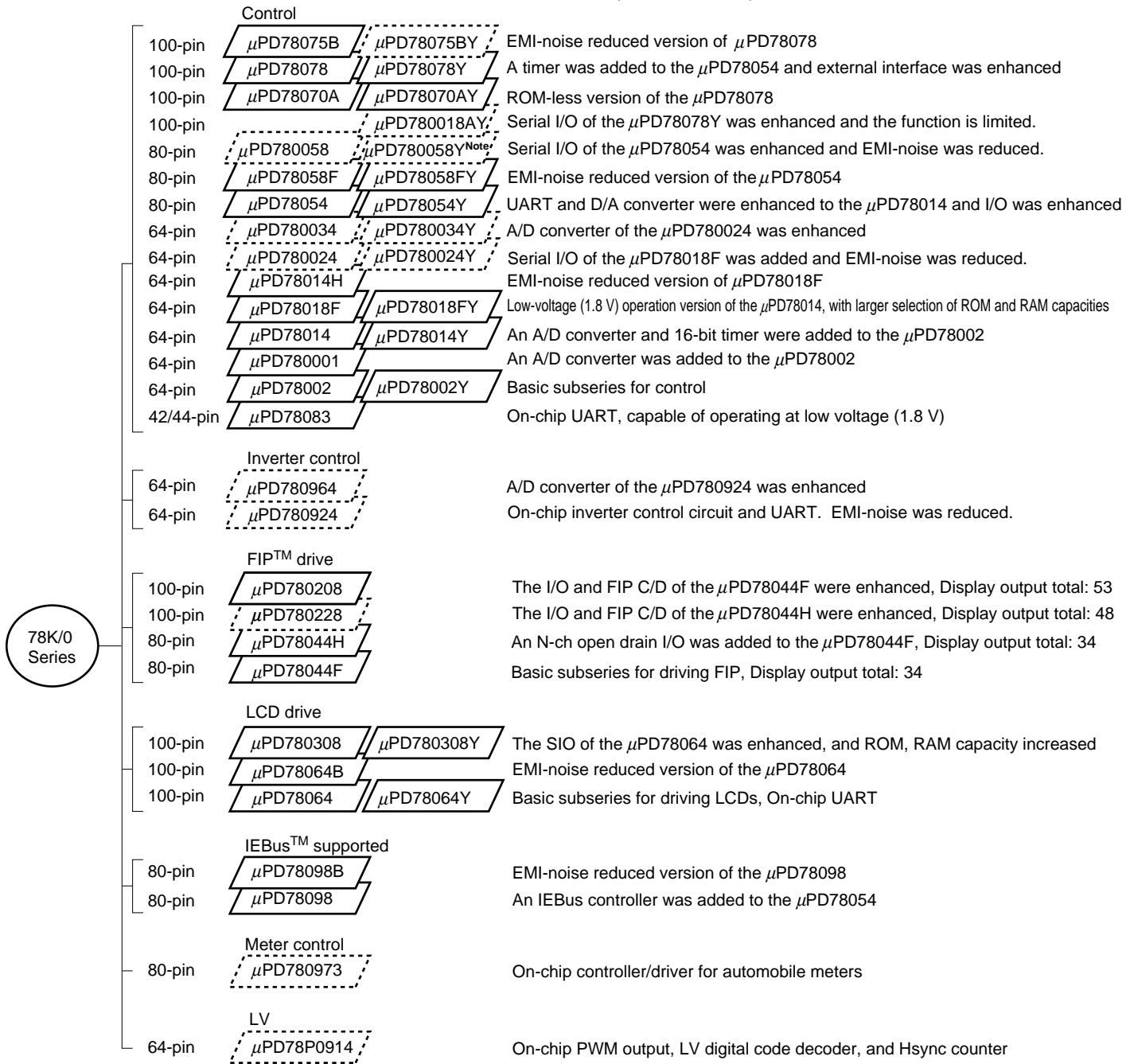
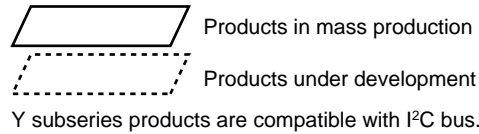
## ORDERING INFORMATION

Part Number	Package
$\mu$ PD78011FYCW-xxx	64-pin plastic shrink DIP (750 mil)
$\mu$ PD78011FYGC-xxx-AB8	64-pin plastic QFP (14 × 14 mm)
$\mu$ PD78012FYCW-xxx	64-pin plastic shrink DIP (750 mil)
$\mu$ PD78012FYGC-xxx-AB8	64-pin plastic QFP (14 × 14 mm)
$\mu$ PD78013FYCW-xxx	64-pin plastic shrink DIP (750 mil)
$\mu$ PD78013FYGC-xxx-AB8	64-pin plastic QFP (14 × 14 mm)
$\mu$ PD78014FYCW-xxx	64-pin plastic shrink DIP (750 mil)
$\mu$ PD78014FYGC-xxx-AB8	64-pin plastic QFP (14 × 14 mm)
$\mu$ PD78015FYCW-xxx	64-pin plastic shrink DIP (750 mil)
$\mu$ PD78015FYGC-xxx-AB8	64-pin plastic QFP (14 × 14 mm)
$\mu$ PD78016FYCW-xxx	64-pin plastic shrink DIP (750 mil)
$\mu$ PD78016FYGC-xxx-AB8	64-pin plastic QFP (14 × 14 mm)
★ $\mu$ PD78018FYCW-xxx	64-pin plastic shrink DIP (750 mil)
★ $\mu$ PD78018FYGC-xxx-AB8	64-pin plastic QFP (14 × 14 mm)

**Remark** xxx indicates a ROM code suffix.

★ 78K/0 SERIES DEVELOPMENT

The following shows the products organized according to usage. The names in the parallelograms are subseries names.



Note Under planning

The following lists the main functional differences between Y subseries products.

Functions		ROM Capacity	Serial Interface Configuration	I/O	V <sub>DD</sub> MIN. Value
Subseries Name					
Control	μPD78075BY	32 K to 40 K	3-wire/2-wire/I <sup>2</sup> C : 1 ch	88	1.8 V
	μPD78078Y	48 K to 60 K	With automatic transmit/receive function, 3-wire : 1 ch		
	μPD78070AY	–	3-wire/UART : 1 ch	61	2.7 V
	μPD780018AY	48 K to 60 K	With automatic transmit/receive function, 3-wire : 1 ch Time division, 3-wire : 1 ch I <sup>2</sup> C bus (for multimaster) : 1 ch	88	
	μPD780058Y	24 K to 60 K	3-wire/2-wire/I <sup>2</sup> C : 1 ch With automatic transmit/receive function, 3-wire : 1 ch 3-wire/time division UART : 1 ch	68	1.8 V
	μPD78058FY	48 K to 60 K	3-wire/2-wire/I <sup>2</sup> C : 1 ch	69	2.7 V
	μPD78054Y	16 K to 60 K	With automatic transmit/receive function, 3-wire : 1 ch 3-wire/UART : 1 ch		
	μPD780034Y	8 K to 32 K	UART : 1 ch	51	1.8 V
	μPD780024Y		3-wire : 1 ch I <sup>2</sup> C bus (for multimaster) : 1 ch		
	μPD78018FY	8 K to 60 K	3-wire/2-wire/I <sup>2</sup> C : 1 ch With automatic transmit/receive function, 3-wire : 1 ch	53	2.7 V
	μPD78014Y	8 K to 32 K	3-wire/2-wire/SBI/I <sup>2</sup> C : 1 ch With automatic transmit/receive function, 3-wire : 1 ch		
	μPD78002Y	8 K to 16 K	3-wire/2-wire/SBI/I <sup>2</sup> C : 1 ch		
LCD drive	μPD780308Y	48 K to 60 K	3-wire/2-wire/I <sup>2</sup> C : 1 ch 3-wire/time division UART : 1 ch 3-wire : 1 ch	57	2.0 V
	μPD78064Y	16 K to 32 K	3-wire/2-wire/I <sup>2</sup> C : 1 ch 3-wire/UART : 1 ch		

**Remark** The functions other than the serial interface are the same as those of subseries products without the suffix Y.

**OVERVIEW OF FUNCTION (1/2)**

★

Item		μPD78011FY	μPD78012FY	μPD78013FY	μPD78014FY	μPD78015FY	μPD78016FY	μPD78018FY
Product Name								
Internal memory	ROM	8K bytes	16K bytes	24K bytes	32K bytes	40K bytes	48K bytes	60 K bytes
	High-speed RAM	512 bytes			1024 bytes			
	Expanded RAM	—					512 bytes	1024 bytes
	Buffer RAM	32 bytes						
Memory space		64K bytes						
General-purpose registers		8 bits × 32 registers (8 bits × 8 registers × 4 banks)						
Minimum instruction execution time		On-chip minimum instruction execution time cycle modification function						
	When main system clock selected	0.4 μs/0.8 μs/1.6 μs/3.2 μs/6.4 μs (at 10.0 MHz operation)						
	When subsystem clock selected	122 μs (at 32.768 kHz operation)						
Instruction set		<ul style="list-style-type: none"> <li>• 16-bit operation</li> <li>• Multiplication/division (8 bits × 8 bits, 16 bits ÷ 8 bits)</li> <li>• Bit manipulation (set, reset, test, boolean operation)</li> <li>• BCD correction, etc.</li> </ul>						
I/O ports		Total : 53 <ul style="list-style-type: none"> <li>• CMOS input : 2</li> <li>• CMOS I/O : 47</li> <li>• N-channel open-drain I/O (15 V withstand voltage) : 4</li> </ul>						
A/D converter		<ul style="list-style-type: none"> <li>• 8-bit resolution × 8 channels</li> <li>• Operable over a wide power supply voltage range: V<sub>DD</sub> = 1.8 to 5.5 V</li> </ul>						
Serial interface		<ul style="list-style-type: none"> <li>• 3-wire serial I/O/2-wire serial I/O/I<sup>2</sup>C bus mode selectable: 1 channel</li> <li>• 3-wire mode (on-chip max. 32 bytes automatic data transmit/receive function): 1 channel</li> </ul>						
Timer		<ul style="list-style-type: none"> <li>• 16-bit timer/event counter : 1 channel</li> <li>• 8-bit timer/event counter : 2 channels</li> <li>• Watch timer : 1 channel</li> <li>• Watchdog timer : 1 channel</li> </ul>						
Timer output		3 (14-bit PWM output × 1)						
Clock output		39.1 kHz, 78.1 kHz, 156 kHz, 313 kHz, 625 kHz, 1.25 MHz (at main system clock: 10.0 MHz operation), 32.768 kHz (at subsystem clock: 32.768 kHz operation)						
Buzzer output		2.4 kHz, 4.9 kHz, 9.8 kHz (at main system clock: 10.0 MHz operation)						
Vectored interrupt sources	Maskable	Internal : 8 External : 4						
	Non-maskable	Internal : 1						
	Software	1						

**OVERVIEW OF FUNCTION (2/2)**

Item	μPD78011FY	μPD78012FY	μPD78013FY	μPD78014FY	μPD78015FY	μPD78016FY	μPD78018FY
Product Name							
Test input	Internal : 1 External : 1						
Supply voltage	V <sub>DD</sub> = 1.8 to 5.5 V						
Operating ambient temperature	T <sub>A</sub> = -40 to +85°C						
Package	<ul style="list-style-type: none"> <li>• 64-pin plastic shrink DIP (750 mil)</li> <li>• 64-pin plastic QFP (14 × 14 mm)</li> </ul>						

**TABLE OF CONTENTS**

1. PIN CONFIGURATION (TOP VIEW) ..... 8

2. BLOCK DIAGRAM ..... 11

3. PIN FUNCTIONS ..... 12

    3.1 PORT PINS ..... 12

    3.2 PINS OTHER THAN PORT PINS ..... 13

    3.3 PIN I/O CIRCUITS AND RECOMMENDED CONNECTION OF UNUSED PINS ..... 15

4. MEMORY SPACE ..... 17

5. PERIPHERAL HARDWARE FUNCTION FEATURES ..... 19

    5.1 PORTS ..... 19

    5.2 CLOCK GENERATOR ..... 20

    5.3 TIMER/EVENT COUNTER ..... 21

    5.4 CLOCK OUTPUT CONTROL CIRCUIT ..... 23

    5.5 BUZZER OUTPUT CONTROL CIRCUIT ..... 23

    5.6 A/D CONVERTER ..... 24

    5.7 SERIAL INTERFACES ..... 24

6. INTERRUPT FUNCTIONS AND TEST FUNCTIONS ..... 26

    6.1 INTERRUPT FUNCTIONS ..... 26

    6.2 TEST FUNCTIONS ..... 29

7. EXTERNAL DEVICE EXPANSION FUNCTIONS ..... 30

8. STANDBY FUNCTIONS ..... 30

9. RESET FUNCTIONS ..... 30

10. INSTRUCTION SET ..... 31

11. ELECTRICAL SPECIFICATIONS ..... 34

12. CHARACTERISTIC CURVE (REFERENCE VALUES) ..... 61

13. PACKAGE DRAWINGS ..... 62

14. RECOMMENDED SOLDERING CONDITIONS ..... 64

APPENDIX A. DEVELOPMENT TOOLS ..... 65

APPENDIX B. RELATED DOCUMENTS ..... 67

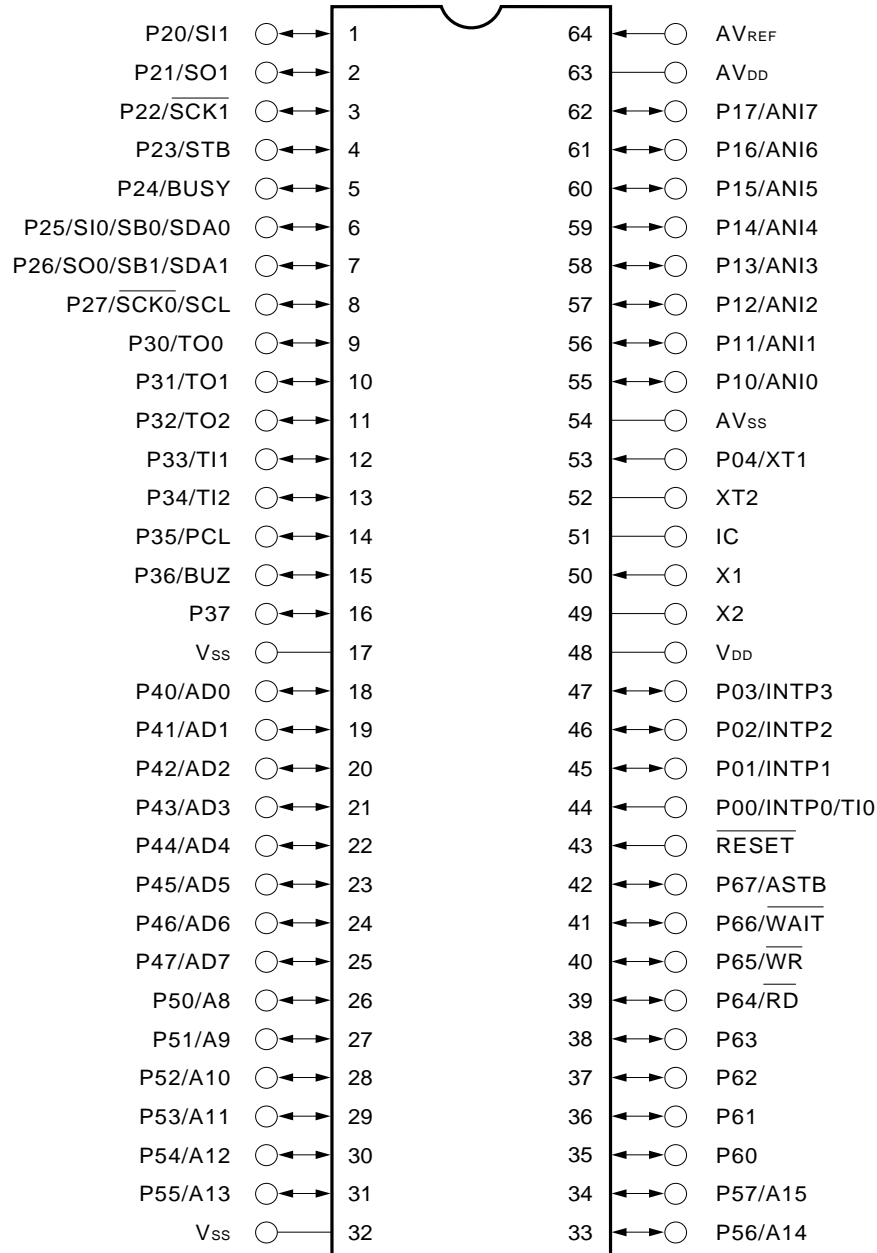
1. PIN CONFIGURATION (TOP VIEW)

• 64-Pin Plastic Shrink DIP (750 mil)

μPD78011FYCW-xxx, 78012FYCW-xxx, 78013FYCW-xxx,

μPD78014FYCW-xxx, 78015FYCW-xxx, 78016FYCW-xxx,

★ μPD78018FYCW-xxx



- Cautions**
1. Always connect the IC (Internally Connected) pin to VSS directly.
  2. Always connect the AVDD pin to VDD.
  3. Always connect the AVSS pin to VSS.

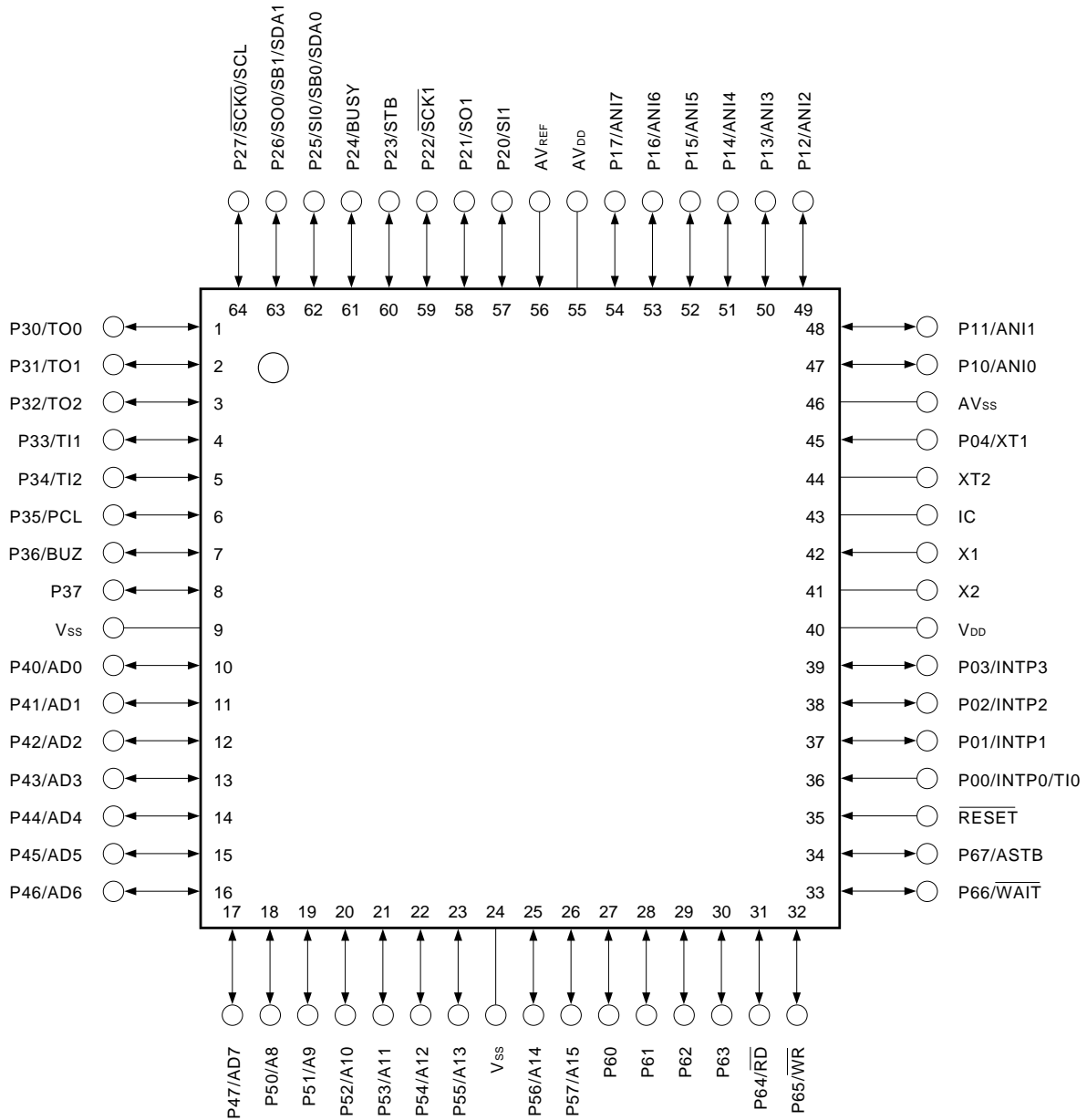


• 64-Pin Plastic QFP (14 × 14 mm)

μPD78011FYGC-xxx-AB8, 78012FYGC-xxx-AB8, 78013FYGC-xxx-AB8,

μPD78014FYGC-xxx-AB8, 78015FYGC-xxx-AB8, 78016FYGC-xxx-AB8,

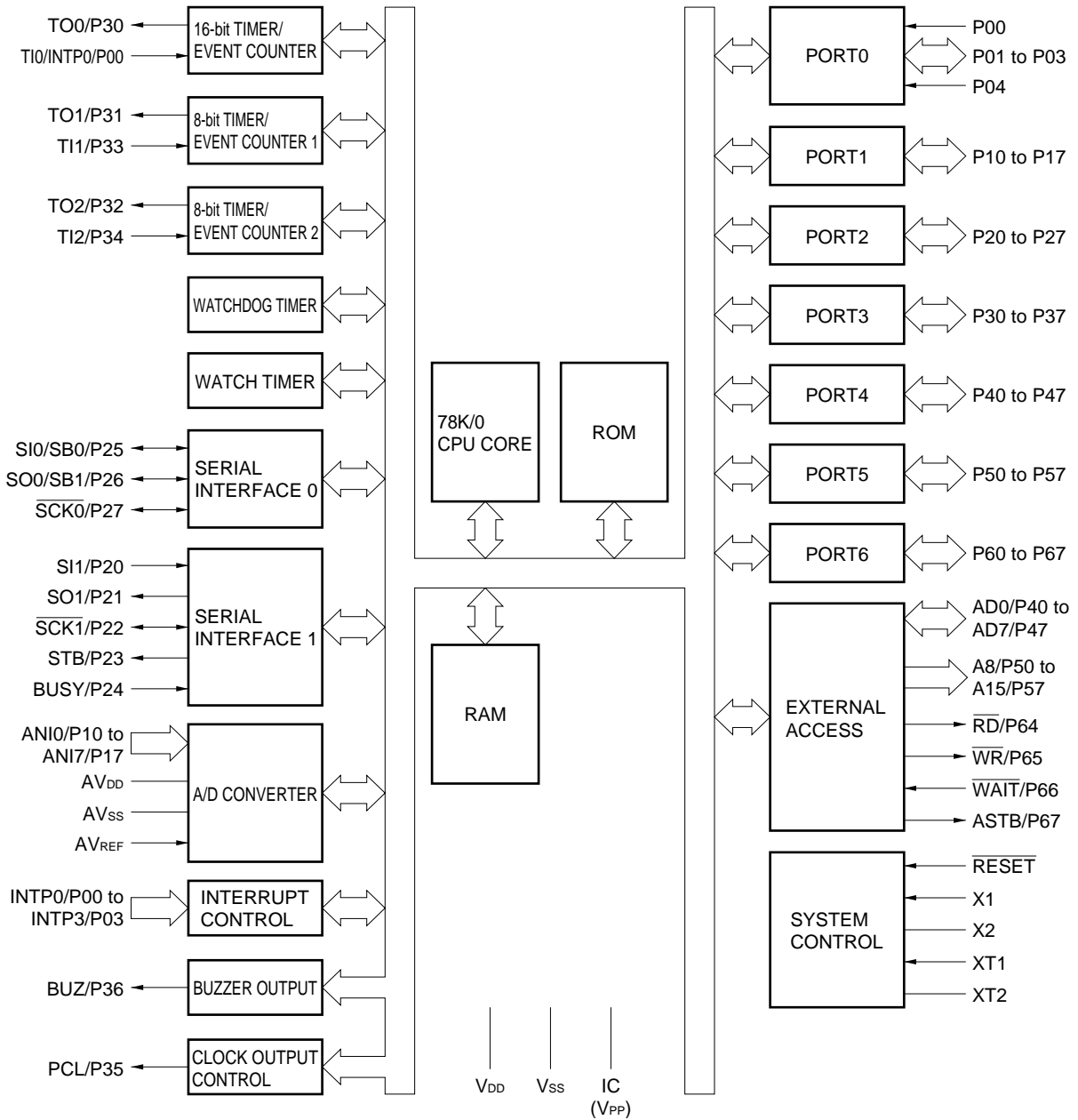
★ μPD78018FYGC-xxx-AB8



- Cautions**
1. Always connect the IC (Internally Connected) pin to V<sub>SS</sub> directly.
  2. Always connect the AV<sub>DD</sub> pin to V<sub>DD</sub>.
  3. Always connect the AV<sub>SS</sub> pin to V<sub>SS</sub>.

A8 to A15	: Address Bus	PCL	: Programmable Clock
AD0 to AD7	: Address/Data Bus	$\overline{RD}$	: Read Strobe
ANI0 to ANI7	: Analog Input	$\overline{RESET}$	: Reset
ASTB	: Address Strobe	SB0, SB1	: Serial Bus
AV <sub>DD</sub>	: Analog Power Supply	$\overline{SCK0}$ , $\overline{SCK1}$	: Serial Clock
AV <sub>REF</sub>	: Analog Reference Voltage	SCL	: Serial Clock
AV <sub>SS</sub>	: Analog Ground	SDA0, SDA1	: Serial Data
BUSY	: Busy	SI0, SI1	: Serial Input
BUZ	: Buzzer Clock	SO0, SO1	: Serial Output
IC	: Internally Connected	STB	: Strobe
INTP0 to INTP3	: Interrupt from Peripherals	TI0 to TI2	: Timer Input
P00 to P04	: Port0	TO0 to TO2	: Timer Output
P10 to P17	: Port1	V <sub>DD</sub>	: Power Supply
P20 to P27	: Port2	V <sub>SS</sub>	: Ground
P30 to P37	: Port3	$\overline{WAIT}$	: Wait
P40 to P47	: Port4	$\overline{WR}$	: Write Strobe
P50 to P57	: Port5	X1, X2	: Crystal (Main System Clock)
P60 to P67	: Port6	XT1, XT2	: Crystal (Subsystem Clock)

2. BLOCK DIAGRAM



- Remarks**
1. Internal ROM & RAM capacity varies depending on the product.
  2. ( ) : μPD78P018FY

### 3. PIN FUNCTIONS

#### 3.1 PORT PINS (1/2)

Pin Name	I/O	Function		On Reset	Dual-Function Pin
P00	Input	Port 0 5-bit I/O port	Input only	Input	INTP0/TI0
P01	Input/ output		Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be used in software.	Input	INTP1
P02					INTP2
P03					INTP3
P04 <sup>Note 1</sup>	Input		Input only	Input	XT1
P10 to P17	Input/ output	Port 1 8-bit input/output port. Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be used in software. <sup>Note 2</sup>		Input	ANI0 to ANI7
P20	Input/ output	Port 2 8-bit input/output port. Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be used in software.	Input	S11	
P21				SO1	
P22				$\overline{\text{SCK1}}$	
P23				STB	
P24				BUSY	
P25				SI0/SB0/SDA0	
P26				SO0/SB1/SDA1	
P27				$\overline{\text{SCK0/SCL}}$	
P30	Input/ output	Port 3 8-bit input/output port. Input/output can be specified in 1-bit units. When used as an input port, on-chip pull-up resistor can be used in software.	Input	TO0	
P31				TO1	
P32				TO2	
P33				TI1	
P34				TI2	
P35				PCL	
P36				BUZ	
P37				—	
P40 to P47	Input/ output	Port 4 8-bit input/output port. Input/output can be specified in 8-bit unit. When used as an input port, on-chip pull-up resistor can be used in software. Test input flag (KRIF) is set to 1 by falling edge detection.		Input	AD0 to AD7

**Notes 1.** When using the P04/XT1 pins as an input port, set 1 to bit 6 (FRC) of the processor clock control register (PCC). Do not use the on-chip feedback register of the subsystem clock oscillator.

**2.** When using the P10/ANI0 to P17/ANI7 pins as the A/D converter analog input, on-chip pull-up resistor is automatically unused.

3.1 PORT PINS (2/2)

Pin Name	I/O	Function		On Reset	Dual-Function Pin
P50 to P57	Input/output	Port 5 8-bit input/output port. LED can be driven directly. Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be used in software.		Input	A8 to A15
P60	Input/output	Port 6 8-bit input/output port. Input/output can be specified bit-wise.	N-ch open-drain input/output port. On-chip pull-up resistor can be specified by mask option. LED can be driven directly.	Input	—
P61					
P62					
P63					
P64		When used as an input port, on-chip pull-up resistor can be used in software.	$\overline{RD}$		
P65			$\overline{WR}$		
P66			$\overline{WAIT}$		
P67			ASTB		

3.2 PINS OTHER THAN PORT PINS (1/2)

Pin Name	I/O	Function		On Reset	Dual-Function Pin
INTP0	Input	External interrupt request input by which the effective edge (rising edge, falling edge, or both rising edge and falling edge) can be specified.		Input	P00/TI0
INTP1					P01
INTP2		P02			
INTP3		Falling edge detection external interrupt request input.			P03
SI0	Input	Serial interface serial data input.		Input	P25/SB0/SDA0
SI1					P20
SO0	Output	Serial interface serial data output.		Input	P26/SB1/SDA1
SO1					P21
SB0	Input/output	Serial interface serial data input/output.		Input	P25/SI0/SDA0
SB1					P26/SO0/SDA1
SDA0					P25/SI0/SB0
SDA1					P26/SO0/SB1
$\overline{SCK0}$	Input/output	Serial interface serial clock input/output.		Input	P27/SCL
SCL					$P27/\overline{SCK0}$
SCK1					P22
STB	Output	Serial interface automatic transmit/receive strobe output.		Input	P23
BUSY	Input	Serial interface automatic transmit/receive busy input.		Input	P24

## 3.2 PINS OTHER THAN PORT PINS (2/2)

Pin Name	I/O	Function	On Reset	Dual-Function Pin
T10	Input	External count clock input to 16-bit timer (TM0).	Input	P00/INTP0
T11		External count clock input to 8-bit timer (TM1).		P33
T12		External count clock input to 8-bit timer (TM2).		P34
TO0	Output	16-bit timer (TM0) output (shared as 14-bit PWM output).	Input	P30
TO1		8-bit timer (TM1) output.		P31
TO2		8-bit timer (TM2) output.		P32
PCL	Output	Clock output (for main system clock, subsystem clock trimming).	Input	P35
BUZ	Output	Buzzer output.	Input	P36
AD0 to AD7	Input /output	Low-order address/data bus at external memory expansion.	Input	P40 to P47
A8 to A15	Output	High-order address bus at external memory expansion.	Input	P50 to P57
$\overline{RD}$	Output	External memory read operation strobe signal output.	Input	P64
$\overline{WR}$		External memory write operation strobe signal output.		P65
$\overline{WAIT}$	Input	Wait insertion at external memory access.	Input	P66
ASTB	Output	Strobe output which latches the address information output at port 4 and port 5 to access external memory.	Input	P67
ANI0 to ANI7	Input	A/D converter analog input.	Input	P10 to P17
AVREF	Input	A/D converter reference voltage input.	—	—
AVDD	—	A/D converter analog power supply. Connected to V <sub>DD</sub> .	—	—
AVSS	—	A/D converter ground potential. Connected to V <sub>SS</sub> .	—	—
$\overline{RESET}$	Input	System reset input.	—	—
X1	Input	Main system clock oscillation crystal connection.	—	—
X2	—		—	—
XT1	Input	Subsystem clock oscillation crystal connection.	Input	P04
XT2	—		—	—
V <sub>DD</sub>	—	Positive power supply.	—	—
V <sub>SS</sub>	—	Ground potential.	—	—
IC	—	Internal connection. Connected to V <sub>SS</sub> directly.	—	—

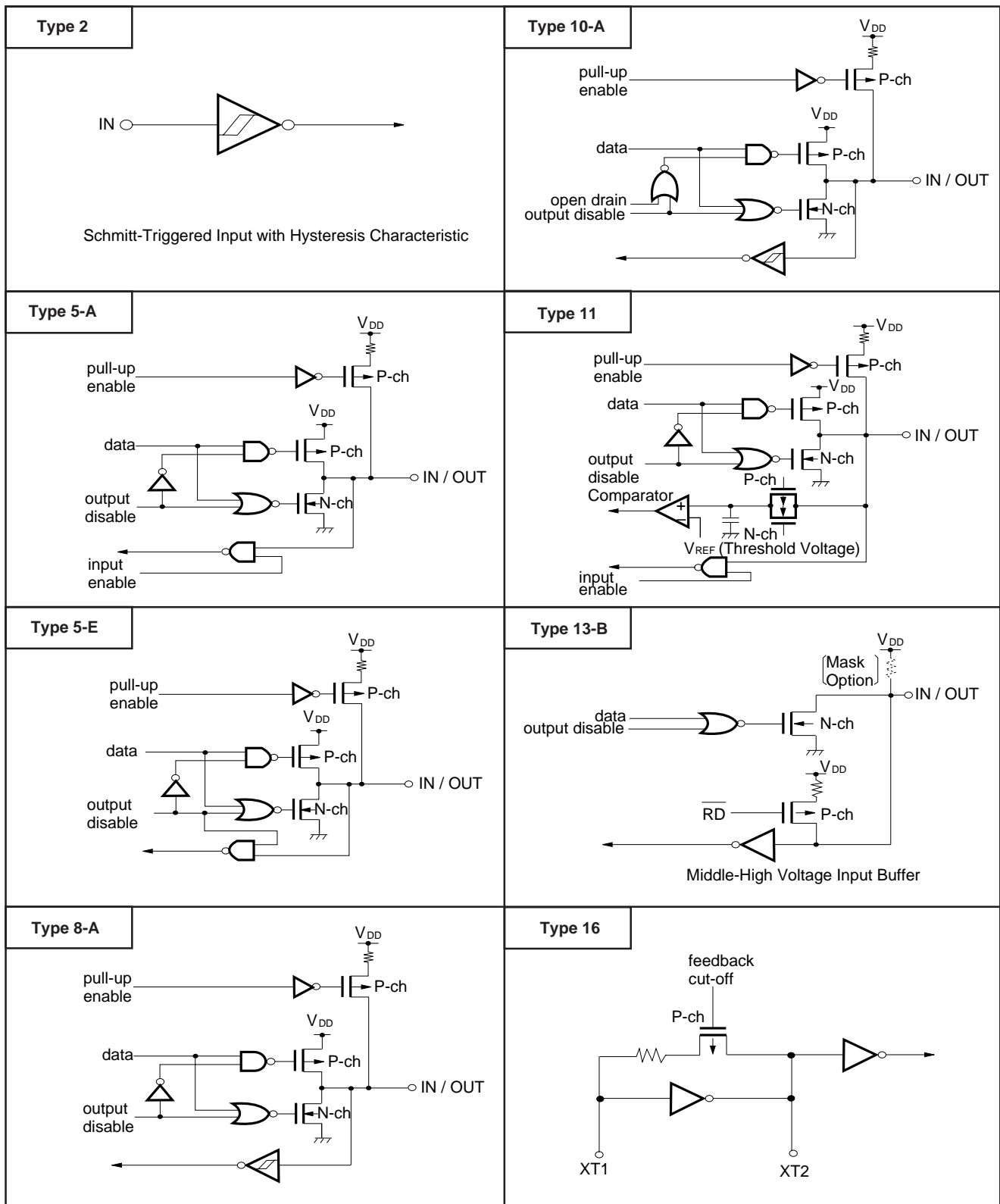
**3.3 PIN I/O CIRCUITS AND RECOMMENDED CONNECTION OF UNUSED PINS**

The input/output circuit type of each pin and recommended connection of unused pins are shown in Table 3-1. For the input/output circuit configuration of each type, refer to **Figure 3-1**.

**Table 3-1. Input/Output Circuit Type of Each Pin**

Pin Name	Input/output Circuit Type	I/O	Recommended Connection when Not Used	
P00/INTP0/TI0	2	Input	Connected to V <sub>SS</sub> .	
P01/INTP1	8-A	Input/output	Individually connected to V <sub>SS</sub> via resistor.	
P02/INTP2				
P03/INTP3				
P04/XT1	16	Input	Connected to V <sub>DD</sub> or V <sub>SS</sub> .	
P10/ANI0 to P17/ANI7	11	Input/output	Individually connected to V <sub>DD</sub> or V <sub>SS</sub> via resistor.	
P20/SI1	8-A			
P21/SO1	5-A			
P22/ $\overline{\text{SCK1}}$	8-A			
P23/STB	5-A			
P24/BUSY	8-A			
P25/SI0/SB0	10-A			
P26/SO0/SB1				
P27/ $\overline{\text{SCK0}}$				
P30/TO0	5-A			
P31/TO1				
P32/TO2				
P33/TI1	8-A			
P34/TI2				
P35/PCL	5-A			
P36/BUZ				
P37				
P40/AD0 to P47/AD7	5-E			Individually connected to V <sub>DD</sub> via resistor.
P50/A8 to P57/A15	5-A			Individually connected to V <sub>DD</sub> or V <sub>SS</sub> via resistor.
P60 to P63	13-B			Individually connected to V <sub>DD</sub> via resistor.
P64/ $\overline{\text{RD}}$	5-A			Individually connected to V <sub>DD</sub> or V <sub>SS</sub> via resistor.
P65/ $\overline{\text{WR}}$				
P66/ $\overline{\text{WAIT}}$				
P67/ASTB				
$\overline{\text{RESET}}$	2	Input	—	
XT2	16	—	Leave open.	
AV <sub>REF</sub>	—	—	Connected to V <sub>SS</sub> .	
AV <sub>DD</sub>			Connected to V <sub>DD</sub> .	
AV <sub>SS</sub>			Connected to V <sub>SS</sub> .	
IC			Connected to V <sub>SS</sub> directly.	

Figure 3-1. Pin Input/Output Circuits

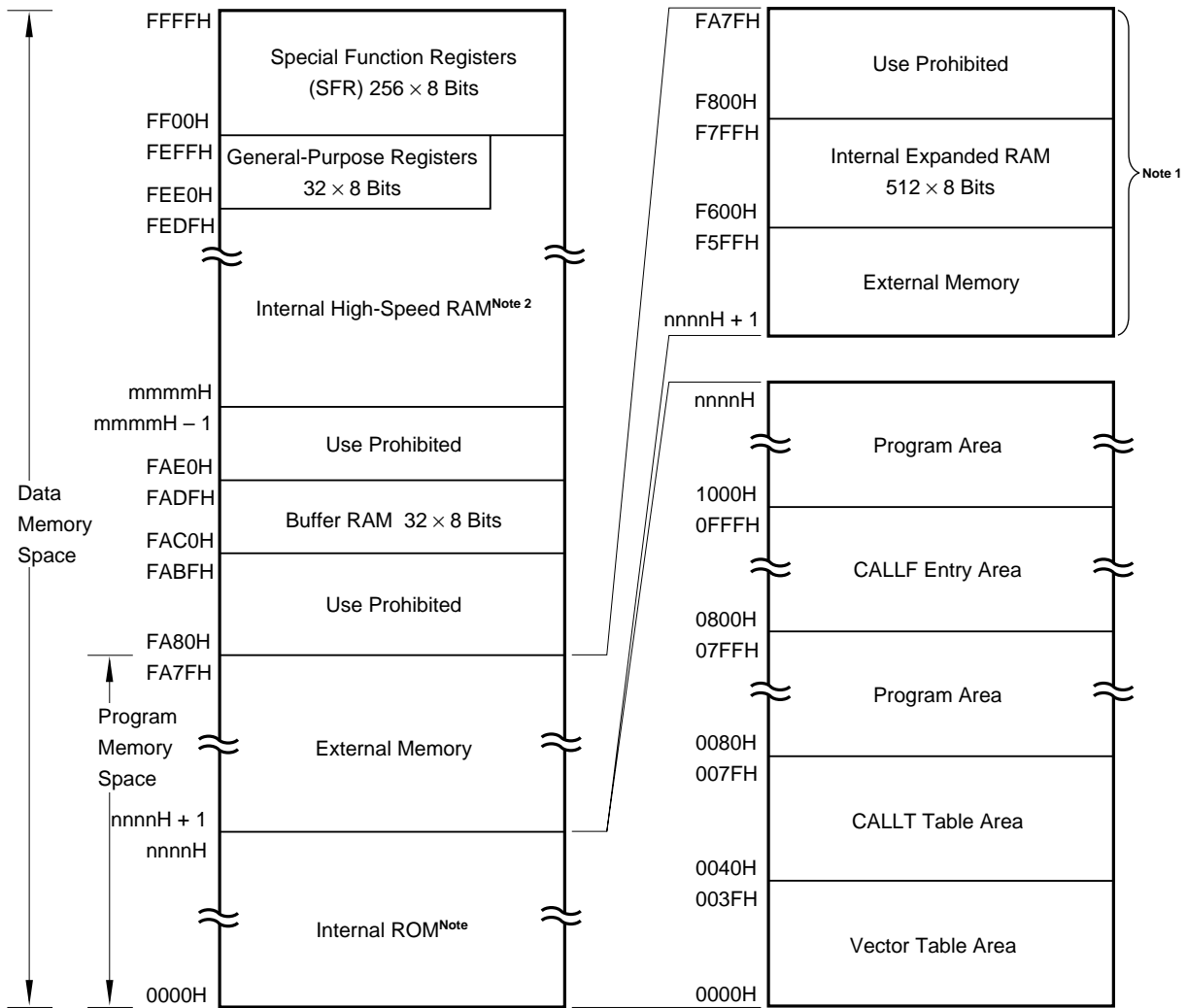




★ 4. MEMORY SPACE

The memory map of the μPD78011FY, 78012FY, 78013FY, 78014FY, 78015FY and 78016FY is shown in Figures 4-1 and 4-2.

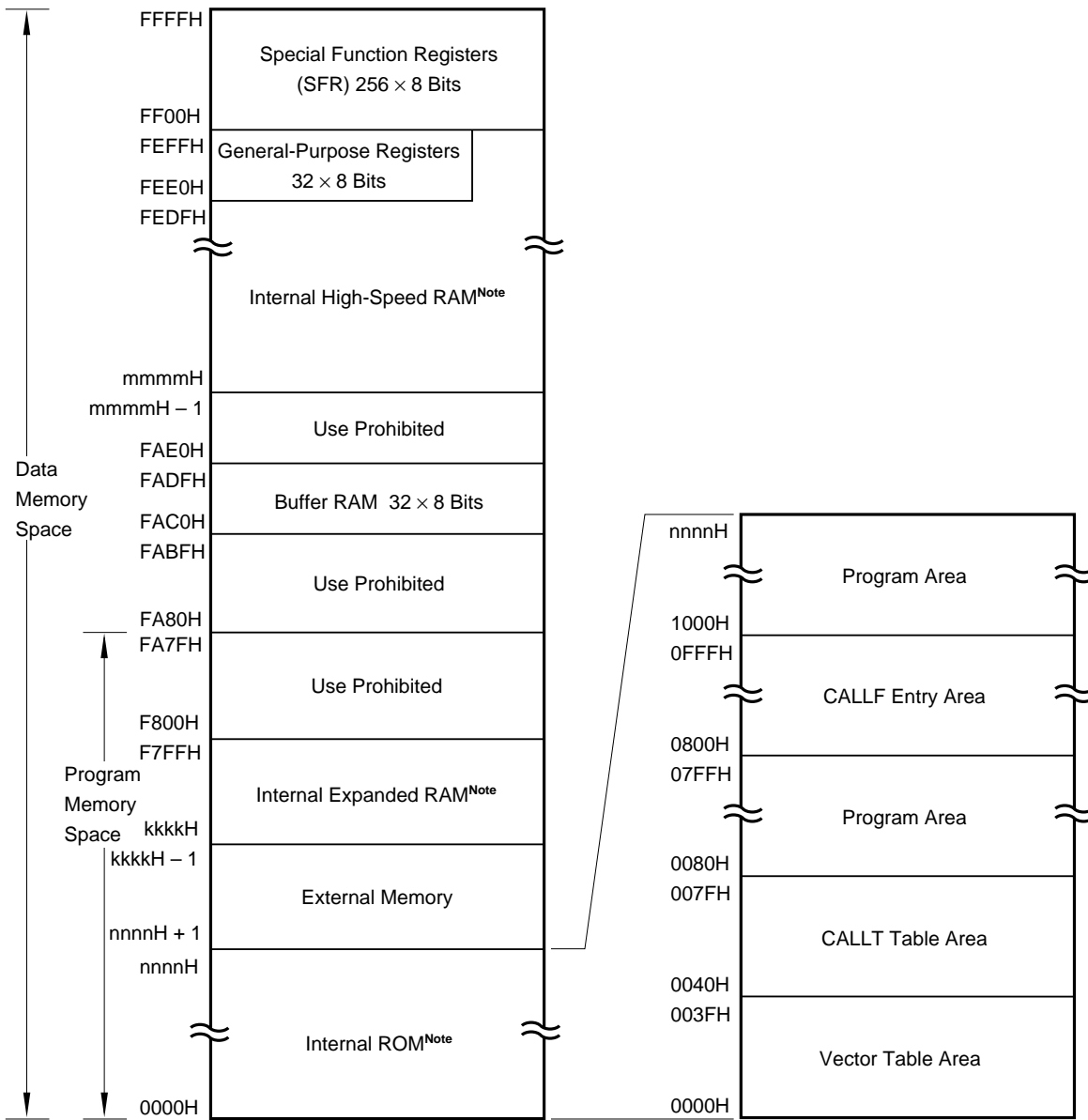
Figure 4-1. Memory Map (μPD78011FY, 78012FY, 78013FY, 78014FY)



**Note** Internal ROM and internal high-speed RAM capacities vary depending on the product (refer to the table below).

Product Name	Internal ROM End Address nnnnH	Internal High-Speed RAM Start Address mmmmH
μPD78011FY	1FFFH	FD00H
μPD78012FY	3FFFH	
μPD78013FY	5FFFH	FB00H
μPD78014FY	7FFFH	

Figure 4-2. Memory Map (μPD78015FY, 78016FY, 78018FY)



**Note** Internal ROM, internal high-speed RAM, and internal expanded RAM capacities vary depending on the product (refer to the table below).

Product Name	Internal ROM End Address nnnnH	Internal High-Speed RAM Start Address mmmmH	Internal Expanded RAM Start Address kkkkH
μPD78015FY	9FFFH	FB00H	F600H
μPD78016FY	BFFFH		F400H
μPD78018FY	EFFFH		

## 5. PERIPHERAL HARDWARE FUNCTION FEATURES

### 5.1 PORTS

The I/O port has the following three types

- CMOS input (P00, P04) : 2
  - CMOS input/output (P01 to P03, port 1 to port 5, P64 to P67) : 47
  - N-ch open-drain input/output(15V withstand voltage) (P60 to P63) : 4
- 
- Total : 53

**Table 5-1. Functions of Ports**

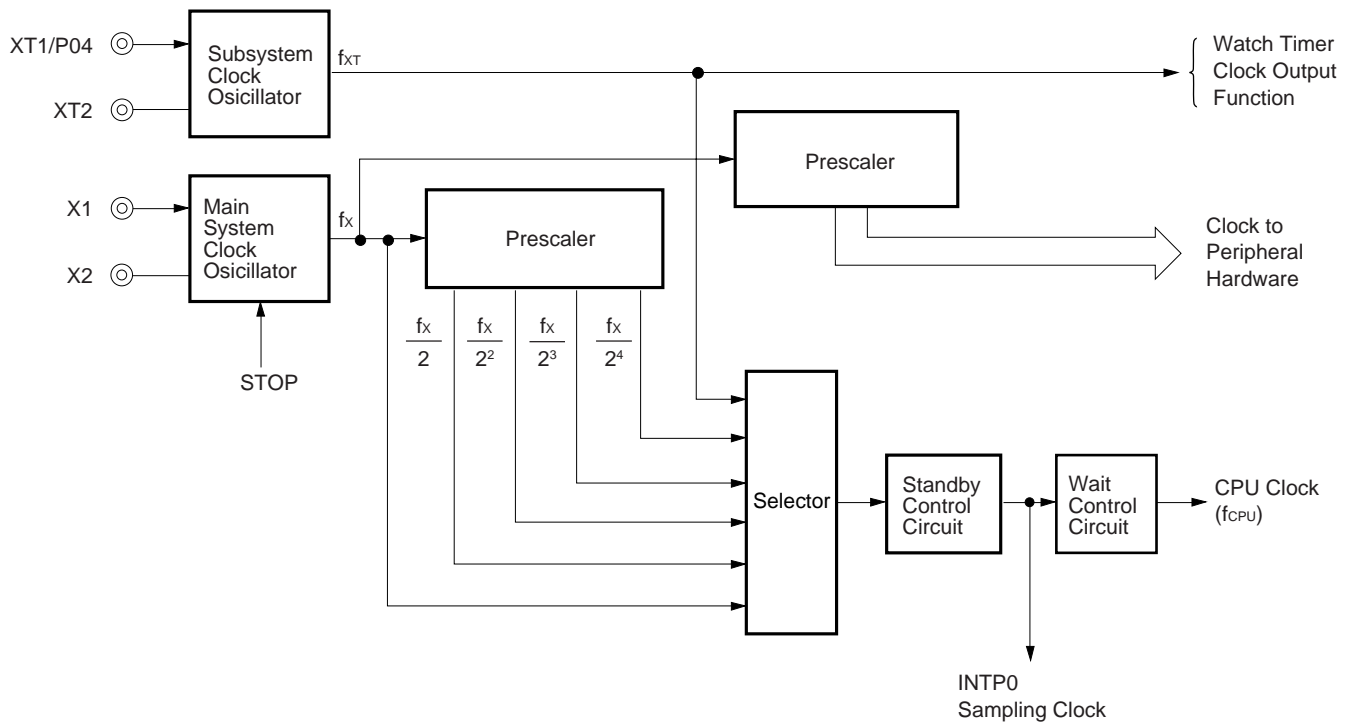
Port Name	Pin Name	Function
Port 0	P00, P04	Dedicated Input port
	P01 to P03	Input/output ports. Input/output can be specified bit-wise. When used as an input port, pull-up resistor can be used in software.
Port 1	P10 to P17	Input/output ports. Input/output can be specified bit-wise. When used as an input port, pull-up resistor can be used in software.
Port 2	P20 to P27	Input/output ports. Input/output can be specified bit-wise. When used as an input port, pull-up resistor can be used in software.
Port 3	P30 to P37	Input/output ports. Input/output can be specified bit-wise. When used as an input port, pull-up resistor can be used in software.
Port 4	P40 to P47	Input/output ports. Input/output can be specified in 8-bit units. When used as an input port, pull-up resistor can be used in software. Test input flag (KRIF) is set to 1 by falling edge detection.
Port 5	P50 to P57	Input/output ports. Input/output can be specified bit-wise. When used as an input port, pull-up resistor can be used in software. LED can be driven directly.
Port 6	P60 to P63	N-ch open-drain input/output port. Input/output can be specified bit-wise. On-chip pull-up resistor can be specified by mask option. LED can be driven directly.
	P64 to P67	Input/output ports. Input/output can be specified bit-wise. When used as an input port, pull-up resistor can be used in software.

### 5.2 CLOCK GENERATOR

There are two types of clock generator: main system clock and subsystem clock.  
The minimum instruction execution time can be changed.

- $0.4\mu\text{s}/0.8\mu\text{s}/1.6\mu\text{s}/3.2\mu\text{s}/6.4\mu\text{s}$  (Main system clock: at 10.0 MHz operation)
- $122\mu\text{s}$  (Subsystem clock: at 32.768 KHz operation)

Figure 5-1. Clock Generator Block Diagram



5.3 TIMER/EVENT COUNTER

The following five channels are incorporated in the timer/event counter.

- 16-bit timer/event counter : 1 channel
- 8-bit timer/event counter : 2 channels
- Watch timer : 1 channel
- Watchdog timer : 1 channel

Table 5-2. Operation of Timer/Event Counter

		16-bit Timer/Event Counter	8-bit Timer/Event Counter	Watch Timer	Watchdog Timer
Operation mode	Interval timer	1 channel	2 channels	1 channel	1 channel
	External event counter	1 channel	2 channels	–	–
Functions	Timer output	1 output	2 outputs	–	–
	PWM output	1 output	–	–	–
	Pulse width measurement	1 input	–	–	–
	Square wave output	1 output	2 outputs	–	–
	Interrupt request	2	2	1	1
	Test input	–	–	1 input	–

Figure 5-2. 16-bit Timer/Event Counter Block Diagram

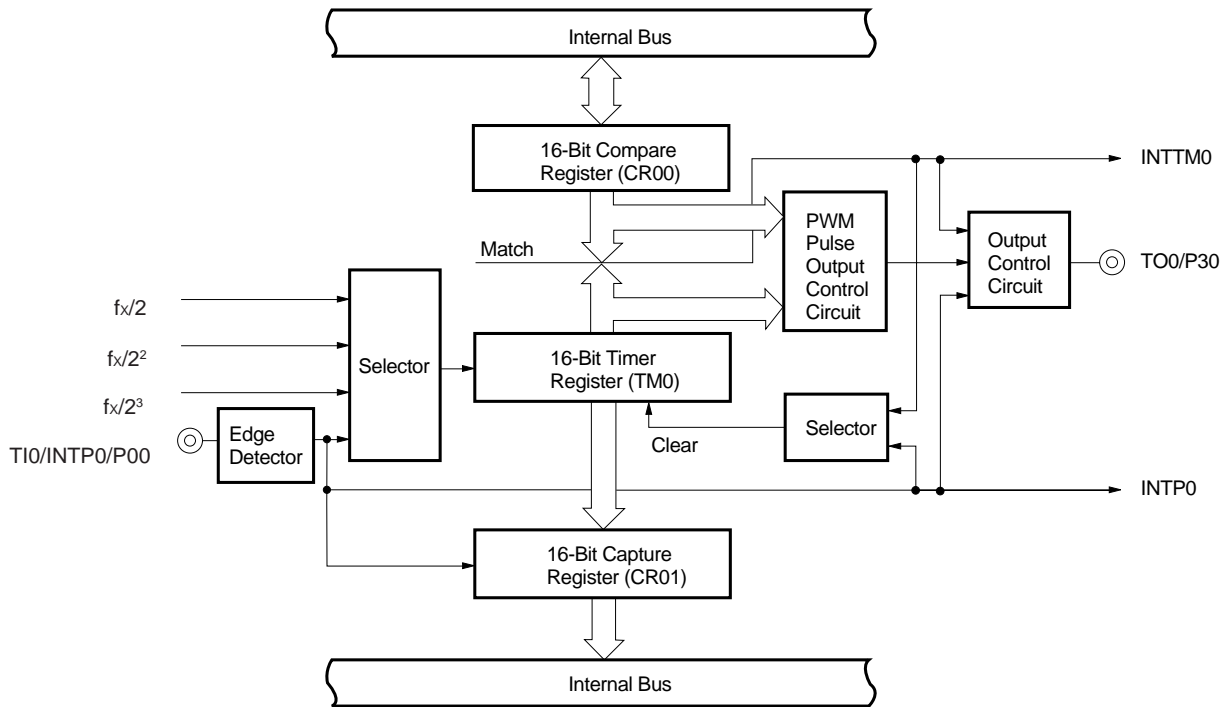


Figure 5-3. 8-bit Timer/Event Counter Block Diagram

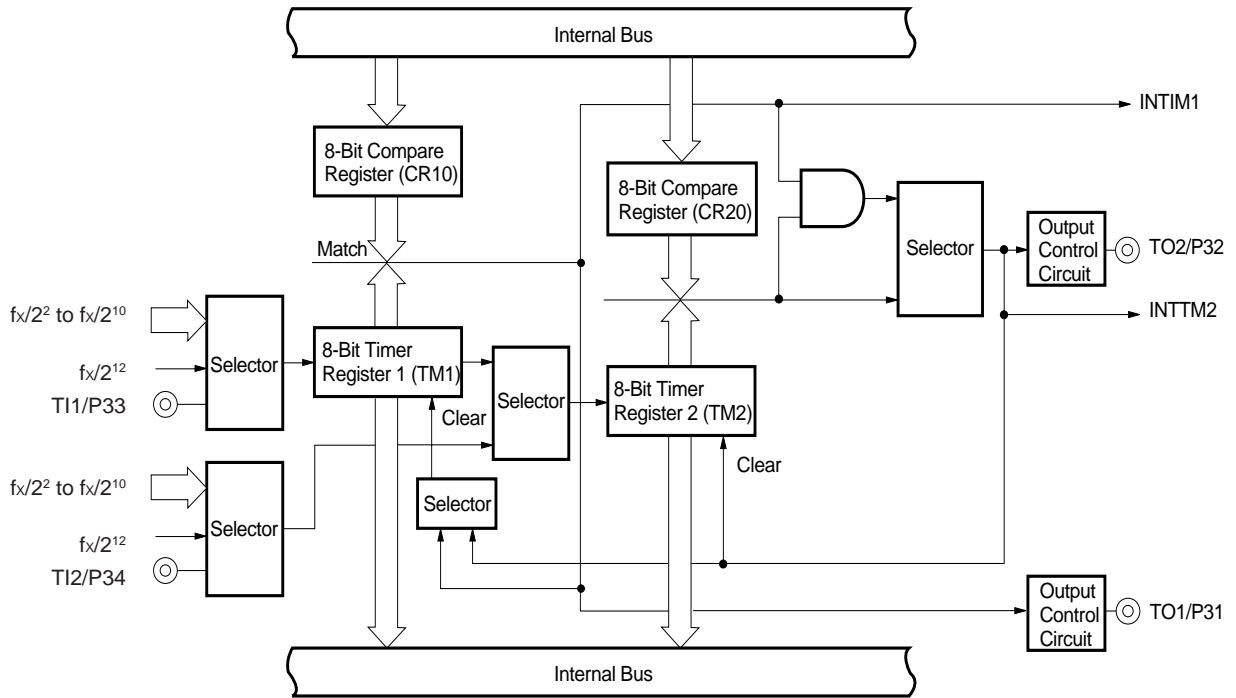


Figure 5-4. Watch Timer Block Diagram

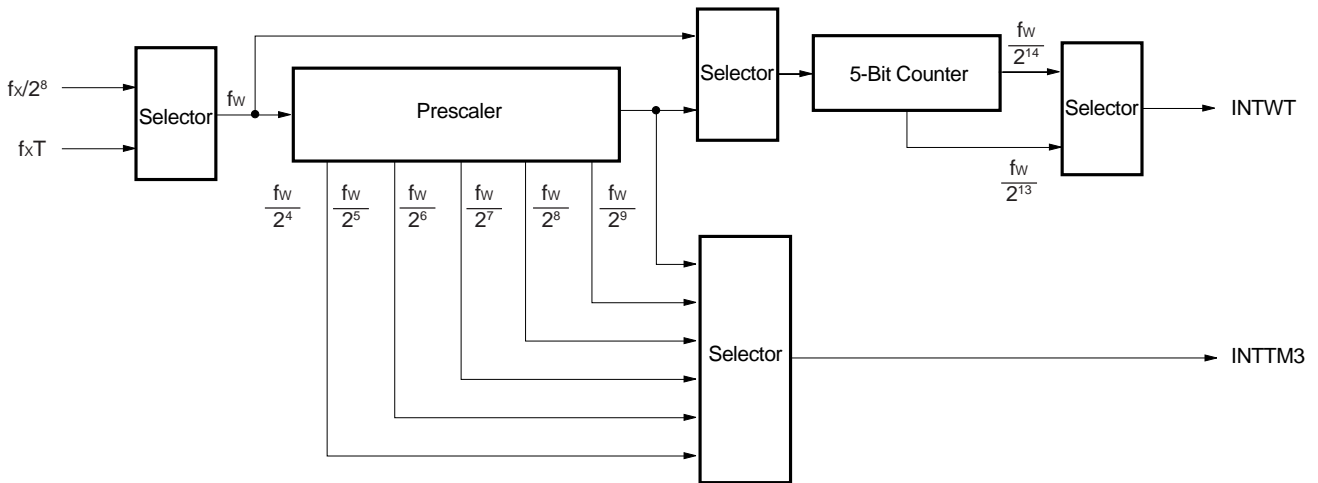
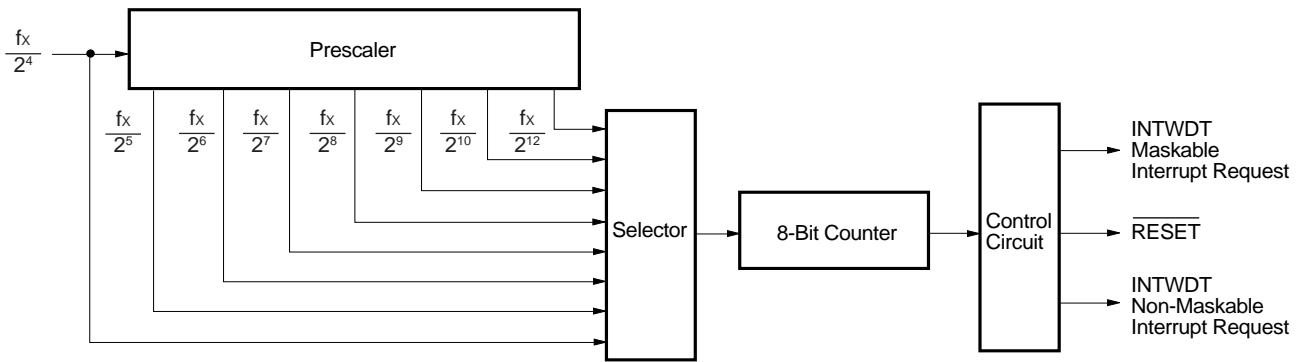


Figure 5-5. Watchdog Timer Block Diagram

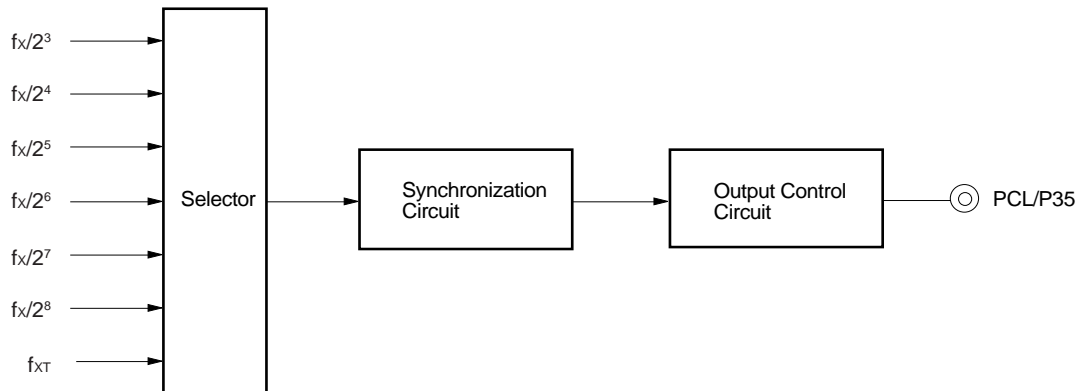


**5.4 CLOCK OUTPUT CONTROL CIRCUIT**

The clock with the following frequencies can be output for clock output.

- 39.1 kHz/78.1 kHz/156 kHz/313 kHz/625 kHz/1.25 MHz (Main system clock: at 10.0 MHz operation)
- 32.768 kHz (Subsystem clock: at 32.768 kHz operation)

Figure 5-6. Clock Output Control Block Diagram

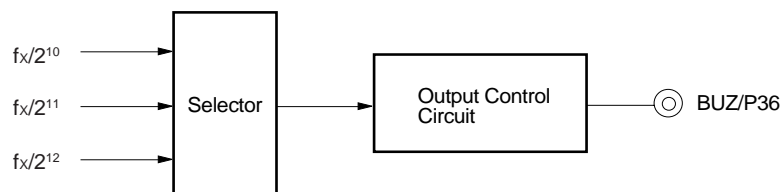


**5.5 BUZZER OUTPUT CONTROL CIRCUIT**

The clock with the following frequencies can be output for buzzer output.

- 2.4 kHz/4.9 kHz/9.8 kHz (Main system clock: at 10.0 MHz operation)

Figure 5-7. Buzzer Output Control Block Diagram

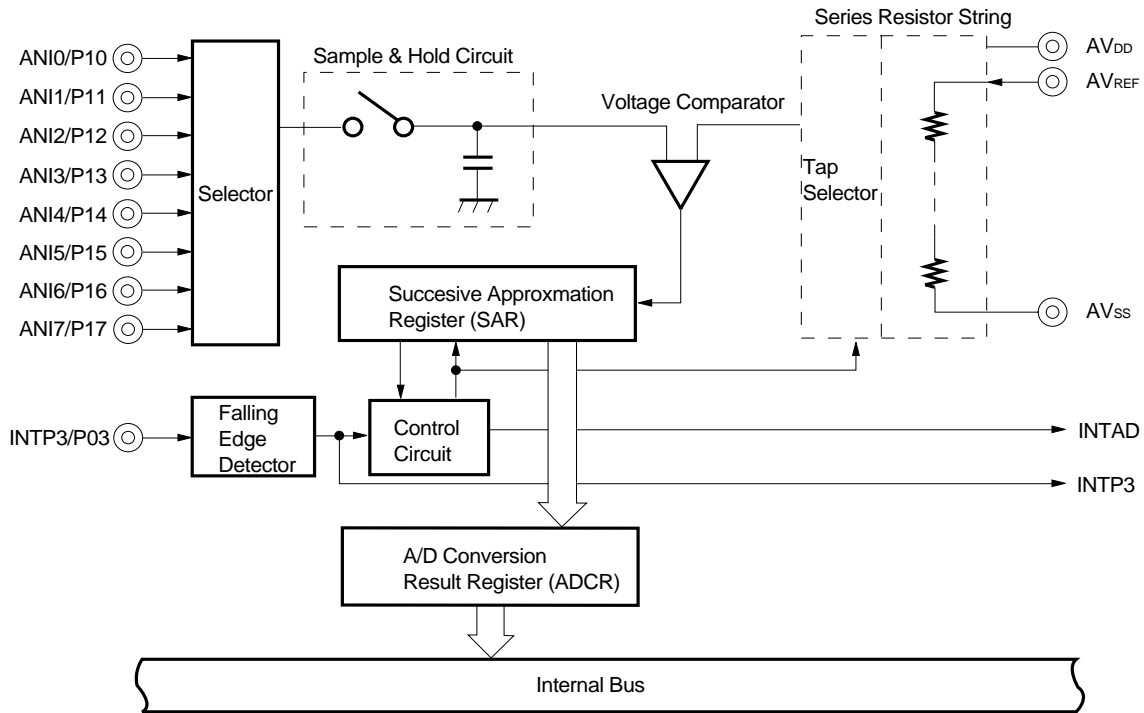


**5.6 A/D CONVERTER**

The A/D converter has on-chip eight 8-bit resolution channels. There are the following two method to start A/D conversion.

- Hardware starting
- Software starting

**Figure 5-8. A/D Converter Block Diagram**



**5.7 SERIAL INTERFACES**

There are two on-chip clocked serial interfaces as follows.

- Serial Interface channel 0
- Serial Interface channel 1

**Table 5-3. Type and Function of Serial Interface**

Function	Serial Interface Channel 0	Serial Interface Channel 1
3-wire serial I/O mode	O (MSB/LSB-first switchable)	O (MSB/LSB-first switchable)
3-wire serial I/O mode with automatic data transmit/receive function	–	O (MSB/LSB-first switchable)
2-wire serial I/O mode	O (MSB-first)	–
I <sup>2</sup> C (Inter IC) bus mode	O (MSB-first)	–



Figure 5-9. Serial Interface Channel 0 Block Diagram

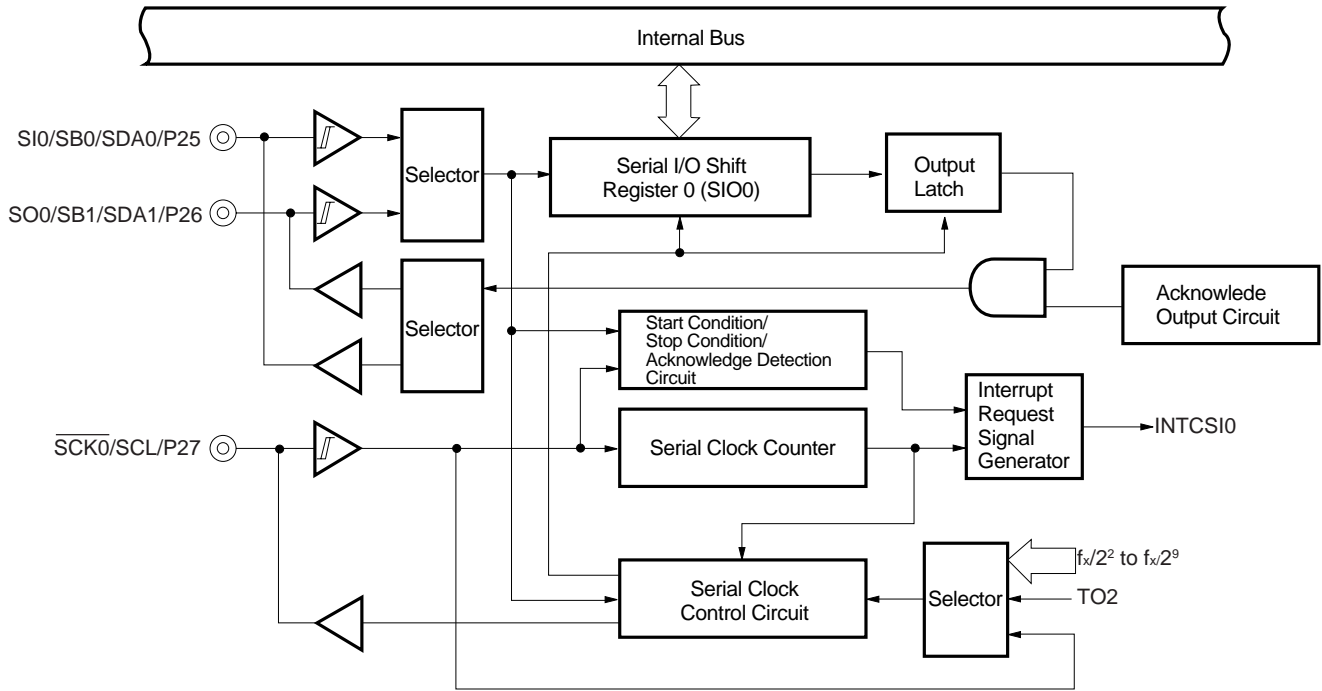
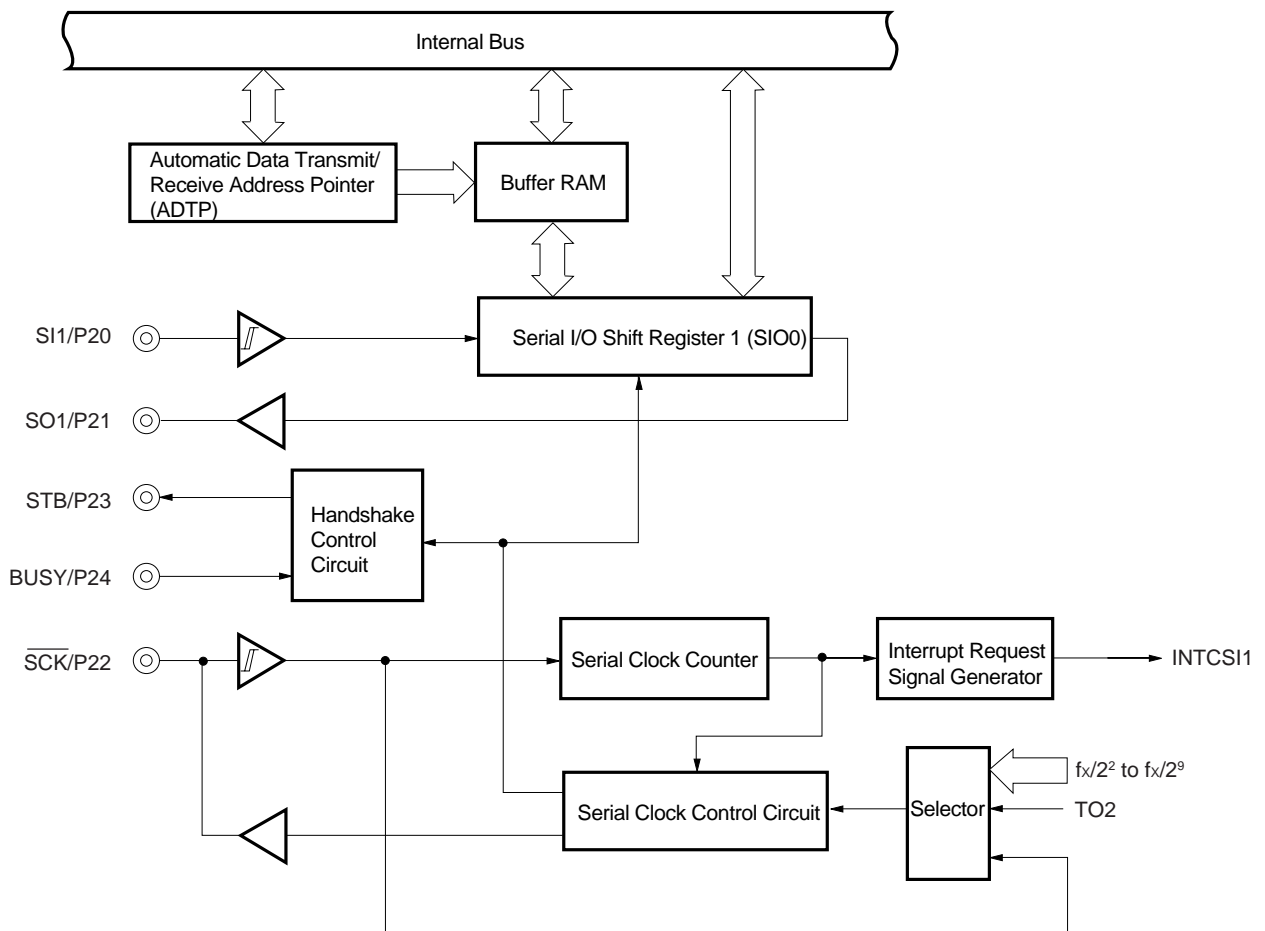


Figure 5-10. Serial Interface Channel 1 Block Diagram



## 6. INTERRUPT FUNCTIONS AND TEST FUNCTIONS

### 6.1 INTERRUPT FUNCTIONS

There are interrupt functions, 14 sources of three different kinds, as shown below.

- Non-maskable : 1
- Maskable : 12
- Software : 1

**Table 6-1. Interrupt Source List**

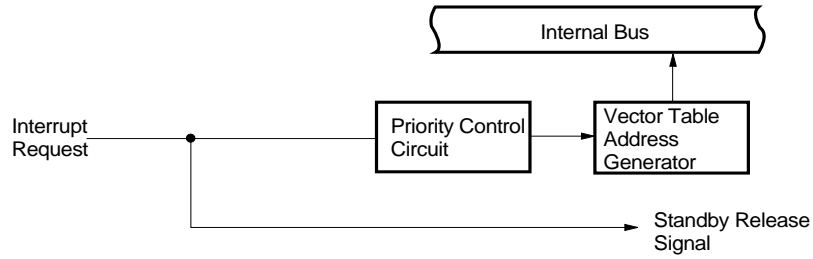
Interrupt Type	Default Priority <sup>Note 1</sup>	Interrupt Source		Internal/ External	Vector Table Address	Basic Configuration Type <sup>Note 2</sup>		
		Name	Trigger					
Non-maskable	—	INTWDT	Watchdog timer overflow (with watchdog timer mode 1 selected)	Internal	0004H	(A)		
Maskable	0	INTWDT	Watchdog timer overflow (with interval timer mode selected)			External	0006H 0008H 000AH 000CH	(B)
	1	INTP0	Pin input edge detection	Internal	000EH 0010H 0012H 0014H 0016H 0018H 001AH			(C)
	2	INTP1						(D)
	3	INTP2						(B)
	4	INTP3				(B)		
	5	INTCSI0	Serial interface channel 0 transfer end	Internal	000EH 0010H 0012H 0014H 0016H 0018H 001AH	(B)		
	6	INTCSI1	Serial interface channel 1 transfer end			(B)		
	7	INTTM3	Reference time interval signal from watch timer			(B)		
	8	INTTM0	16 bit timer/event counter match signal generation			(B)		
	9	INTTM1	8-bit timer/event counter 1 match signal generation			(B)		
	10	INTTM2	8-bit timer/event counter 2 match signal generation			(B)		
11	INTAD	A/D converter conversion end	(B)					
Software	—	BRK	BRK instruction execution	—	003EH	(E)		

**Notes 1.** The default priority is the priority applicable when more than one maskable interrupt request is generated. 0 is the highest priority and 11, the lowest.

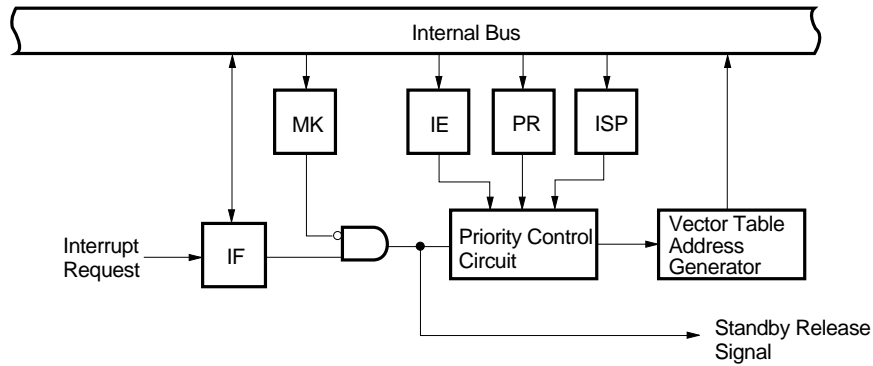
**2.** Basic configuration types (A) to (E) correspond to (A) to (E) on the next page.

Figure 6-1. Basic Interrupt Function Configuration (1/2)

(A) Internal Non-Maskable Interrupt



(B) Internal Maskable Interrupt



(C) External Maskable Interrupt (INTP0)

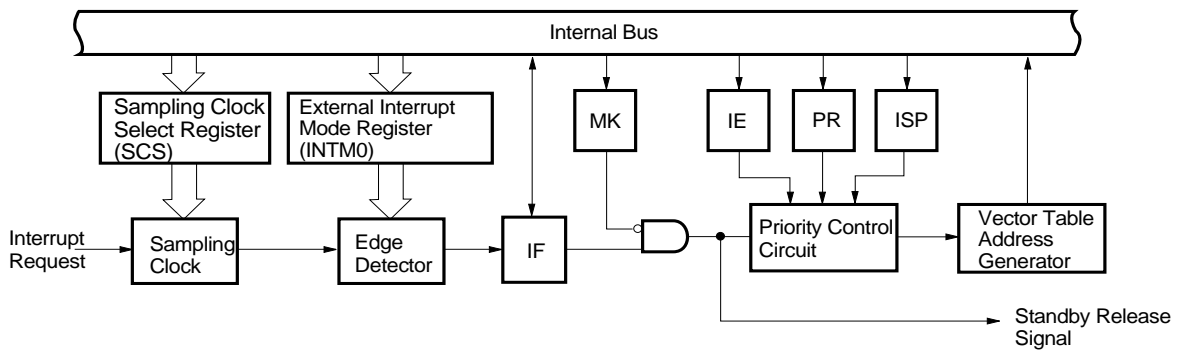
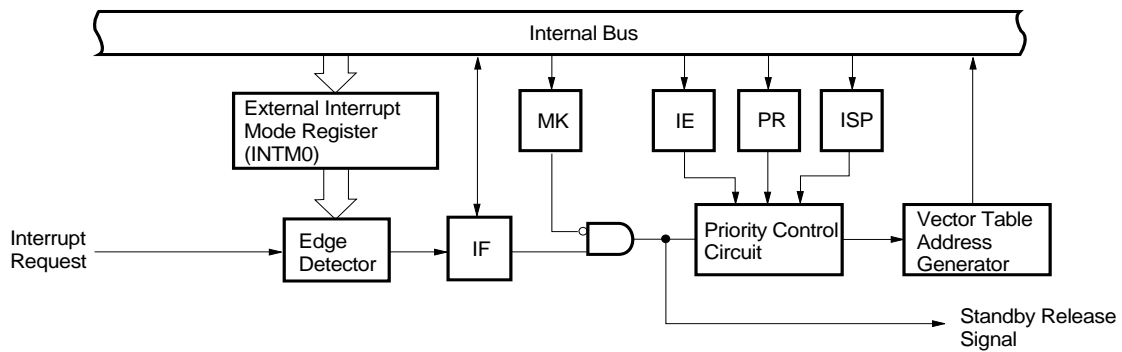
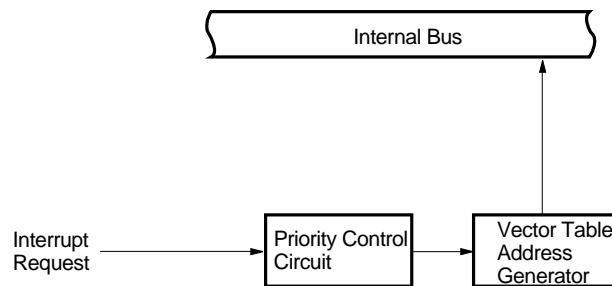


Figure 6-1. Basic Interrupt Function Configuration (2/2)

(D) External Maskable Interrupt (Except INTP0)



(E) Software Interrupt



- IF : Interrupt request flag
- IE : Interrupt enable flag
- ISP : In-service priority flag
- MK : Interrupt mask flag
- PR : Priority specification flag

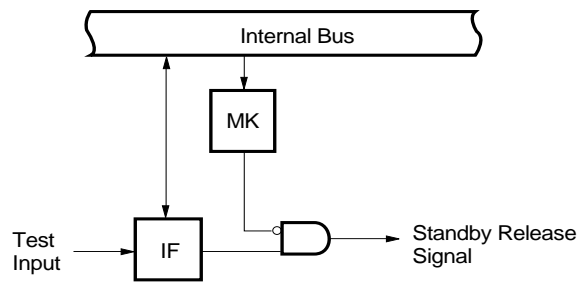
6.2 TEST FUNCTIONS

There are two test functions as shown in Table 6-2.

Table 6-2. Test Source List

Test Source		Internal/External
Name	Trigger	
INTWT	Watch timer overflow	Internal
INTPT4	Port 4 falling edge detection	External

Figure 6-2. Test Function Basic Configuration



IF : Test input flag  
 MK : Test mask flag

### 7. EXTERNAL DEVICE EXPANSION FUNCTIONS

The external device expansion function is used to connect external devices to areas other than the internal ROM, RAM and SFR.

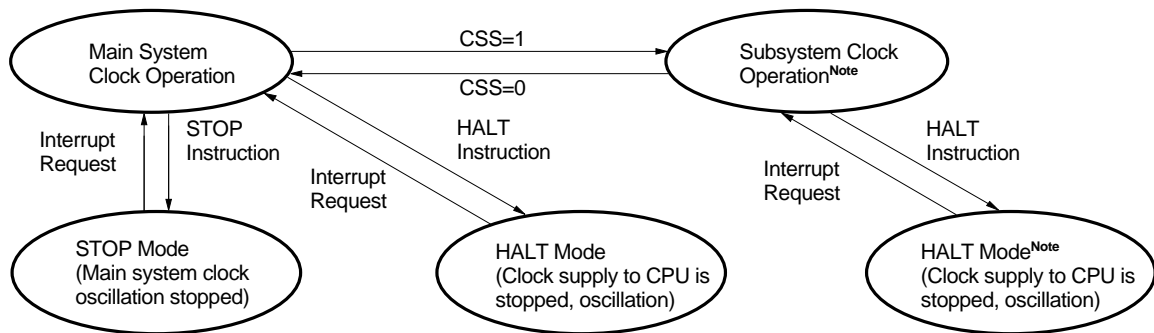
Ports 4 to 6 are used for connection with external devices.

### 8. STANDBY FUNCTIONS

There are the following two standby functions to reduce the current dissipation.

- HALT mode : The CPU operating clock is stopped. The average consumption current can be reduced by intermittent operation in combination with the normal operating mode.
- STOP mode : The main system clock oscillation is stopped. The whole operation by the main system clock is stopped, so that the system operates with ultra-low power consumption using only the subsystem clock.

Figure 8-1. Standby Functions



**Note** The power consumption can be reduced by stopping the main system clock. When the CPU is operating on the subsystem clock, set the MCC to stop the main system clock. The STOP instruction cannot be used.

**Caution** When the main system clock is stopped and the system is operated by the subsystem clock, the subsystem clock should be switched again to the main system clock after the oscillation stabilization time is secured by the program by the program.

### 9. RESET FUNCTIONS

There are the following two reset methods.

- External reset input by  $\overline{\text{RESET}}$  pin.
- Internal reset by watchdog timer runaway time detection.

10. INSTRUCTION SET

(1) 8-Bit Instruction

MOV, XCH, ADD, ADDC, SUB, SUBC, AND, OR, XOR, CMP, MULU, DIVUW, INC, DEC, ROR, ROL, RORC, ROLC, ROR4, ROL4, PUSH, POP, DBNZ

2nd Operand 1st Operand	#byte	A	r Note	sfr	saddr	!addr16	PSW	[DE]	[HL]	[HL+byte] [HL+B] [HL+C]	\$addr16	1	None
A	ADD ADDC SUB SUBC AND OR XOR CMP		MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH	MOV	MOV XCH	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP		ROR ROL RORC ROLC	
r	MOV	MOV	ADD ADDC SUB SUBC AND OR XOR CMP										INC DEC
★ B, C											DBNZ		
sfr	MOV	MOV											
saddr	MOV  SUBC AND OR XOR CMP	MOV ADD ADDC SUB									DBNZ		INC DEC
!addr16		MOV											
PSW	MOV	MOV											PUSH POP
[DE]		MOV											
[HL]		MOV											ROR4 ROL4
[HL+byte] [HL+B] [HL+C]		MOV											
X													MULU
C													DIVUW

Note Except r=A

**(2) 16-Bit Instruction**

MOVW, XCHW ADDW, SUBW, CMPW, PUSH, POP, INCW, DECW

2nd Operand 1st Operand	#byte	AX	rp <sup>Note</sup>	saddrp	!addr16	SP	None	
AX	ADDW SUBW CMPW		MOVW XCHW	MOVW	MOVW	MOVW	MOVW	
rp	MOVW	MOVW <sup>Note</sup>						INCW, DECW PUSH, POP
sfrp	MOVW	MOVW						
saddrp	MOVW	MOVW						
!addr16		MOVW						
SP	MOVW	MOVW						

**Note** Only when rp=BC, DE, HL.

**(3) Bit Manipulation Instruction**

MOV1, AND1, OR1, XOR1, SET1, CLR1, NOT1, BT, BF, BTCLR

2nd Operand 1st Operand	A.bit	sfr.bit	saddr.bit	PWS.bit	[HL].bit	CY	\$addr16	None
A.bit						MOV1	BT BF BTCLR	SET1 CLR1
sfr.bit						MOV1	BT BF BTCLR	SET1 CLR1
saddr.bit						MOV1	BT BF BTCLR	SET1 CLR1
PSW.bit						MOV1	BT BF BTCLR	SET1 CLR1
[HL].bit						MOV1	BT BF BTCLR	SET1 CLR1
CY	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1			SET1 CLR1 NOT1



**(4) Call Instruction/Branch Instruction**

CALL, CALLF, CALLT, BR, BC, BNC, BZ, BNZ, BT, BF, BTCLR, DBNZ

2nd Operand 1st Operand	AX	!addr16	!addr11	[addr5]	\$addr16
Basic instruction	BR	CALL, BR	CALLF	CALLT	BR, BC, BNC, BZ, BNZ
Compound instruction					BT,BF,BTCLR, DBNZ

**(5) Other Instruction**

ADJBA, ADJBS, BRK, RET, RETI, RETB, SEL, NOP, EI, DI, HALT, STOP

## 11. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings ( $T_A = 25\text{ }^\circ\text{C}$ )

Parameter	Symbol	Test Conditions		Rating	Unit
Supply voltage	$V_{DD}$			-0.3 to +7.0	V
	$AV_{DD}$			-0.3 to $V_{DD} + 0.3$	V
	$AV_{REF}$			-0.3 to $V_{DD} + 0.3$	V
	$AV_{SS}$			-0.3 to +0.3	V
Input voltage	$V_{I1}$	P00 to P04, P10 to P17, P20 to P27, P30 to P37 P40 to P47, P50 to P57, P64 to P67, X1, X2, XT2		-0.3 to $V_{DD} + 0.3$	V
	$V_{I2}$	P60 to P67	Open-drain	-0.3 to +16	V
Output voltage	$V_O$			-0.3 to $V_{DD} + 0.3$	V
Analog input voltage	$V_{AN}$	P10 to P17	Analog input pin	$AV_{SS} - 0.3$ to $AV_{REF} + 0.3$	V
Output current high		1 pin		-10	mA
	$I_{OH}$	P10 to P17, P20 to P27, P30 to P37 total		-15	mA
		P01 to P03, P40 to P47, P50 to P57, P60 to P67 total		-15	mA
Output current low		1 pin	Peak value	30	mA
			rms	15	mA
		P40 to P47, P50 to P55 total	Peak value	100	mA
			rms	70	mA
	$I_{OL}$ Note	P01 to P03, P56, P57, P60 to P67 total	Peak value	100	mA
			rms	70	mA
		P01 to P03, P64 to P67 total	Peak value	50	mA
			rms	20	mA
		P10 to P17, P20 to P27, P30 to P37 total	Peak value	50	mA
			rms	20	mA
Operating ambient temperature	$T_A$			-40 to +85	$^\circ\text{C}$
Storage temperature	$T_{stg}$			-65 to +150	$^\circ\text{C}$

**Note** rms should be calculated as follows:  $[\text{rms}] = [\text{peak value}] \times \sqrt{\text{duty}}$

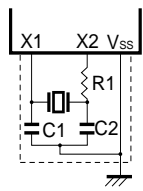
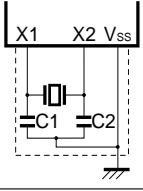
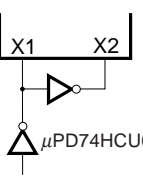
**Caution** Product quality may suffer if the absolute maximum rating is exceeded for even a single parameter or even momentarily. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions which ensure that the absolute maximum ratings are not exceeded.

**Capacitance** (  $T_A = 25\text{ }^\circ\text{C}$ ,  $V_{DD} = V_{SS} = 0\text{ V}$  )

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	$C_{IN}$	$f = 1\text{ MHz}$ Unmeasured pins returned to 0 V			15	pF
I/O capacitance	$C_{IO}$	$f = 1\text{ MHz}$ Unmeasured pins returned to 0 V	P01 to P03, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P64 to P67		15	pF
			P60 to P63		20	pF

**Remark** The characteristics of a dual-function pin and a port pin are the same unless specified otherwise.

**Main System Clock Oscillation Circuit Characteristics** (  $T_A = -40\text{ to }+85\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.8\text{ to }5.5\text{ V}$  )

Resonator	Recommended Circuit	Parameter	Test Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillator frequency ( $f_x$ ) <b>Note 1</b>	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	1		10	MHz
			$1.8\text{ V} \leq V_{DD} < 2.7\text{ V}$	1		5	
		Oscillation stabilization time <b>Note 2</b>	After $V_{DD}$ reaches oscillator voltage range MIN.			4	ms
Crystal resonator		Oscillator frequency ( $f_x$ ) <b>Note 1</b>	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	1		10	MHz
			$1.8\text{ V} \leq V_{DD} < 2.7\text{ V}$	1		5	
		Oscillation stabilization time <b>Note 2</b>	$V_{DD} = 4.5\text{ to }5.5\text{ V}$			10	ms
						30	
External clock		X1 input frequency ( $f_x$ ) <b>Note 1</b>		1.0		10.0	MHz
		X1 input high/low level width ( $t_{xH}$ , $t_{xL}$ )		45		500	ns

**Notes 1.** Indicates only oscillation circuit characteristics. Refer to **AC Characteristics** for instruction execution time.

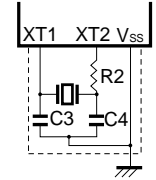
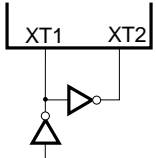
**2.** Time required to stabilize oscillation after reset or STOP mode release.

**Cautions 1.** When using the main system clock oscillator, wiring the area enclosed with the dotted line should be carried out as follows to avoid an adverse effect from wiring capacitance.

- Wiring should be as short as possible.
- Wiring should not cross other signal lines.
- Wiring should not be placed close to a varying high current.
- The potential of the oscillator capacitor ground should be the same as  $V_{SS}$ .
- Do not ground wiring to a ground pattern in which a high current flows.
- Do not fetch a signal from the oscillator.

**2.** When the main system clock is stopped and the system is operated by the subsystem clock, the subsystem clock should be switched again to the main system clock after the oscillation stabilization time is secured by the program.

**Subsystem Clock Oscillation Circuit Characteristics** ( $T_A = -40$  to  $+85$  °C,  $V_{DD} = 1.8$  to  $5.5$  V)

Resonator	Recommended Circuit	Parameter	Test Conditions	MIN.	TYP.	MAX.	Unit
Crystal resonator		Oscillator frequency ( $f_{XT}$ ) <b>Note 1</b>		32	32.768	35	kHz
		Oscillation stabilization time <b>Note 2</b>	$V_{DD} = 4.5$ to $5.5$ V		1.2	2	s
External clock		XT1 input frequency ( $f_{XT}$ ) <b>Note 1</b>		32		100	
		XT1 input high/low level width ( $t_{XTH}$ , $t_{XTL}$ )		5		15	μs

**Notes 1.** Indicates only oscillation circuit characteristics. Refer to **AC Characteristics** for instruction execution time.

**2.** Time required to stabilize oscillation after  $V_{DD}$  reaches oscillator voltage MIN.

**Cautions 1.** When using the subsystem clock oscillator, wiring in the area enclosed with the dotted line should be carried out as follows to avoid an adverse effect from wiring capacitance.

- Wiring should be as short as possible.
- Wiring should not cross other signal lines.
- Wiring should not be placed close to a varying high current.
- The potential of the oscillator capacitor ground should be the same as  $V_{SS}$ .
- Do not ground wiring to a ground pattern in which a high current flows.
- Do not fetch a signal from the oscillator.

**2.** The subsystem clock oscillation circuit is a circuit with a low amplification level, more prone to misoperation due to noise than the main system clock.

Particular care is therefore required with the wiring method when the subsystem clock is used.

★ Recommended Oscillation Circuit Constant

Recommended oscillation circuit constant differs depending on the model.

(1) μPD78011FY, 78012FY, 78013FY, 78014FY

(a) Main system clock: ceramic resonator (T<sub>A</sub> = -45 to +85 °C)

Manufacturer	Product Name	Frequency (MHz)	Recommended Oscillation Circuit Constant		Oscillation Voltage Range	
			C1 (pF)	C2 (pF)	MIN. (V)	MAX. (V)
TDK Corp.	CCR4.19MC3	4.19	Built-in	Built-in	1.8	5.5
	FCR4.19MC5	4.19	Built-in	Built-in	1.8	5.5
	CCR5.00MC3	5.00	Built-in	Built-in	1.8	5.5
	FCR5.00MC5	5.00	Built-in	Built-in	1.8	5.5
	CCR8.38MC	8.00	Built-in	Built-in	2.7	5.5
	FCR8.38MC5	8.00	Built-in	Built-in	2.7	5.5
	CCR10.00MC	10.00	Built-in	Built-in	2.7	5.5
	FCR10.00MC5	10.00	Built-in	Built-in	2.7	5.5
Murata Mfg. Co. Ltd.	CSA4.19MG	4.19	30	30	1.8	5.5
	CST4.19MGW	4.19	Built-in	Built-in	1.8	5.5
	CSA5.00MG	5.00	30	30	1.8	5.5
	CST5.00MGW	5.00	Built-in	Built-in	1.8	5.5
	CSA8.38MTZ	8.38	30	30	2.7	5.5
	CST8.38MTW	8.38	Built-in	Built-in	2.7	5.5
	CSA10.00MTZ	10.00	30	30	2.7	5.5
	CST10.00MTW	10.00	Built-in	Built-in	2.7	5.5

(b) Main system clock: ceramic resonator (T<sub>A</sub> = -20 to +80 °C)

Manufacturer	Product Name	Frequency (MHz)	Recommended Oscillation Circuit Constant		Oscillation Voltage Range	
			C1 (pF)	C2 (pF)	MIN. (V)	MAX. (V)
Kyocera Corp.	PBRC5.00A	5.00	33	33	1.8	5.5
	PBRC5.00B	5.00	Built-in	Built-in	1.8	5.5
	KBR-5.00MSA	5.00	33	33	1.8	5.5
	KBR-5.00MKS	5.00	Built-in	Built-in	1.8	5.5
	KBR-8M	8.00	33	33	2.7	5.5
	KBR-10M	10.00	33	33	2.7	5.5

**Caution** The oscillation circuit constants and oscillation voltage range indicate conditions for stable oscillation but do not guarantee the accuracy of the oscillation frequency. If the application circuit requires accuracy of the oscillation frequency, it is necessary to set the oscillation frequency of the resonator in the application circuit. For this, it is necessary to directly contact manufacturer of the resonator being used.

(2) μPD78015FY, 78016FY

(a) Main system clock: ceramic resonator (T<sub>A</sub> = -45 to +85 °C)

Manufacturer	Product Name	Frequency (MHz)	Recommended Oscillation Circuit Constant			Oscillation Voltage Range	
			C1 (pF)	C2 (pF)	R1 (kΩ)	MIN. (V)	MAX. (V)
Murata Mfg. Co. Ltd.	CSB1000J	1.00	100	100	5.6	1.8	6.0
	CSA2.00MG040	2.00	100	100	0	1.8	6.0
	CST2.00MG040	2.00	Built-in	Built-in	0	1.8	6.0
	CSA4.00MG040	4.00	100	100	0	1.8	6.0
	CST4.00MGW040	4.00	Built-in	Built-in	0	1.8	6.0
	CSA6.00MG	6.00	30	30	0	1.8	6.0
	CST6.00MGW	6.00	Built-in	Built-in	0	1.8	6.0
	CSA10.0MTZ	10.0	30	30	0	1.8	6.0
	CST10.0MTW	10.0	Built-in	Built-in	0	1.8	6.0
Murata Mfg. Co. Ltd. (EMI noise reduced products)	CSA6.00MG040	6.00	100	100	0	2.7	6.0
	CST6.00MGW040	6.00	Built-in	Built-in	0	2.7	6.0
	CSA10.0MTZ040	10.0	100	100	0	2.7	6.0
	CST10.0MTW040	10.0	Built-in	Built-in	0	2.7	6.0
TDK Corp.	FCR4.0MC5	4.0	Built-in	Built-in	2.2	1.8	6.0
	FCR10.0MC	10.0	Built-in	Built-in	1.0	1.8	6.0

(b) Main system clock: ceramic resonator (T<sub>A</sub> = -20 to +80 °C)

Manufacturer	Product Name	Frequency (MHz)	Recommended Oscillation Circuit Constant		Oscillation Voltage Range	
			C1 (pF)	C2 (pF)	MIN. (V)	MAX. (V)
Kyocera Corp.	PBRC5.00A	5.00	33	33	1.8	5.5
	PBRC5.00B	5.00	Built-in	Built-in	1.8	5.5
	KBR-5.00MSA	5.00	33	33	1.8	5.5
	KBR-5.00MKS	5.00	Built-in	Built-in	1.8	5.5
	KBR-8M	8.00	33	33	2.7	5.5
	KBR-10M	10.00	33	33	2.7	5.5

**Caution** The oscillation circuit constants and oscillation voltage range indicate conditions for stable oscillation but do not guarantee the accuracy of the oscillation frequency. If the application circuit requires accuracy of the oscillation frequency, it is necessary to set the oscillation frequency of the resonator in the application circuit. For this, it is necessary to directly contact manufacturer of the resonator being used.

(3) μPD78018FY

(a) Main system clock: ceramic resonator (T<sub>A</sub> = -40 to +85 °C)

Manufacturer	Product Name	Frequency (MHz)	Recommended Oscillation Circuit Constant		Oscillation Voltage Range	
			C1 (pF)	C2 (pF)	MIN. (V)	MAX. (V)
TDK Corp.	CCR4.0MC3	4.00	Built-in	Built-in	1.8	5.5
	FCR4.0MC5	4.00	Built-in	Built-in	1.8	5.5
	CCR8.0MC5	8.00	Built-in	Built-in	2.7	5.5
	FCR8.0MC	8.00	Built-in	Built-in	2.7	5.5
	CCR10.0MC5	10.0	Built-in	Built-in	2.7	5.5
	FCR10.0MC	10.0	Built-in	Built-in	2.7	5.5
Murata Mfg. Co. Ltd.	CSA4.0MG	4.00	30	30	1.8	5.5
	CST4.0MGW	4.00	Built-in	Built-in	1.8	5.5
	CSA8.0MTZ	8.00	30	30	2.7	5.5
	CST8.0MTW	8.00	Built-in	Built-in	2.7	5.5

(b) Main system clock: ceramic resonator (T<sub>A</sub> = -20 to +80 °C)

Manufacturer	Product Name	Frequency (MHz)	Recommended Oscillation Circuit Constant		Oscillation Voltage Range	
			C1 (pF)	C2 (pF)	MIN. (V)	MAX. (V)
Kyocera Corp.	FBRC4.00A	4.00	33	33	1.8	5.5
	FBRC4.00B	4.00	Built-in	Built-in	1.8	5.5
	KBR-4.00MSB	4.00	33	33	1.8	5.5
	KBR-4.00MKC	4.00	Built-in	Built-in	1.8	5.5
	KBR-8M	8.00	33	33	2.7	5.5
	KBR-10M	10.00	33	33	2.7	5.5

**Caution** The oscillation circuit constants and oscillation voltage range indicate conditions for stable oscillation but do not guarantee the accuracy of the oscillation frequency. If the application circuit requires accuracy of the oscillation frequency, it is necessary to set the oscillation frequency of the resonator in the application circuit. For this, it is necessary to directly contact manufacturer of the resonator being used.

**DC Characteristics** (T<sub>A</sub> = -40 to +85 °C, V<sub>DD</sub> = 1.8 to 5.5 V)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit	
Input voltage high	V <sub>IH1</sub>	P10 to P17, P21, P23, P30 to P32, P35 to P37, P40 to P47, P50 to P57, P64 to 67	V <sub>DD</sub> = 2.7 to 5.5 V	0.7 V <sub>DD</sub>		V <sub>DD</sub>	V
				0.8 V <sub>DD</sub>		V <sub>DD</sub>	V
	V <sub>IH2</sub>	P00 to P03, P20, P22, P24 to P27, P33, P34, $\overline{\text{RESET}}$	V <sub>DD</sub> = 2.7 to 5.5 V	0.8 V <sub>DD</sub>		V <sub>DD</sub>	V
				0.85 V <sub>DD</sub>		V <sub>DD</sub>	V
	V <sub>IH3</sub>	P60 to P63 (N-ch open-drain)	V <sub>DD</sub> = 2.7 to 5.5 V	0.7 V <sub>DD</sub>		15	V
				0.8 V <sub>DD</sub>		15	V
	V <sub>IH4</sub>	X1, X2	V <sub>DD</sub> = 2.7 to 5.5 V	V <sub>DD</sub> - 0.5		V <sub>DD</sub>	V
				V <sub>DD</sub> - 0.2		V <sub>DD</sub>	V
	V <sub>IH5</sub>	XT1/P04, XT2	4.5 V ≤ V <sub>DD</sub> ≤ 5.5 V	0.8 V <sub>DD</sub>		V <sub>DD</sub>	V
			2.7 V ≤ V <sub>DD</sub> < 4.5 V	0.9 V <sub>DD</sub>		V <sub>DD</sub>	V
1.8 V ≤ V <sub>DD</sub> < 2.7 V <b>Note</b>			0.9 V <sub>DD</sub>		V <sub>DD</sub>	V	
Input voltage low	V <sub>IL1</sub>	P10 to P17, P21, P23, P30 to P32, P35 to P37, P40 to P47, P50 to P57, P64 to 67	V <sub>DD</sub> = 2.7 to 5.5 V	0		0.3 V <sub>DD</sub>	V
				0		0.2 V <sub>DD</sub>	V
	V <sub>IL2</sub>	P00 to P03, P20, P22, P24 to P27, P33, P34, $\overline{\text{RESET}}$	V <sub>DD</sub> = 2.7 to 5.5 V	0		0.2 V <sub>DD</sub>	V
				0		0.15 V <sub>DD</sub>	V
	V <sub>IL3</sub>	P60 to P63	4.5 V ≤ V <sub>DD</sub> ≤ 5.5 V	0		0.3 V <sub>DD</sub>	V
			2.7 V ≤ V <sub>DD</sub> < 4.5 V	0		0.2 V <sub>DD</sub>	V
				0		0.1 V <sub>DD</sub>	V
	V <sub>IL4</sub>	X1, X2	V <sub>DD</sub> = 2.7 to 5.5 V	0		0.4	V
				0		0.2	V
	V <sub>IL5</sub>	XT1/P04, XT2	4.5 V ≤ V <sub>DD</sub> ≤ 5.5 V	0		0.2 V <sub>DD</sub>	V
2.7 V ≤ V <sub>DD</sub> < 4.5 V			0		0.1 V <sub>DD</sub>	V	
1.8 V ≤ V <sub>DD</sub> < 2.7 V <b>Note</b>			0		0.1 V <sub>DD</sub>	V	
Output voltage high	V <sub>OH1</sub>	V <sub>DD</sub> = 4.5 to 5.5 V, I <sub>OH</sub> = -1 mA	V <sub>DD</sub> - 1.0			V	
		I <sub>OH</sub> = -100 μA	V <sub>DD</sub> - 0.5			V	
Output voltage low	V <sub>OL1</sub>	P50 to P57, P60 to P63	V <sub>DD</sub> = 4.5 to 5.5 V, I <sub>OL</sub> = 15 mA		0.4	2.0	V
		P01 to P03, P10 to P17, P20 to P27 P30 to P37, P40 to P47, P64 to P67	V <sub>DD</sub> = 4.5 to 5.5 V, I <sub>OL</sub> = 1.6 mA			0.4	V
	V <sub>OL2</sub>	SB0, SB1, $\overline{\text{SCK0}}$	V <sub>DD</sub> = 4.5 to 5.5 V, open-drain pulled-up (R = 1 KΩ)			0.2 V <sub>DD</sub>	V
	V <sub>OL3</sub>	I <sub>OL</sub> = 400 μA				0.5	V

**Note** When using XT1/P04 as P04, input the inverse of P04 to XT2 using an inverter.

**Remark** The characteristics of a dual-function pin and a port pin are the same unless specified otherwise.



**DC Characteristics** ( $T_A = -40$  to  $+85$  °C,  $V_{DD} = 1.8$  to  $5.5$  V)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit	
Input leakage current high	I <sub>LIH1</sub>	$V_{IN} = V_{DD}$			3	μA	
							P00 to P03, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60 to P67, $\overline{RESET}$
	I <sub>LIH2</sub>				20	μA	
	I <sub>LIH3</sub>	$V_{IN} = 15$ V			80	μA	
Input leakage current low	I <sub>LIL1</sub>	$V_{IN} = 0$ V			-3	μA	
							P00 to P03, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60 to P67, $\overline{RESET}$
	I <sub>LIL2</sub>						
	I <sub>LIL3</sub>				-3 <b>Note</b>	μA	
Output leakage current high	I <sub>LOH1</sub>	$V_{OUT} = V_{DD}$			3	μA	
Output leakage current low	I <sub>LOL</sub>	$V_{OUT} = 0$ V			-3	μA	
Mask option pull-up resistor	R1	$V_{IN} = 0$ V, P60 to P63	20	40	90	kΩ	
Software pull-up resistor	R2	$V_{IN} = 0$ V, P01 to P03, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60 to P67	15	40	90	kΩ	

**Note** For P60 to P63, if pull-up resistor is not provided (specifiable by mask option) a low-level input leak current of -200 μA (MAX.) flows only during the 3 clocks (no-wait time) after an instruction has been executed to read out port 6 (P6) or port mode register 6 (PM6). Outside the period of 3 clocks following execution a read-out instruction, the current is -3 μA (MAX.).

**Remark** The characteristics of a dual-function pin and a port pin are the same unless specified otherwise.

**DC Characteristics** ( $T_A = -40$  to  $+85$  °C,  $V_{DD} = 1.8$  to  $5.5$  V)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit	
Supply current <b>Note 1</b>	I <sub>DD1</sub>	10.00 MHz crystal oscillation operation mode	$V_{DD} = 5.0\text{ V} \pm 10\%$ <b>Note 2</b>		9.0	18.0	mA
			$V_{DD} = 3.0\text{ V} \pm 10\%$ <b>Note 3</b>		1.3	2.6	mA
	I <sub>DD2</sub>	10.00 MHz crystal oscillation HALT mode	$V_{DD} = 5.0\text{ V} \pm 10\%$ <b>Note 2</b>		2.4	4.8	mA
			$V_{DD} = 3.0\text{ V} \pm 10\%$ <b>Note 3</b>		1.2	2.4	mA
	I <sub>DD3</sub>	32.768 kHz crystal oscillation operation mode <b>Note 4</b>	$V_{DD} = 5.0\text{ V} \pm 10\%$		60	120	μA
			$V_{DD} = 3.0\text{ V} \pm 10\%$		35	70	μA
			$V_{DD} = 2.0\text{ V} \pm 10\%$		24	48	μA
	I <sub>DD4</sub>	32.768 kHz crystal oscillation HALT mode <b>Note 4</b>	$V_{DD} = 5.0\text{ V} \pm 10\%$		25	50	μA
			$V_{DD} = 3.0\text{ V} \pm 10\%$		5	15	μA
			$V_{DD} = 2.0\text{ V} \pm 10\%$		2	10	μA
	I <sub>DD5</sub>	XT1 = $V_{DD}$ STOP mode when using feedback resistor	$V_{DD} = 5.0\text{ V} \pm 10\%$		1	30	μA
			$V_{DD} = 3.0\text{ V} \pm 10\%$		0.5	10	μA
$V_{DD} = 2.0\text{ V} \pm 10\%$				0.3	10	μA	
I <sub>DD6</sub>	XT1 = $V_{DD}$ STOP mode when not using feedback resistor	$V_{DD} = 5.0\text{ V} \pm 10\%$		0.1	30	μA	
		$V_{DD} = 3.0\text{ V} \pm 10\%$		0.05	10	μA	
		$V_{DD} = 2.0\text{ V} \pm 10\%$		0.05	10	μA	

- Notes**
- 1.** This current excludes the  $A_{VREF}$  current, port current, and current which flows in the built-in pull-down resistor.
  - 2.** When operating at high-speed mode (when the processor clock control register (PCC) is set to 00H)
  - 3.** When operating at low-speed mode (when the PCC is set to 04H)
  - 4.** When main system clock stopped.

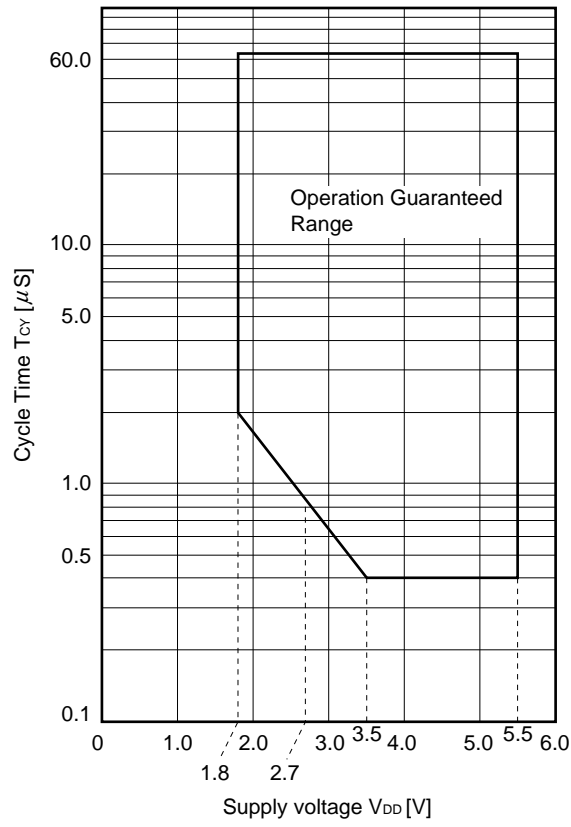
AC Characteristics

(1) Basic Operation (T<sub>A</sub> = -40 to +85 °C, V<sub>DD</sub> = 1.8 to 5.5 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Cycle time (Min. instruction execution time)	T <sub>CY</sub>	Operating on main system clock	3.5 V ≤ V <sub>DD</sub> ≤ 5.5 V	0.4		64	μs
			2.7 V ≤ V <sub>DD</sub> < 3.5 V	0.8		64	μs
			1.8 V ≤ V <sub>DD</sub> < 2.7 V	2.0		64	μs
		Operating on subsystem clock		40	122	125	μs
TI0 input frequency	t <sub>TIH0</sub>	3.5 V ≤ V <sub>DD</sub> ≤ 5.5 V		2/f <sub>sam</sub> + 0.1 <b>Note</b>			μs
	t <sub>TIL0</sub>	2.7 V ≤ V <sub>DD</sub> < 3.5 V		2/f <sub>sam</sub> + 0.2 <b>Note</b>			μs
		1.8 V ≤ V <sub>DD</sub> < 2.7 V		2/f <sub>sam</sub> + 0.5 <b>Note</b>			μs
TI1, TI2 input frequency	f <sub>TI1</sub>	V <sub>DD</sub> = 4.5 to 5.5 V		0		4	MHz
				0		275	kHz
TI1, TI2 input high/low-level width	t <sub>TIH1</sub>	V <sub>DD</sub> = 4.5 to 5.5 V		100			ns
	t <sub>TIL1</sub>			1.8			μs
Interrupt request input high/low-level width	t <sub>INTH</sub>	INTP0	3.5 V ≤ V <sub>DD</sub> ≤ 5.5 V	2/f <sub>sam</sub> + 0.1 <b>Note</b>			μs
			2.7 V ≤ V <sub>DD</sub> < 3.5 V	2/f <sub>sam</sub> + 0.2 <b>Note</b>			μs
			1.8 V ≤ V <sub>DD</sub> < 2.7 V	2/f <sub>sam</sub> + 0.5 <b>Note</b>			μs
	t <sub>INTL</sub>	INTP1 to INTP3, KR0 to KR7	V <sub>DD</sub> = 2.7 to 5.5 V		10		μs
					20		μs
RESET low level width	t <sub>RSL</sub>	V <sub>DD</sub> = 2.7 to 5.5 V		10		μs	
				20		μs	

**Note** In combination with bits 0 (SCS0) and 1 (SCS1) of sampling clock select register (SCS), selection of f<sub>sam</sub> is possible between f<sub>x</sub>/2<sup>N+1</sup>, f<sub>x</sub>/64 and f<sub>x</sub>/128 (when N= 0 to 4).

T<sub>CY</sub> vs V<sub>DD</sub> (At main system clock operation)



(2) Read/Write Operation ( $T_A = -40$  to  $+85$  °C,  $V_{DD} = 2.7$  to  $5.5$  V)

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
ASTB high-level width	$t_{ASTH}$		$0.5t_{CY}$		ns
Address setup time	$t_{ADS}$		$0.5t_{CY} - 30$		ns
Address hold time	$t_{ADH}$		50		ns
Data input time from address	$t_{ADD1}$			$(2.5 + 2n) t_{CY} - 50$	ns
	$t_{ADD2}$			$(3 + 2n) t_{CY} - 100$	ns
Data input time from $\overline{RD}\downarrow$	$t_{RDD1}$			$(1 + 2n) t_{CY} - 25$	ns
	$t_{RDD2}$			$(2.5 + 2n) t_{CY} - 100$	ns
Read data hold time	$t_{RDH}$		0		ns
$\overline{RD}$ low-level width	$t_{RDL1}$		$(1.5 + 2n) t_{CY} - 20$		ns
	$t_{RDL2}$		$(2.5 + 2n) t_{CY} - 20$		ns
$\overline{WAIT}\downarrow$ input time from $\overline{RD}\downarrow$	$t_{RDWT1}$			$0.5t_{CY}$	ns
	$t_{RDWT2}$			$1.5t_{CY}$	ns
$\overline{WAIT}\downarrow$ input time from $\overline{WR}\downarrow$	$t_{WRWT}$			$0.5t_{CY}$	ns
$\overline{WAIT}$ low-level width	$t_{WTL}$		$(0.5 + 2n) t_{CY} + 10$	$(2 + 2n) t_{CY}$	ns
Write data setup time	$t_{WDS}$		100		ns
Write data hold time	$t_{WDH}$	Load resistor $\geq 5$ k $\Omega$	20		ns
$\overline{WR}$ low-level width	$t_{WRL1}$		$(2.5 + 2n) t_{CY} - 20$		ns
$\overline{RD}\downarrow$ delay time from $\overline{ASTB}\downarrow$	$t_{ASTRD}$		$0.5t_{CY} - 30$		ns
$\overline{WR}\downarrow$ delay time from $\overline{ASTB}\downarrow$	$t_{ASTWR}$		$1.5t_{CY} - 30$		ns
$\overline{ASTB}\uparrow$ delay time from $\overline{RD}\uparrow$ in external fetch	$t_{RDAST}$		$t_{CY} - 10$	$t_{CY} + 40$	ns
Address hold time from $\overline{RD}\uparrow$ in external fetch	$t_{RDADH}$		$t_{CY}$	$t_{CY} + 50$	ns
Write data output time from $\overline{RD}\uparrow$	$t_{RDWD}$	$V_{DD} = 4.5$ to $5.5$ V	$0.5t_{CY} + 5$	$0.5t_{CY} + 30$	ns
			$0.5t_{CY} + 15$	$0.5t_{CY} + 90$	ns
Write data output time from $\overline{WR}\downarrow$	$t_{WRWD}$	$V_{DD} = 4.5$ to $5.5$ V	5	30	ns
			15	90	ns
Address hold time from $\overline{WR}\uparrow$	$t_{WRADH}$	$V_{DD} = 4.5$ to $5.5$ V	$t_{CY}$	$t_{CY} + 60$	ns
			$t_{CY}$	$t_{CY} + 100$	ns
$\overline{RD}\uparrow$ delay time from $\overline{WAIT}\uparrow$	$t_{WTRD}$		$0.5t_{CY}$	$2.5t_{CY} + 80$	ns
$\overline{WR}\uparrow$ delay time from $\overline{WAIT}\uparrow$	$t_{WTWR}$		$0.5t_{CY}$	$2.5t_{CY} + 80$	ns

- Remarks**
- $t_{CY} = T_{CY}/4$
  - n indicates number of waits.

(3) Serial Interface (T<sub>A</sub> = -40 to +85 °C, V<sub>DD</sub> = 1.8 to 5.5 V)

(a) Serial Interface Channel 0

(i) 3-wire serial I/O mode ( $\overline{\text{SCK0}}$ ... Internal clock output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{\text{SCK0}}$ cycle time	t <sub>KCY1</sub>	4.5 V ≤ V <sub>DD</sub> ≤ 5.5 V	800			ns
		2.7 V ≤ V <sub>DD</sub> < 4.5 V	1600			ns
		2.0 V ≤ V <sub>DD</sub> < 2.7 V	3200			ns
			4800			ns
$\overline{\text{SCK0}}$ high/low-level width	t <sub>KH1</sub>	V <sub>DD</sub> = 4.5 to 5.5 V	t <sub>KCY1</sub> /2 - 50			ns
	t <sub>KL1</sub>		t <sub>KCY1</sub> /2 - 100			ns
SIO setup time (to $\overline{\text{SCK0}}\uparrow$ )	t <sub>SIK1</sub>	4.5 V ≤ V <sub>DD</sub> ≤ 5.5 V	100			ns
		2.7 V ≤ V <sub>DD</sub> < 4.5 V	150			ns
		2.0 V ≤ V <sub>DD</sub> < 2.7 V	300			ns
			400			ns
SIO hold time (from $\overline{\text{SCK0}}\uparrow$ )	t <sub>KS1</sub>		400			ns
SO0 output delay time from $\overline{\text{SCK0}}\downarrow$	t <sub>KSO1</sub>	C = 100 pF <b>Note</b>			300	ns

**Note** C is the load capacitance of  $\overline{\text{SCK0}}$  and SO0 output line.

(ii) 3-wire serial I/O mode ( $\overline{\text{SCK0}}$ ... External clock input)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{\text{SCK0}}$ cycle time	t <sub>KCY2</sub>	4.5 V ≤ V <sub>DD</sub> ≤ 5.5 V	800			ns
		2.7 V ≤ V <sub>DD</sub> < 4.5 V	1600			ns
		2.0 V ≤ V <sub>DD</sub> < 2.7 V	3200			ns
			4800			ns
$\overline{\text{SCK0}}$ high/low-level width	t <sub>KH2</sub>	4.5 V ≤ V <sub>DD</sub> ≤ 5.5 V	400			ns
		2.7 V ≤ V <sub>DD</sub> < 4.5 V	800			ns
	t <sub>KL2</sub>	2.0 V ≤ V <sub>DD</sub> < 2.7 V	1600			ns
			2400			ns
SIO setup time (to $\overline{\text{SCK0}}\uparrow$ )	t <sub>SIK2</sub>	V <sub>DD</sub> = 2.0 to 5.5 V	100			ns
			150			ns
SIO hold time (from $\overline{\text{SCK0}}\uparrow$ )	t <sub>KS2</sub>		400			ns
SO0 output delay time from $\overline{\text{SCK0}}\downarrow$	t <sub>KSO2</sub>	C = 100 pF <b>Note</b>	V <sub>DD</sub> = 2.0 to 5.5 V		300	ns
					500	ns
$\overline{\text{SCK0}}$ rise, fall time	t <sub>r2</sub> t <sub>f2</sub>	When external device expansion function is used			160	ns
		When external device expansion function is not used	When 16-bit timer output function is used		700	ns
			When 16-bit timer output function is not used		1000	ns

**Note** C is the load capacitance of SO0 output line.

(iii) 2-wire serial I/O mode ( $\overline{\text{SCK0}}$ ... Internal clock output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit	
$\overline{\text{SCK0}}$ cycle time	$t_{\text{KCY3}}$	R = 1 kΩ <b>Note</b> C = 100 pF	$2.7 \text{ V} \leq V_{\text{DD}} \leq 5.5 \text{ V}$	1600			ns
			$2.0 \text{ V} \leq V_{\text{DD}} < 2.7 \text{ V}$	3200			ns
				4800			ns
$\overline{\text{SCK0}}$ high-level width	$t_{\text{KH3}}$	$V_{\text{DD}} = 2.7 \text{ to } 5.5 \text{ V}$	$t_{\text{KCY3}}/2 - 160$			ns	
			$t_{\text{KCY3}}/2 - 190$			ns	
$\overline{\text{SCK0}}$ low-level width	$t_{\text{KL3}}$	$V_{\text{DD}} = 4.5 \text{ to } 5.5 \text{ V}$	$t_{\text{KCY3}}/2 - 50$			ns	
			$t_{\text{KCY3}}/2 - 100$			ns	
SB0, SB1 setup time (to $\overline{\text{SCK0}}\uparrow$ )	$t_{\text{SIK3}}$	$4.5 \text{ V} \leq V_{\text{DD}} \leq 5.5 \text{ V}$	300			ns	
			$2.7 \text{ V} \leq V_{\text{DD}} < 4.5 \text{ V}$	350			ns
			$2.0 \text{ V} \leq V_{\text{DD}} < 2.7 \text{ V}$	400			ns
				500			ns
SB0, SB1 hold time (from $\overline{\text{SCK0}}\uparrow$ )	$t_{\text{KS13}}$		600			ns	
SB0, SB1 output delay time from $\overline{\text{SCK0}}\downarrow$	$t_{\text{KSO3}}$		0		300	ns	

**Note** R and C are the load resistance and load capacitance of the  $\overline{\text{SCK0}}$ , SB0 and SB1 output line.

(iv) 2-wire serial I/O mode ( $\overline{\text{SCK0}}$ ... External clock input)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{\text{SCK0}}$ cycle time	tkCY4	2.7 V ≤ V <sub>DD</sub> ≤ 5.5 V		1600			ns
		2.0 V ≤ V <sub>DD</sub> < 2.7 V		3200			ns
				4800			ns
$\overline{\text{SCK0}}$ high-level width	tkH4	2.7 V ≤ V <sub>DD</sub> ≤ 5.5 V		650			ns
		2.0 V ≤ V <sub>DD</sub> < 2.7 V		1300			ns
				2100			ns
$\overline{\text{SCK0}}$ low-level width	tkL4	2.7 V ≤ V <sub>DD</sub> ≤ 5.5 V		800			ns
		2.0 V ≤ V <sub>DD</sub> < 2.7 V		1600			ns
				2400			ns
SB0, SB1 setup time (to $\overline{\text{SCK0}}\uparrow$ )	tSIK4	V <sub>DD</sub> = 2.0 to 5.5 V		100			ns
				150			ns
SB0, SB1 hold time (from $\overline{\text{SCK0}}\uparrow$ )	tkS4			tkCY4/2			ns
SB0, SB1 output delay time from $\overline{\text{SCK0}}\downarrow$	tkSO4	R = 1 kΩ, C = 100 pF <b>Note</b>	4.5 V ≤ V <sub>DD</sub> ≤ 5.5 V	0		300	ns
			2.0 V ≤ V <sub>DD</sub> < 4.5 V	0		500	ns
				0		800	ns
$\overline{\text{SCK0}}$ rise, fall time	tr4 tf4	When external device expansion function is used				160	ns
		When external device expansion function is not used	When 16-bit timer output function is used			700	ns
			When 16-bit timer output function is not used			1000	ns

**Note** R and C are the load resistance and load capacitance of the SB0 and SB1 output line.



(v) I<sup>2</sup>C bus mode (SCK0... Internal clock output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit	
SCL cycle time	t <sub>KCY5</sub>	R = 1 kΩ <b>Note</b> C = 100 pF	2.7 V ≤ V <sub>DD</sub> ≤ 5.5 V	10			μs
			2.0 V ≤ V <sub>DD</sub> < 2.7 V	20			μs
				30			μs
SCL high-level width	t <sub>KH5</sub>	V <sub>DD</sub> = 2.7 to 5.5 V	t <sub>KCY5</sub> - 160				ns
			t <sub>KCY5</sub> - 190				ns
SCL low-level width	t <sub>KL5</sub>	V <sub>DD</sub> = 4.5 to 5.5 V	t <sub>KCY5</sub> - 50				ns
			t <sub>KCY5</sub> - 100				ns
SDA0, SDA1 setup time (to SCL↑)	t <sub>SIK5</sub>	2.7 V ≤ V <sub>DD</sub> ≤ 5.5 V	200				ns
			2.0 V ≤ V <sub>DD</sub> ≤ 2.7 V	300			ns
				400			ns
SDA0, SDA1 hold time (from SCL↓)	t <sub>KSI5</sub>		0			ns	
SDA0, SDA1 output delay time from SCL↓	t <sub>KSO5</sub>	4.5 V ≤ V <sub>DD</sub> ≤ 5.5 V	0		300		ns
		2.0 V ≤ V <sub>DD</sub> < 4.5 V	0		500		ns
			0		600		ns
SDA0, SDA1↓ from SCL↑ or SDA0, SDA1↑ from SCL↑	t <sub>KSB</sub>		200			ns	
SCL↓ from SDA0, SDA1↓	t <sub>SBK</sub>	V <sub>DD</sub> = 2.0 to 5.5 V	400				ns
			500				ns
SDA0, SDA1 high-level width	t <sub>SBH</sub>		500			ns	

**Note** R and C are the load resistance and load capacitance of the SCL, SDA0 and SDA1 output line.

(vi) I<sup>2</sup>C bus mode (SCK0... External clock output)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
SCL cycle time	t <sub>KCY6</sub>			1000			ns
SCL high/low-level width	t <sub>KH6</sub> t <sub>KL6</sub>	V <sub>DD</sub> = 2.0 to 5.5 V		400			ns
				600			ns
SDA0, SDA1 setup time (to SCL↑)	t <sub>SIK6</sub>	V <sub>DD</sub> = 2.0 to 5.5 V		200			ns
				300			ns
SDA0, SDA1 hold time (from SCL↓)	t <sub>KSI6</sub>			0			ns
SDA0, SDA1 output delay time from SCL↓	t <sub>KSO6</sub>	R = 1 kΩ, C = 100 pF <b>Note</b>	4.5 V ≤ V <sub>DD</sub> ≤ 5.5 V	0		300	ns
			2.0 V ≤ V <sub>DD</sub> < 4.5 V	0		500	ns
				0		600	ns
SDA0, SDA1↓ from SCL↑ or SDA0, SDA1↑ from SCL↑	t <sub>KSB</sub>			200			ns
SCL↓ from SDA0, SDA1	t <sub>SBK</sub>	V <sub>DD</sub> = 2.0 to 5.5 V		400			ns
				500			ns
SDA0, SDA1 high-level width	t <sub>SBH</sub>	V <sub>DD</sub> = 2.0 to 5.5 V		500			ns
				800			ns
SCL rise, fall time	t <sub>R6</sub> t <sub>F6</sub>	When external device expansion function is used				160	ns
		When external device expansion function is not used	When 16-bit timer output function is used			700	ns
			When 16-bit timer output function is not used			1000	ns

**Note** R and C are the load resistance and load capacitance of the SB0 and SB1 output line.

(b) Serial Interface Channel 1

(i) 3-wire serial I/O mode (SCK1... Internal clock output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
SCK1 cycle time	t <sub>KCY7</sub>	4.5 V ≤ V <sub>DD</sub> ≤ 5.5 V	800			ns
		2.7 V ≤ V <sub>DD</sub> < 4.5 V	1600			ns
		2.0 V ≤ V <sub>DD</sub> < 2.7 V	3200			ns
			4800			ns
SCK1 high/low-level width	t <sub>KH7</sub>	V <sub>DD</sub> = 4.5 to 5.5 V	t <sub>KCY7</sub> /2 – 50			ns
	t <sub>KL7</sub>		t <sub>KCY7</sub> /2 – 100			ns
SI1 setup time (to SCK1↑)	t <sub>SIK7</sub>	4.5 V ≤ V <sub>DD</sub> ≤ 5.5 V	100			ns
		2.7 V ≤ V <sub>DD</sub> < 4.5 V	150			ns
		2.0 V ≤ V <sub>DD</sub> < 2.7 V	300			ns
			400			ns
SI1 hold time (from SCK1↑)	t <sub>KS17</sub>		400			ns
SO1 output delay time from SCK1↓	t <sub>KSO7</sub>	C = 100 pF <b>Note</b>			300	ns

**Note** C is the load capacitance of SCK1 and SO1 output line.

(ii) 3-wire serial I/O mode (SCK1... External clock input)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
SCK1 cycle time	t <sub>KCY8</sub>	4.5 V ≤ V <sub>DD</sub> ≤ 5.5 V	800			ns
		2.7 V ≤ V <sub>DD</sub> < 4.5 V	1600			ns
		2.0 V ≤ V <sub>DD</sub> < 2.7 V	3200			ns
			4800			ns
SCK1 high/low-level width	t <sub>KH8</sub> t <sub>KL8</sub>	4.5 V ≤ V <sub>DD</sub> ≤ 5.5 V	400			ns
		2.7 V ≤ V <sub>DD</sub> < 4.5 V	800			ns
		2.0 V ≤ V <sub>DD</sub> < 2.7 V	1600			ns
			2400			ns
SI1 setup time (to SCK1↑)	t <sub>SIK8</sub>	V <sub>DD</sub> = 2.0 to 5.5 V	100			ns
			150			ns
SI1 hold time (from SCK1↑)	t <sub>KS18</sub>		400			ns
SO0 output delay time from SCK1↓	t <sub>KSO8</sub>	C = 100 pF <b>Note</b> V <sub>DD</sub> = 2.0 to 5.5 V			300	ns
					500	ns
SCK1 rise, fall time	t <sub>R8</sub> t <sub>F8</sub>	When external device expansion function is used			160	ns
		When external device expansion function is not used	When 16-bit timer output function is used		700	ns
			When 16-bit timer output function is not used		1000	ns

**Note** C is the load capacitance of SO1 output line.

(iii) 3-wire serial I/O mode with automatic transmit/receive function ( $\overline{\text{SCK1}}$ ... Internal clock output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{\text{SCK1}}$ cycle time	$t_{\text{KCY9}}$	$4.5 \text{ V} \leq V_{\text{DD}} \leq 5.5 \text{ V}$	800			ns
		$2.7 \text{ V} \leq V_{\text{DD}} < 4.5 \text{ V}$	1600			ns
		$2.0 \text{ V} \leq V_{\text{DD}} < 2.7 \text{ V}$	3200			ns
			4800			ns
$\overline{\text{SCK1}}$ high/low-level width	$t_{\text{KH9}}$	$V_{\text{DD}} = 4.5 \text{ to } 5.5 \text{ V}$	$t_{\text{KCY9}}/2 - 50$			ns
	$t_{\text{KL9}}$		$t_{\text{KCY9}}/2 - 100$			ns
SI1 setup time (to $\overline{\text{SCK1}}\uparrow$ )	$t_{\text{SIK9}}$	$4.5 \text{ V} \leq V_{\text{DD}} \leq 5.5 \text{ V}$	100			ns
		$2.7 \text{ V} \leq V_{\text{DD}} < 4.5 \text{ V}$	150			ns
		$2.0 \text{ V} \leq V_{\text{DD}} < 2.7 \text{ V}$	300			ns
			400			ns
SI1 hold time (from $\overline{\text{SCK1}}\uparrow$ )	$t_{\text{KS9}}$		400			ns
SO1 output delay time from $\overline{\text{SCK1}}\downarrow$	$t_{\text{KSO9}}$	$C = 100 \text{ pF}$ <b>Note</b>			300	ns
$\text{STB}\uparrow$ from $\overline{\text{SCK1}}\uparrow$	$t_{\text{SBD}}$		$t_{\text{KCY9}}/2 - 100$		$t_{\text{KCY9}}/2 + 100$	ns
Strobe signal high-level width	$t_{\text{SBW}}$	$2.7 \text{ V} \leq V_{\text{DD}} \leq 5.5 \text{ V}$	$t_{\text{KCY9}} - 30$		$t_{\text{KCY9}} + 30$	ns
		$2.0 \text{ V} \leq V_{\text{DD}} < 2.7 \text{ V}$	$t_{\text{KCY9}} - 60$		$t_{\text{KCY9}} + 60$	ns
			$t_{\text{KCY9}} - 90$		$t_{\text{KCY9}} + 90$	ns
Busy signal setup time (to busy signal detection timing)	$t_{\text{BYS}}$		100			ns
Busy signal hold time (from busy signal detection timing)	$t_{\text{BYH}}$	$4.5 \text{ V} \leq V_{\text{DD}} \leq 5.5 \text{ V}$	100			ns
		$2.7 \text{ V} \leq V_{\text{DD}} < 4.5 \text{ V}$	150			ns
		$2.0 \text{ V} \leq V_{\text{DD}} < 2.7 \text{ V}$	200			ns
			300			ns
$\overline{\text{SCK1}}\downarrow$ from busy inactive	$t_{\text{SPS}}$				$2t_{\text{KCY9}}$	ns

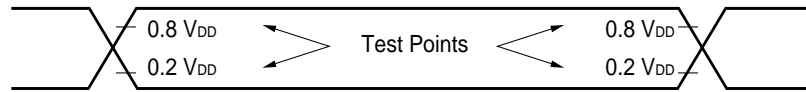
**Note** C is the load capacitance of  $\overline{\text{SCK1}}$  and SO1 output line.

(iv) 3-wire serial I/O mode with automatic transmit/receive function ( $\overline{\text{SCK1}}$ ... External clock input)

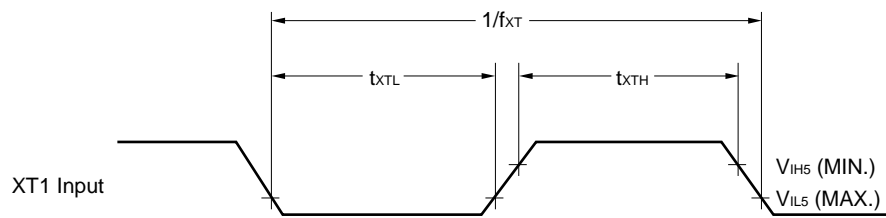
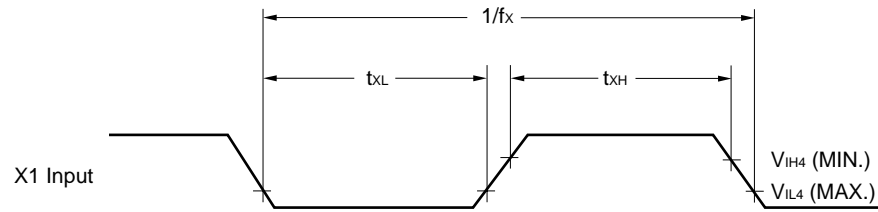
Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{\text{SCK1}}$ cycle time	$t_{\text{KC}10}$	$4.5 \text{ V} \leq V_{\text{DD}} \leq 5.5 \text{ V}$	800			ns
		$2.7 \text{ V} \leq V_{\text{DD}} < 4.5 \text{ V}$	1600			ns
		$2.0 \text{ V} \leq V_{\text{DD}} < 2.7 \text{ V}$	3200			ns
			4800			ns
$\overline{\text{SCK1}}$ high/low-level width	$t_{\text{KH}10},$ $t_{\text{KL}10}$	$4.5 \text{ V} \leq V_{\text{DD}} \leq 5.5 \text{ V}$	400			ns
		$2.7 \text{ V} \leq V_{\text{DD}} < 4.5 \text{ V}$	800			ns
		$2.0 \text{ V} \leq V_{\text{DD}} < 2.7 \text{ V}$	1600			ns
			2400			ns
SI1 setup time (to $\overline{\text{SCK1}}\uparrow$ )	$t_{\text{SIK}10}$	$V_{\text{DD}} = 2.0 \text{ to } 5.5 \text{ V}$	100			ns
			150			ns
SI1 hold time (from $\overline{\text{SCK1}}\uparrow$ )	$t_{\text{KSI}10}$		400			ns
SO1 output delay time from $\overline{\text{SCK1}}\downarrow$	$t_{\text{KSO}10}$	C = 100 pF <b>Note</b> $V_{\text{DD}} = 2.0 \text{ to } 5.5 \text{ V}$			300	ns
					500	ns
$\overline{\text{SCK1}}$ rise, fall time	$t_{\text{R}10}, t_{\text{F}10}$	When external device expansion function is used			160	ns
		When external device expansion function is not used			1000	ns

**Note** C is the load capacitance of the SO1 output line.

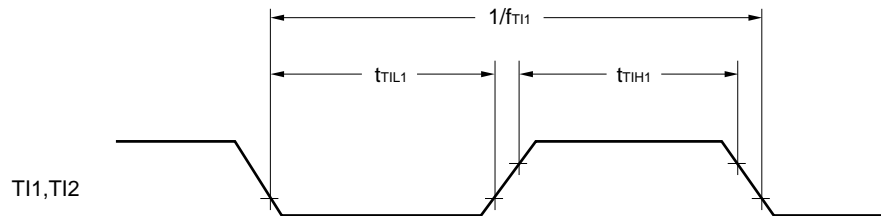
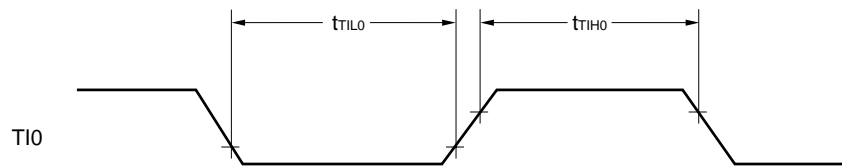
AC Timing Test Point (Excluding X1, XT1 Input)



Clock Timing

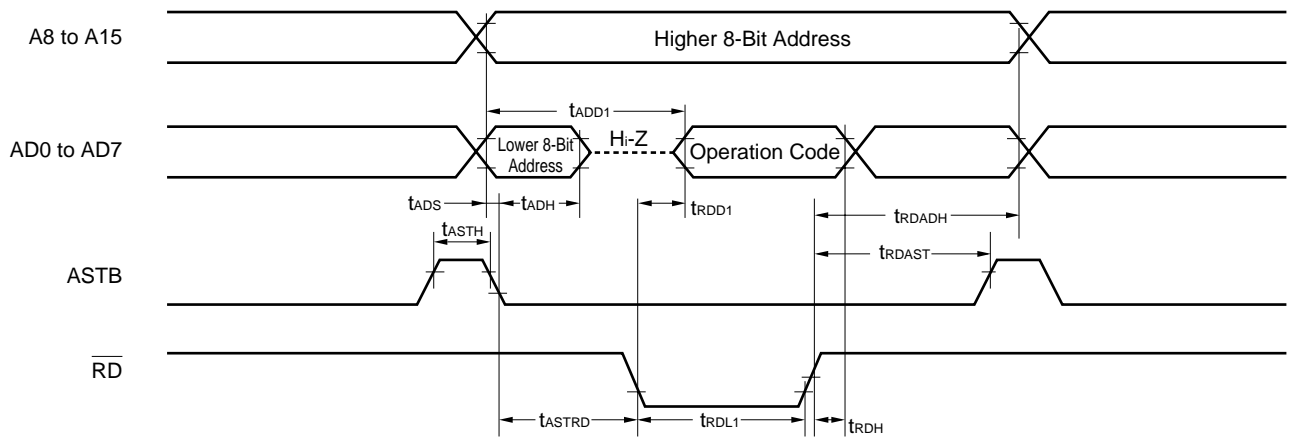


TI Timing

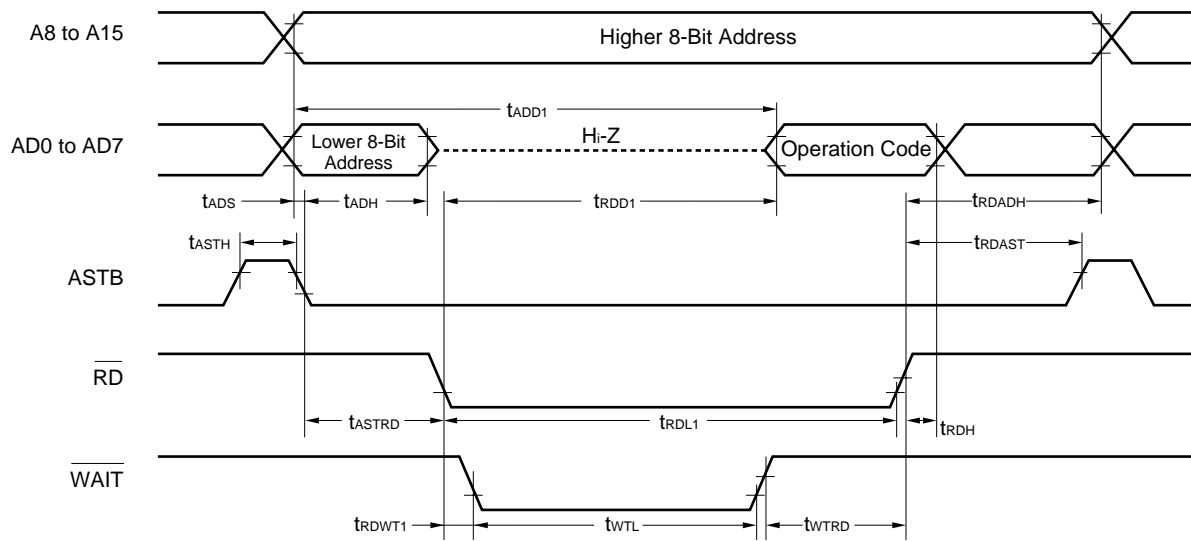


Read/Write Operation

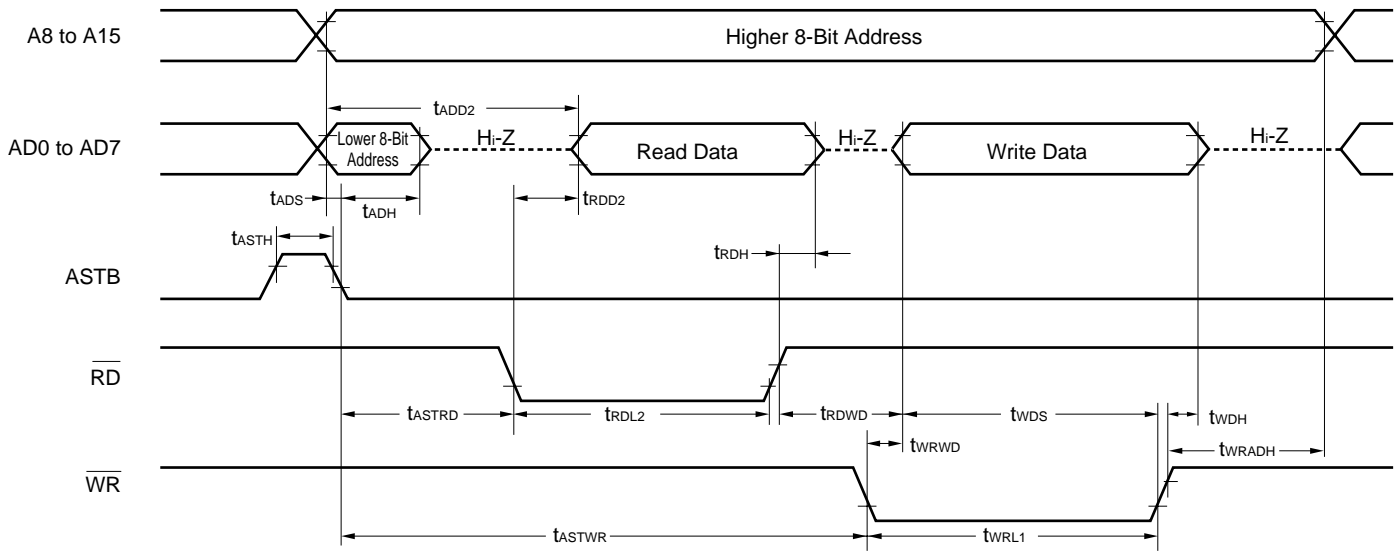
External fetch (No wait):



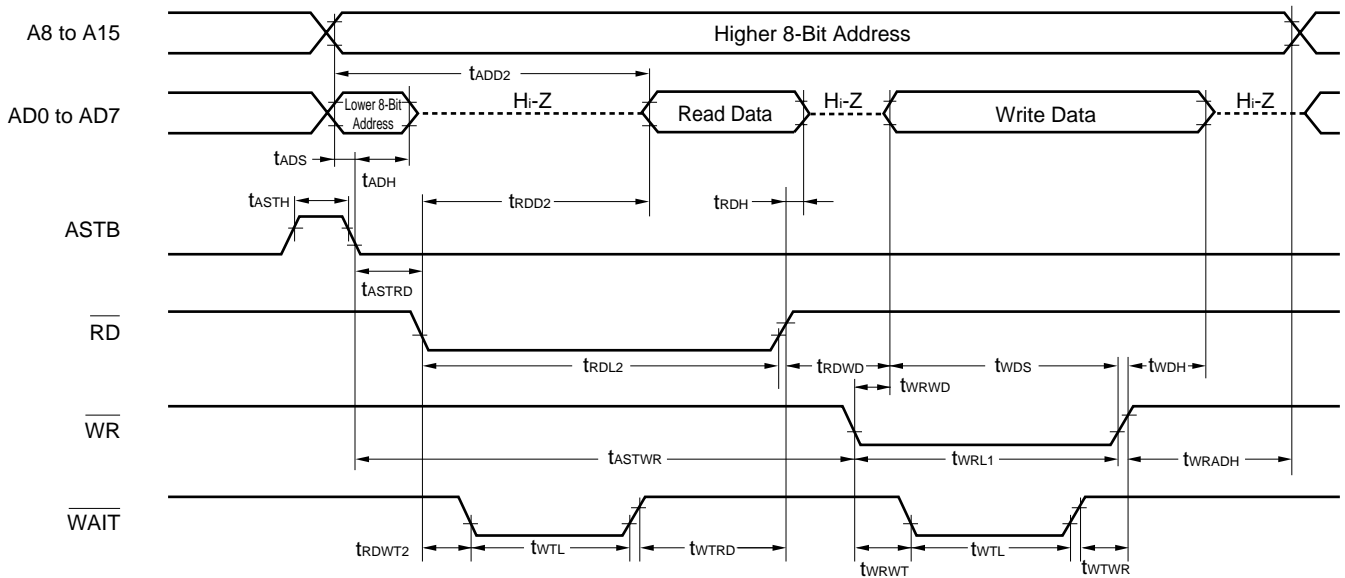
External fetch (Wait insertion):



External data access (No wait):

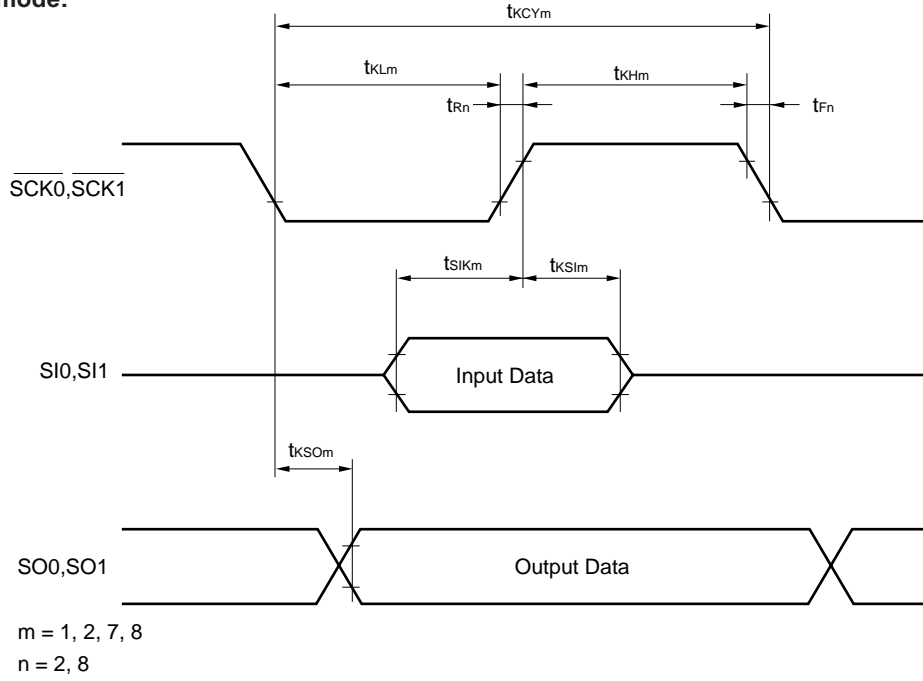


External data access (Wait insertion):

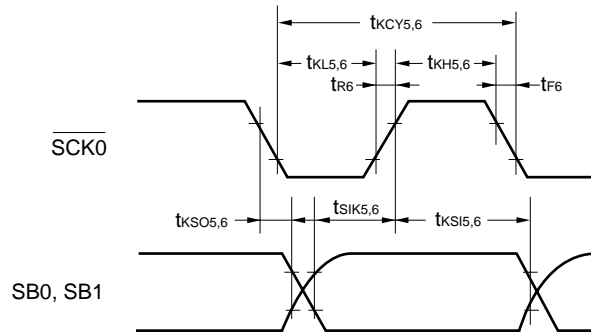




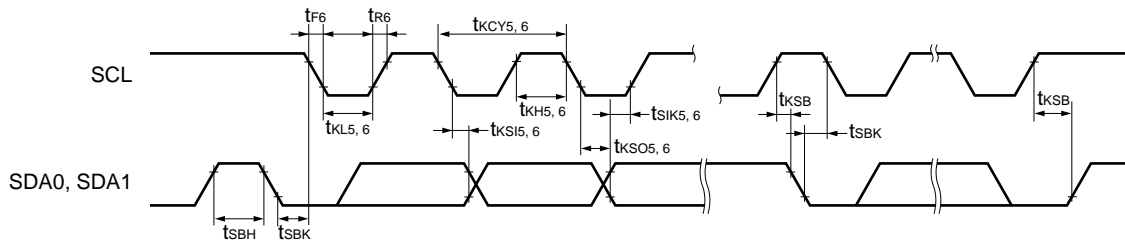
**Serial Transfer Timing**  
**3-wire serial I/O mode:**



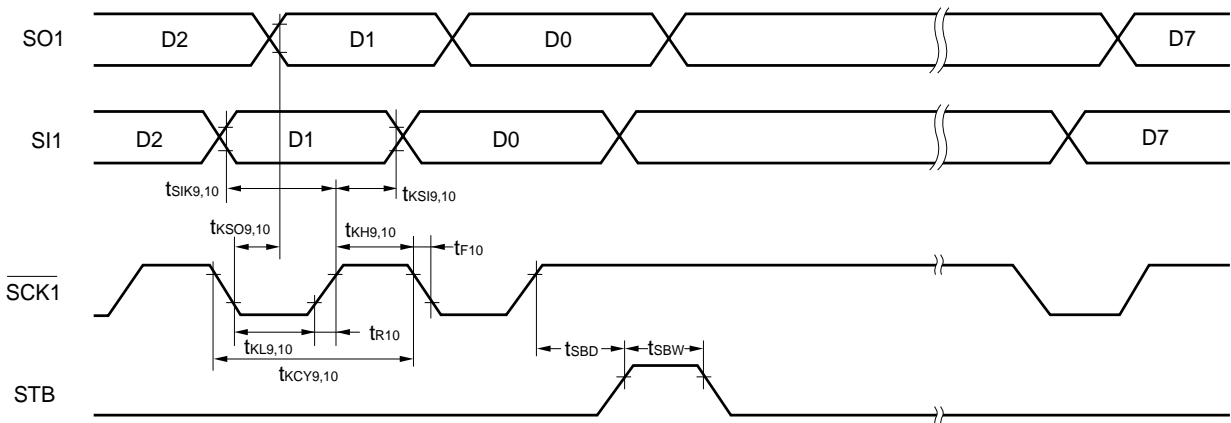
**2-wire serial I/O mode:**



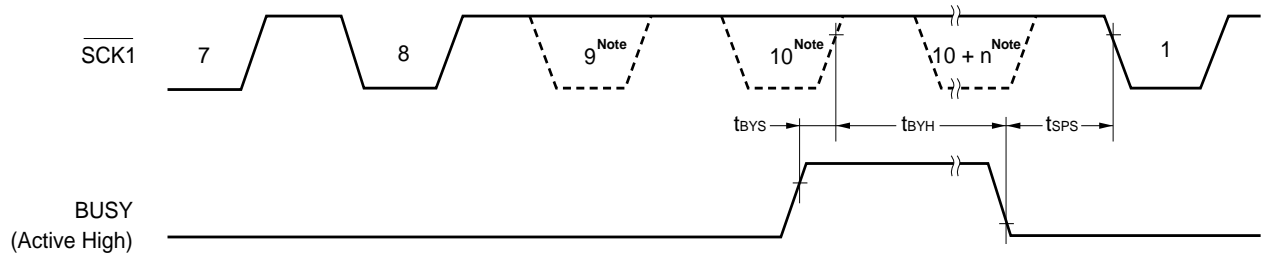
**I<sup>2</sup>C bus mode:**



3-wire serial I/O mode with automatic transmit/receive function:



3-wire serial I/O mode with automatic transmit/receive function (busy processing):



**Note** The signal is not actually driven low here; it is shown as such to indicate the timing.

A/D converter characteristics (T<sub>A</sub> = -40 to +85 °C, AV<sub>DD</sub> = V<sub>DD</sub> = 1.8 to 5.5 V, AV<sub>SS</sub> = V<sub>SS</sub> = 0 V)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Resolution			8	8	8	bit
Overall error <b>Note</b>		2.7 V ≤ AV <sub>REF</sub> ≤ AV <sub>DD</sub>			0.6	%
		1.8 V ≤ AV <sub>REF</sub> < 2.7 V			1.4	%
Conversion time	t <sub>CONV</sub>	2.0 V ≤ AV <sub>DD</sub> ≤ 5.5 V	19.1		200	μs
		1.8 V ≤ AV <sub>DD</sub> < 2.0 V	38.2		200	μs
Sampling time	t <sub>SAMP</sub>		24/f <sub>x</sub>			μs
Analog input voltage	V <sub>IAN</sub>		AV <sub>SS</sub>		AV <sub>REF</sub>	V
Reference voltage	AV <sub>REF</sub>		1.8		AV <sub>DD</sub>	V
AV <sub>REF</sub> resistance	RA <sub>IREF</sub>		4	14		kΩ

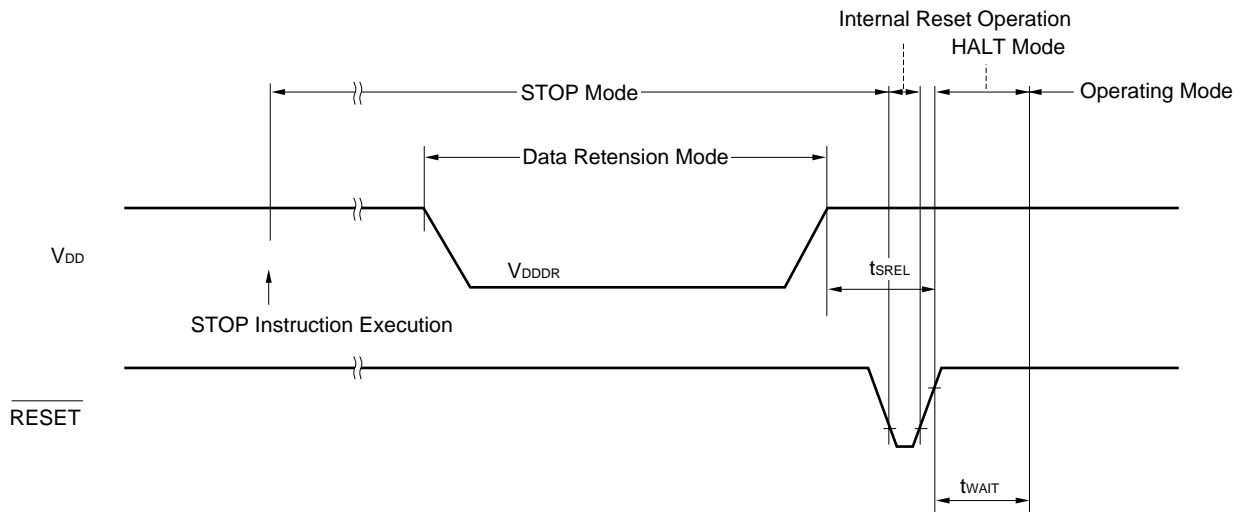
**Note** Overall error excluding quantization error (±1/2 LSB). It is indicated as a ratio to the full-scale value.

**Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics** (T<sub>A</sub> = -40 to +85 °C)

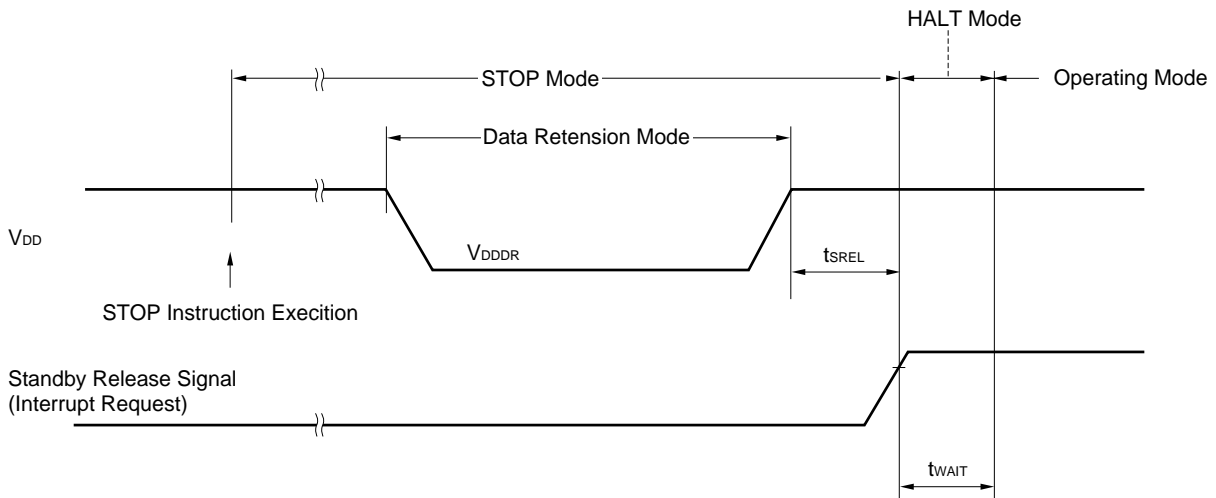
Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V <sub>DDDR</sub>		1.8		5.5	V
Data retention supply current	I <sub>DDDR</sub>	V <sub>DDDR</sub> = 1.8 V Subsystem clock stop and feedback resistor disconnected		0.1	10	μA
Release signal set time	t <sub>SREL</sub>		0			μs
Oscillation stabilization wait time	t <sub>WAIT</sub>	Release by $\overline{\text{RESET}}$		2 <sup>18</sup> /f <sub>x</sub>		ms
		Release by interrupt request		<b>Note</b>		ms

**Note** In combination with bit 0 to bit 2 (OSTS0 to OSTS2) of oscillation stabilization time select register (OSTS), selection of 2<sup>13</sup>/f<sub>x</sub> and 2<sup>15</sup>/f<sub>x</sub> to 2<sup>18</sup>/f<sub>x</sub> is possible.

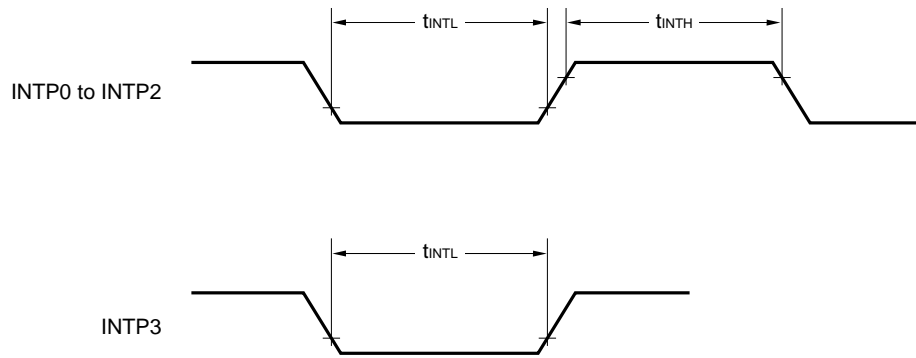
**Data Retention Timing (STOP Mode Release by  $\overline{\text{RESET}}$ )**



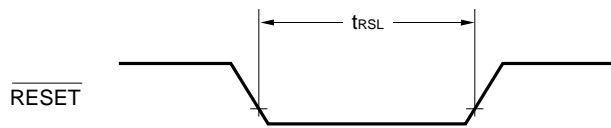
**Data Retention Timing (Standby Release Signal : STOP Mode Release by Interrupt Request Signal)**



**Interrupt Request Input Timing**

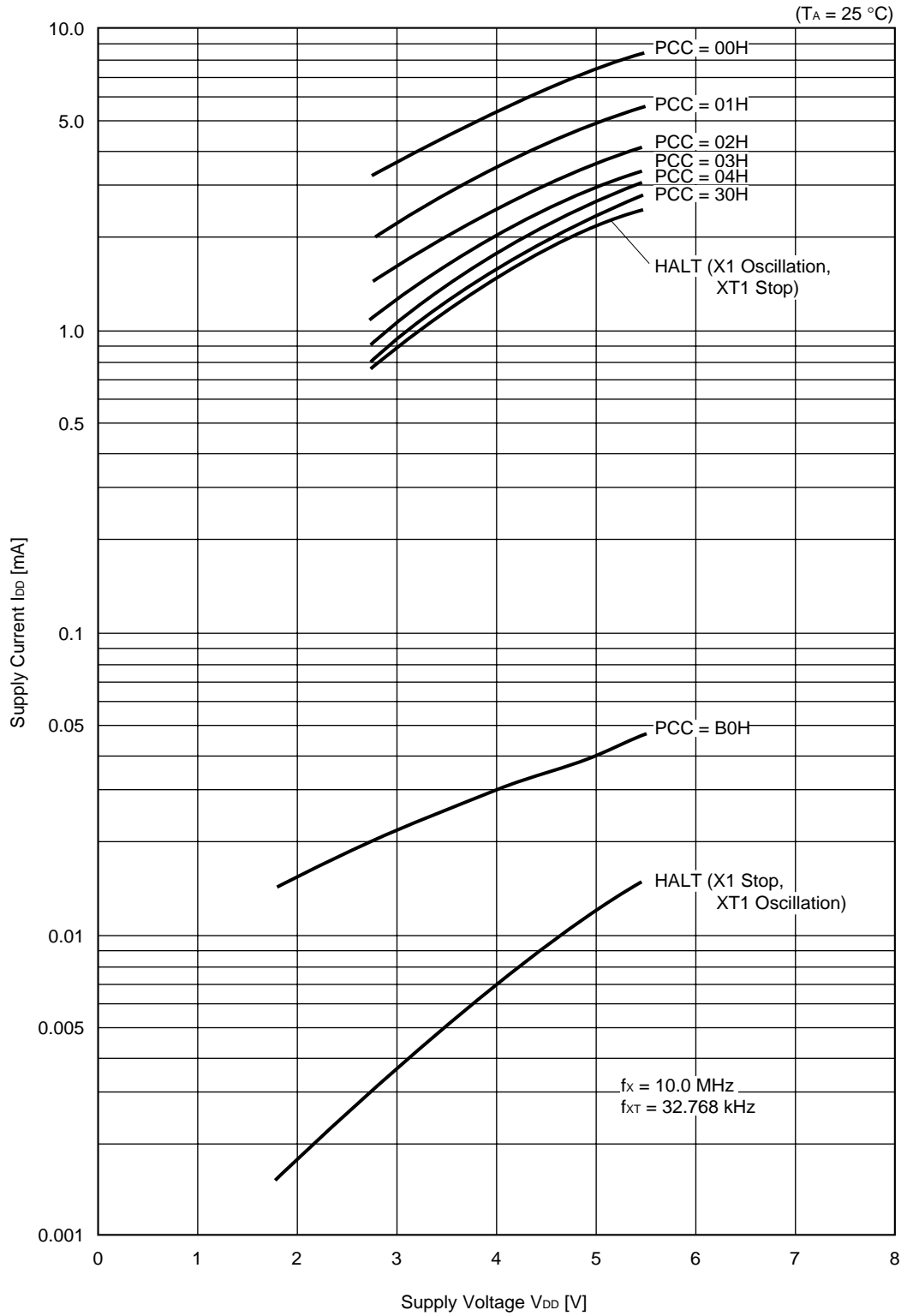


**$\overline{\text{RESET}}$  Input Timing**



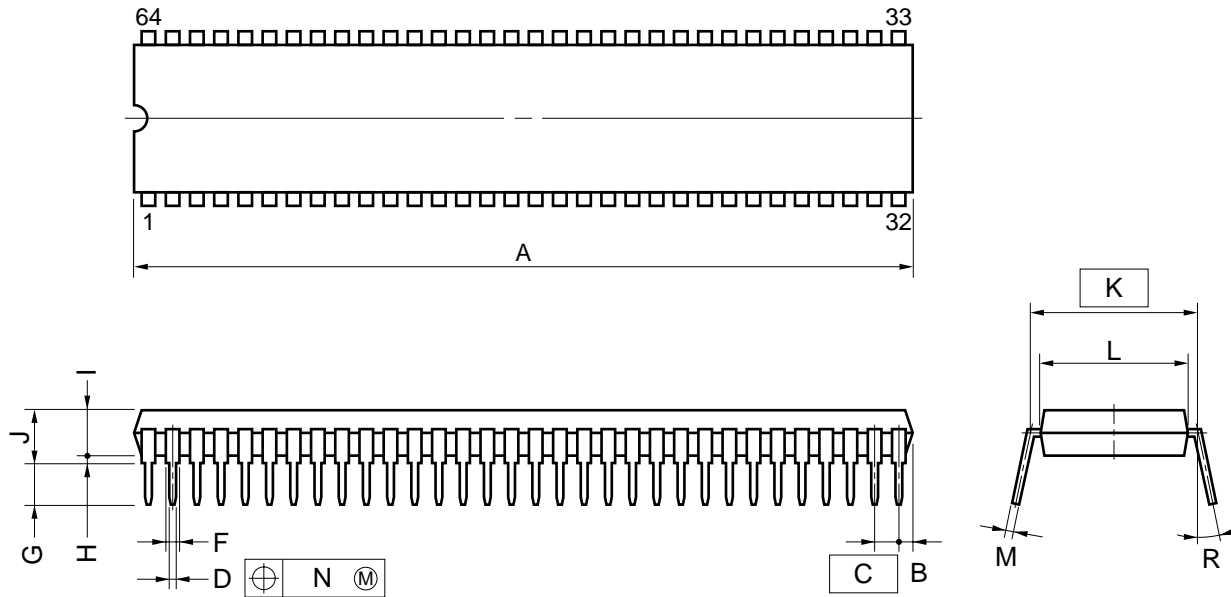
12. CHARACTERISTIC CURVE (REFERENCE VALUES)

I<sub>DD</sub> vs V<sub>DD</sub> (Main System Clock: 10.0 MHz)



13. PACKAGE DRAWINGS

64 PIN PLASTIC SHRINK DIP (750 mil)



NOTE

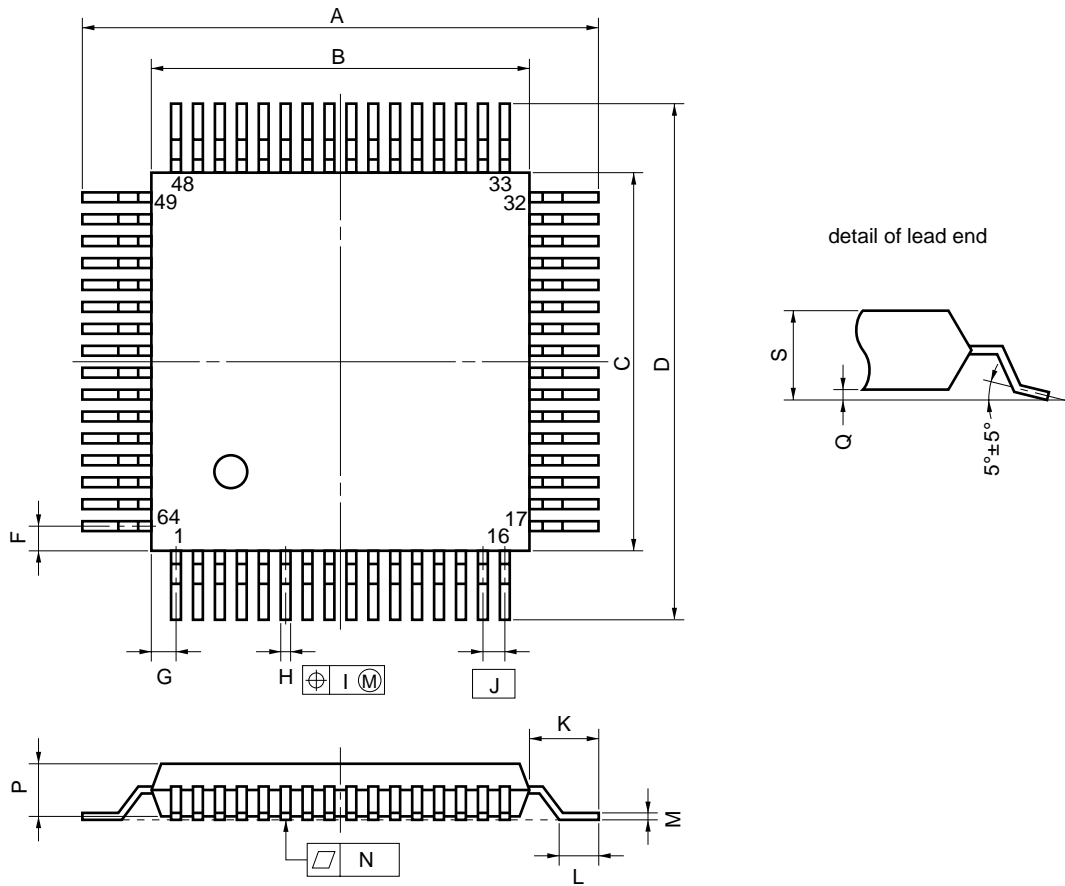
- 1) Each lead centerline is located within 0.17 mm (0.007 inch) of its true position (T.P.) at maximum material condition.
- 2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	58.68 MAX.	2.311 MAX.
B	1.78 MAX.	0.070 MAX.
C	1.778 (T.P.)	0.070 (T.P.)
D	0.50±0.10	0.020 <sup>+0.004</sup> <sub>-0.005</sub>
F	0.9 MIN.	0.035 MIN.
G	3.2±0.3	0.126±0.012
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	19.05 (T.P.)	0.750 (T.P.)
L	17.0	0.669
M	0.25 <sup>+0.10</sup> <sub>-0.05</sub>	0.010 <sup>+0.004</sup> <sub>-0.003</sub>
N	0.17	0.007
R	0~15°	0~15°

P64C-70-750A,C-1

**Remark** Dimensions and materials of ES products are the same as those of mass-production products.

64 PIN PLASTIC QFP (□14)



NOTE

Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

P64GC-80-AB8-2

ITEM	MILLIMETERS	INCHES
A	17.6±0.4	0.693±0.016
B	14.0±0.2	0.551 <sup>+0.009</sup> <sub>-0.008</sub>
C	14.0±0.2	0.551 <sup>+0.009</sup> <sub>-0.008</sub>
D	17.6±0.4	0.693±0.016
F	1.0	0.039
G	1.0	0.039
H	0.35±0.10	0.014 <sup>+0.004</sup> <sub>-0.005</sub>
I	0.15	0.006
J	0.8 (T.P.)	0.031 (T.P.)
K	1.8±0.2	0.071±0.008
L	0.8±0.2	0.031 <sup>+0.009</sup> <sub>-0.008</sub>
M	0.15 <sup>+0.10</sup> <sub>-0.05</sub>	0.006 <sup>+0.004</sup> <sub>-0.003</sub>
N	0.10	0.004
P	2.55	0.100
Q	0.1±0.1	0.004±0.004
S	2.85 MAX.	0.112 MAX.

Remark Dimensions and materials of ES products are the same as those of mass-production products.

**14. RECOMMENDED SOLDERING CONDITIONS**

The μPD78011FY/78012FY/78013FY/78014FY/78015FY/78016FY/78018FY should be soldered and mounted under the conditions recommended in the table below.

For detail of recommended soldering conditions, refer to the information document **Semiconductor Device Mounting Technology Manual (C10535E)**.

For soldering methods and conditions other than those recommended below, contact our salespersonnel.

★ **Table 14-1. Surface Mounting Type Soldering Conditions**

- (1) μPD78011FYGC-xxx-AB8 : 64-Pin Plastic QFP (14 × 14 mm)
- μPD78012FYGC-xxx-AB8 : 64-Pin Plastic QFP (14 × 14 mm)
- μPD78013FYGC-xxx-AB8 : 64-Pin Plastic QFP (14 × 14 mm)
- μPD78014FYGC-xxx-AB8 : 64-Pin Plastic QFP (14 × 14 mm)
- μPD78015FYGC-xxx-AB8 : 64-Pin Plastic QFP (14 × 14 mm)
- μPD78016FYGC-xxx-AB8 : 64-Pin Plastic QFP (14 × 14 mm)
- ★ μPD78018FYGC-xxx-AB8 : 64-Pin Plastic QFP (14 × 14 mm)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235 °C, Duration: 30 sec. max. (at 210 °C or above), Number of times: Three times max.	IR35-00-3
VPS	Package peak temperature: 215 °C, Duration: 40 sec. max. (at 200 °C or above), Number of times: Three times max.	VP15-00-3
Wave soldering	Solder bath temperature: 260 °C max. Duration: 10 sec. max. Number of times: Once Preheating temperature: 120 °C max. (Package surface temperature)	WS60-00-1
Partial heating	Pin temperature: 300 °C max., Duration: 3 sec. max. (per device side)	—

**Caution** Use more than one soldering method should be avoided (except in the case of partial heating).

**Table 14-2. Insertion Type Soldering Conditions**

- μPD78011FYCW-xxx : 64-Pin Plastic Shrink DIP (750 mil)
- μPD78012FYCW-xxx : 64-Pin Plastic Shrink DIP (750 mil)
- μPD78013FYCW-xxx : 64-Pin Plastic Shrink DIP (750 mil)
- μPD78014FYCW-xxx : 64-Pin Plastic Shrink DIP (750 mil)
- μPD78015FYCW-xxx : 64-Pin Plastic Shrink DIP (750 mil)
- μPD78016FYCW-xxx : 64-Pin Plastic Shrink DIP (750 mil)
- μPD78018FYCW-xxx : 64-Pin Plastic Shrink DIP (750 mil)

★

Soldering Method	Soldering Conditions
Wave soldering (pin only)	Solder bath temperature: 260°C max., Duration: 10 sec. max.
Partial heating	Pin temperature: 300°C max., Duration: 3 sec. max. (per pin)

**Caution** Wave soldering is only for the lead part in order that jet solder can not contact with the chip directly.



**APPENDIX A. DEVELOPMENT TOOLS**

The following development tools are available for system development using the  $\mu$ PD78018FY subseries.

**Language Processing Software**

RA78K/0 Notes 1, 2, 3, 4	78K/0 series common assembler package
CC78K/0 Notes 1, 2, 3, 4	78K/0 series common C compiler package
DF78014 Notes 1, 2, 3, 4	Device file common to $\mu$ PD78014 subseries
CC78K/0-L Notes 1, 2, 3, 4	78K/0 series common C compiler library source file

**PROM Writing Tools**

PG-1500	PROM programmer
PA-78P018CW PA-78P018GC PA-78P018KK-S	Programmer adapter connected to PG-1500
PG-1500 controller Notes 1, 2	PG-1500 control program

**Debugging Tool**

IE-78000-R	78K/0 series common in-circuit emulator
★ IE-78000-R-A	78K/0 series common in-circuit emulator (for integrated debugger)
IE-78000-R-BK	78K/0 series common break board
IE-78014-R-EM-A	$\mu$ PD78018F and 78018FY subseries evaluation emulation board ( $V_{DD} = 3.0$ to $6.0$ V)
★ IE-78000-R-SV3	Interface adapter and cable when an EWS is used as the host machine (for IE-78000-R-A)
★ IE-70000-98-IF-B	Interface adapter when PC-9800 series (except notebook PC) is used as the host machine (for IE-78000-R-A)
★ IE-70000-98N-IF	Interface adapter and cable when PC-9800 series notebook PC is used as the host machine (for IE-78000-R-A)
★ IE-70000-PC-IF-B	Interface adapter when IBM PC/AT™ is used as the host machine (for IE-78000-R-A)
EP-78240CW-R EP-78240GC-R	Emulation probe common to $\mu$ PD78244 subseries
EV-9200GC-64	Socket to be mounted on target system board created for the 64-pin plastic QFP (GC-AB8 type)
EV-9900	Tools for removing $\mu$ PD78P018FYKK-S from EV-9200GC-64
SM78K0 Notes 5, 6, 7	78K/0 series common system simulator
★ ID78K0 Notes 4, 5, 6, 7	IE-78000-R-A integrated debugger
SD78K0 Notes 1, 2	IE-78000-R screen debugger
DF78014 Notes 1, 2, 4, 5, 6, 7	Device file common to $\mu$ PD78014 subseries

**Real-Time OS**

RX78K/0 Notes 1, 2, 3, 4	78K/0 series real-time OS
MX78K0 Notes 1, 2, 3, 4	78K/0 series OS

**Fuzzy Inference Development Support System**

FE9000 <b>Note 1</b> /FE9200 <b>Note 6</b>	Fuzzy knowledge data creation tool
FT9080 <b>Note 1</b> /FT9085 <b>Note 2</b>	Translator
FI78K0 <b>Notes 1, 2</b>	Fuzzy inference module
FD78K0 <b>Notes 1, 2</b>	Fuzzy inference debugger

**Notes 1.** PC-9800 series (MS-DOS™) based

2. IBM PC/AT and compatible (PC DOS™/IBM DOS™/MS-DOS) based
3. HP9000 series 300™ (HP-UX™) based
4. HP9000 series 700™ (HP-UX) based, SPARCstation™ (SunOS™) based, EWS4800 series (EWS-UX/V) based
5. PC-9800 series (MS-DOS + Windows™) based
6. IBM PC/AT and compatible (PC DOS/IBM DOS/MS-DOS + Windows) based
7. NEWS™ (NEWS-OS™) based

**Remarks 1.** For development tools manufactured by a third party, refer to the **78K/0 Series Selection Guide (U11126E)**.

2. RA78K/0, CC78K/0, SM78K0, ID78K0, SD78K/0, and RX78K/0 are used in combination with DF78014.

## APPENDIX B. RELATED DOCUMENTS

## Device Related Documents

Document Name		Document No.	
		Japanese	English
★	μPD78018F, 78018FY Subseries User's Manual	U10659J	U10659E
★	78K/0 Series User's Manual - Instruction	U12326J	IEU-1372
★	78K/0 Series Instruction Table	U10903J	—
★	78K/0 Series Instruction Set	U10904J	—
	μPD78018FY Subseries Special Function Register Table	U10287J	—
	78K/0 Series Application Note	Fundamental (I)	IEA-715
		Floating-Point Arithmetic Program	IEA-718
		IEA-1288	IEA-1289

## Development Tools Documents (User's Manual) (1/2)

Document Name		Document No.	
		Japanese	English
	RA78K Series Assembler Package	Operation	EEU-809
		Language	EEU-815
	RA78K Series Structured Assembler Preprocessor	EEU-817	EEU-1402
★	RA78K0 Assembler Package	Operation	U11802J
		Assembly Language	U11801J
		Structured Assembly Language	U11789J
	CC78K Series C Compiler	Operation	EEU-656
		Language	EEU-655
★	CC78K0 C Compiler	Operation	U11517J
		Language	U11518J
	CC78K/0 C Compiler Application Note	Programming Know-how	EEA-618
★	CC78K Series Library Source File	U12322J	—
★	PG-1500 PROM Programmer	U11940J	EEU-1335
	PG-1500 Controller PC-9800 Series (MS-DOS) Based	EEU-704	EEU-1291
	PG-1500 Controller IBM PC Series (PC DOS) Based	EEU-5008	U10540E
★	IE-78000-R	U11376J	U11376E
★	IE-78000-R-A	U10057J	U10057E
	IE-78000-R-BK	EEU-867	EEU-1427
	IE-78014-R-EM-A	EEU-962	U10418E
	EP-78240	EEU-986	EEU-1513
	SM78K0 System Simulator	Reference	U10181J
			U10181E

**Caution** The contents of the above related documents are subject to change without notice. The latest documents should be used for desining, etc.

**Development Tools Documents (User's Manual) (2/2)**

Document Name		Document No.	
		Japanese	English
★ SM78K Series System Simulator	External Part User Open Interface Specifications	U10092J	U10092E
★ ID78K0 Integrated Debugger EWS Based	Reference	U11151J	—
★ ID78K0 Integrated Debugger PC Based	Reference	U11539J	U11539E
★ ID78K0 Integrated Debugger Windows Based	Guide	U11649J	U11649E
★ SD78K/0 Screen Debugger PC-9800 Series (MS-DOS) Based	Introduction	EEU-852	U10539E
	Reference	U10952J	—
★ SD78K/0 Screen Debugger IBM PC/AT (PC DOS) Based	Introduction	EEU-5024	EEU-1414
	Reference	U11279J	U11279E

**Embedded Software Documents (User's Manual)**

Document Name		Document No.	
		Japanese	English
★ 78K/0 Series Real-Time OS	Fundamental	U11537J	U11537E
	Installation	U11536J	U11536E
★ 78K/0 Series OS MX78K0	Fundamental	U12257J	—
Fuzzy Knowledge Data Creation Tool		EEU-829	EEU-1438
78K/0, 78K/II, 87AD Series Fuzzy Inference Development Support System - Translator		EEU-862	EEU-1444
78K/0 Series Fuzzy Inference Development Support System - Fuzzy Inference Module		EEU-858	EEU-1441
78K/0 Series Fuzzy Inference Development Support System - Fuzzy Inference Debugger		EEU-921	EEU-1458

★ **Other Documents**

Document Name		Document No.	
		Japanese	English
IC Package Manual		C10943X	
Semiconductor Device Mounting Technology Manual		C10535J	C10535E
Quality Grades on NEC Semiconductor Device		C11531J	C11531E
NEC Semiconductor Device Reliability/Quality Control System		C10983J	C10983E
Electrostatic Discharge (ESD) Test		MEM-539	—
Guide to Quality Assurance for Semiconductor Device		C11893J	MEI-1202
Guide for Products Related to Microcomputer: Other Companies		U11416J	—

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## NOTES FOR CMOS DEVICES

### ① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

**Note:** Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

### ② HANDLING OF UNUSED INPUT PINS FOR CMOS

**Note:** No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS device behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to  $V_{DD}$  or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

### ③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

**Note:** Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

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Fax: 800-729-9288

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Duesseldorf, Germany  
Tel: 0211-65 03 02  
Fax: 0211-65 03 490

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Tel: 01908-691-133  
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Fax: 040-2444580

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Tel: 02-528-0303  
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United Square, Singapore 1130  
Tel: 253-8311  
Fax: 250-3583

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Tel: 02-719-2377  
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