HD74ALVCH162820

3.3-V 10-bit Flip Flops with Dual Outputs and 3-state Outputs

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Description

The HD74ALVCH162820 flip flops are edge triggered D-type flip flops. On the positive transition of the clock (CLK) input, the device provides true data at the Q outputs. A buffered output enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high impedance state. In the high impedance state, the outputs neither load nor drive the bus lines significantly. The high impedance state and increased drive provide the capability to drive bus line without need for interface or pullup components. $\overline{OE}$ does not affect the internal operations of the flip flops. Old data can be retained or new data can be entered while the outputs are in the high impedance state. Active bus hold circuitry is provided to hold unused or floating data inputs at a valid logic level. All outputs, which are designed to sink up to 12 mA, include 26 Ω resistors to reduce overshoot and undershoot.

Features

- VCC = 2.3 V to 3.6 V
- Typical VOL ground bounce < 0.8 V (@VCC = 3.3 V, Ta = 25°C)
- Typical VOH undershoot > 2.0 V (@VCC = 3.3 V, Ta = 25°C)
- High output current ±12 mA (@VCC = 3.0 V)
- Bus hold on data inputs eliminates the need for external pullup / pulldown resistors
- All outputs have equivalent 26 Ω series resistors, so no external resistors are required.

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Function Table

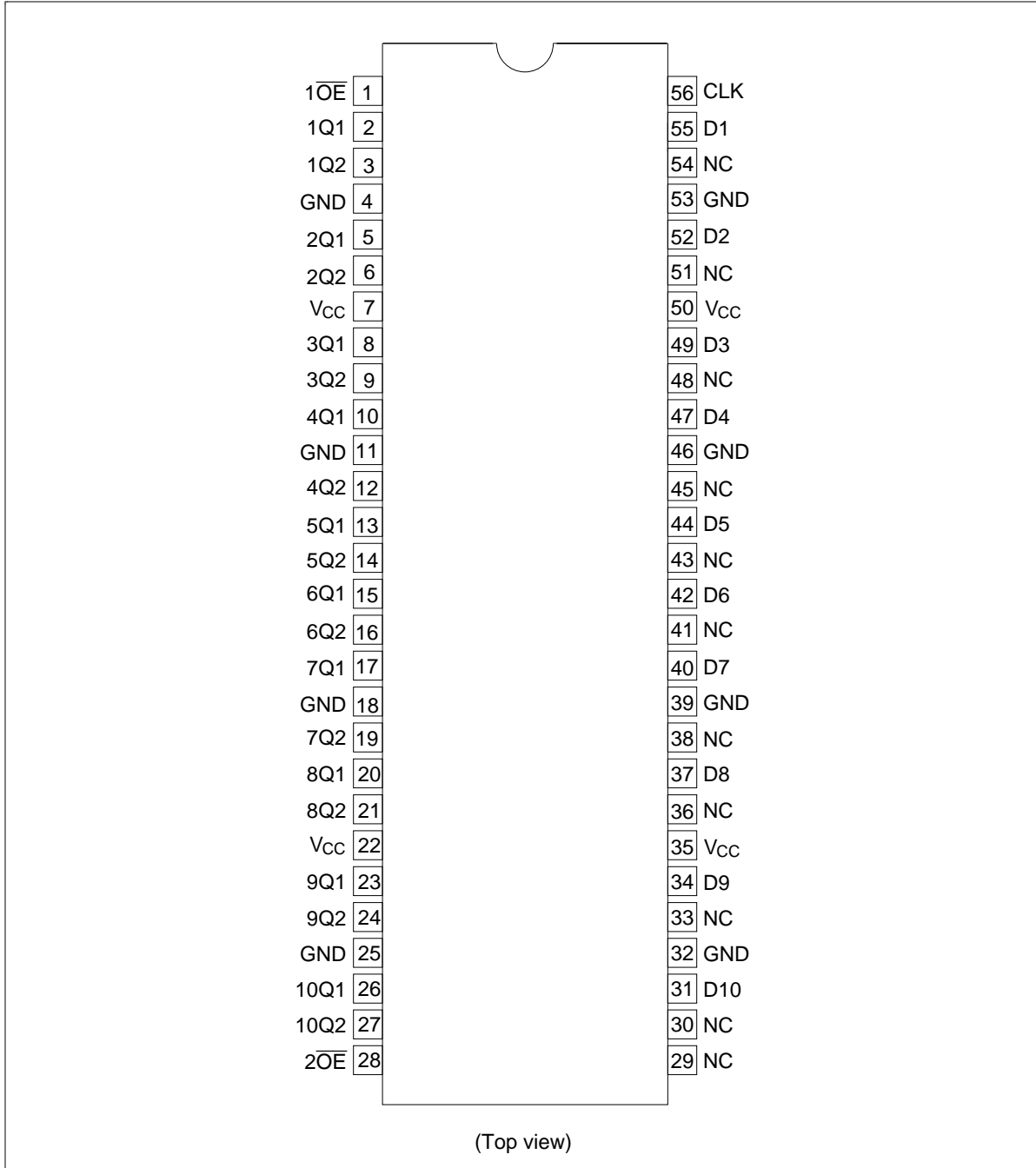| Inputs			Output Q
$\overline{OE}n$ [2]	CLK	D	
L	↑	H	H
L	↑	L	L
L	L	X	Q_0 [1]
H	X	X	Z

H : High level

L : Low level

X : Immaterial

Z : High impedance

↑ : Low to high transition

Notes: 1. Output level before the indicated steady state input conditions were established.

2. n = 1, 2

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Pin Arrangement

1$\overline{\text{OE}}$	1	56	CLK
1Q1	2	55	D1
1Q2	3	54	NC
GND	4	53	GND
2Q1	5	52	D2
2Q2	6	51	NC
V_{CC}	7	50	V_{CC}
3Q1	8	49	D3
3Q2	9	48	NC
4Q1	10	47	D4
GND	11	46	GND
4Q2	12	45	NC
5Q1	13	44	D5
5Q2	14	43	NC
6Q1	15	42	D6
6Q2	16	41	NC
7Q1	17	40	D7
GND	18	39	GND
7Q2	19	38	NC
8Q1	20	37	D8
8Q2	21	36	NC
V_{CC}	22	35	V_{CC}
9Q1	23	34	D9
9Q2	24	33	NC
GND	25	32	GND
10Q1	26	31	D10
10Q2	27	30	NC
2$\overline{\text{OE}}$	28	29	NC

(Top view)

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Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	V_{CC}	–0.5 to 4.6	V	
Input voltage [1]	V_I	–0.5 to 4.6	V	
Output voltage [1, 2]	V_O	–0.5 to V_{CC} +0.5	V	
Input clamp current	I_{IK}	–50	mA	$V_I < 0$
Output clamp current	I_{OK}	±50	mA	$V_O < 0$ or $V_O > V_{CC}$
Continuous output current	I_O	±50	mA	$V_O = 0$ to V_{CC}
V_{CC}, GND current / pin	I_{CC} or I_{GND}	±100	mA	
Maximum power dissipation at Ta = 55°C (in still air) [3]	P_T	1	W	TSSOP
Storage temperature	Tstg	–65 to 150	°C	

Notes: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

1. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

Recommended Operating Conditions

Item	Symbol	Min	Max	Unit	Conditions
Supply voltage	V_{CC}	2.3	3.6	V	
Input voltage	V_I	0	V_{CC}	V	
Output voltage	V_O	0	V_{CC}	V	
High level output current	I_{OH}	—	–6	mA	$V_{CC} = 2.3$ V
		—	–8		$V_{CC} = 2.7$ V
		—	–12		$V_{CC} = 3.0$ V
Low level output current	I_{OL}	—	6	mA	$V_{CC} = 2.3$ V
		—	8		$V_{CC} = 2.7$ V
		—	12		$V_{CC} = 3.0$ V
Input transition rise or fall rate	$\Delta t / \Delta v$	0	10	ns / V	
Operating temperature	Ta	–40	85	°C	

Note: Unused control inputs must be held high or low to prevent them from floating.

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Logic Diagram

To nine other channels

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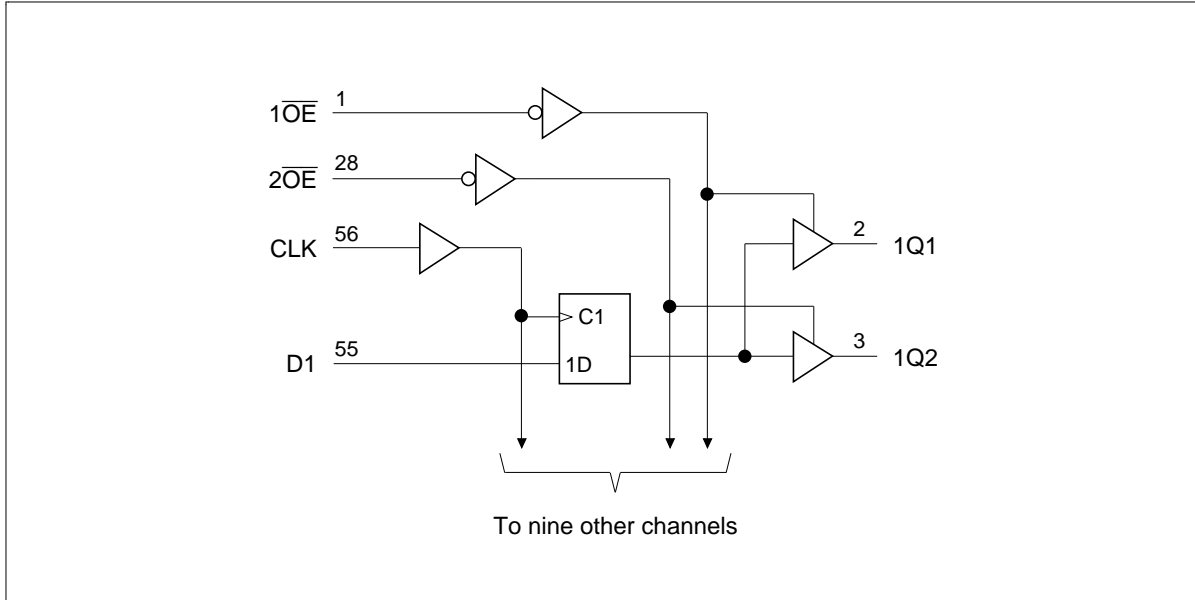
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Electrical Characteristics (Ta = –40 to 85°C)

Item	Symbol	V_{CC} (V) [*1]	Min	Max	Unit	Test Conditions
Input voltage	V_{IH}	2.3 to 2.7	1.7	—	V	
		2.7 to 3.6	2.0	—		
	V_{IL}	2.3 to 2.7	—	0.7		
		2.7 to 3.6	—	0.8		
Output voltage	V_{OH}	Min to Max	V_{CC}–0.2	—	V	I_{OH} = –100 μA
		2.3	1.9	—		I_{OH} = –4 mA, V_{IH} = 1.7 V
		2.3	1.7	—		I_{OH} = –6 mA, V_{IH} = 1.7 V
		3.0	2.4	—		I_{OH} = –6 mA, V_{IH} = 2.0 V
		2.7	2.0	—		I_{OH} = –8 mA, V_{IH} = 2.0 V
		3.0	2.0	—		I_{OH} = –12 mA, V_{IH} = 2.0 V
	V_{OL}	Min to Max	—	0.2		I_{OL} = 100 μA
		2.3	—	0.4		I_{OL} = 4 mA, V_{IL} = 0.7 V
		2.3	—	0.55		I_{OL} = 6 mA, V_{IL} = 0.7 V
		3.0	—	0.55		I_{OL} = 6 mA, V_{IL} = 0.8 V
		2.7	—	0.6		I_{OL} = 8 mA, V_{IL} = 0.8 V
		3.0	—	0.8		I_{OL} = 12 mA, V_{IL} = 0.8 V
Input current	I_{IN}	3.6	—	±5	μA	V_{IN} = V_{CC} or GND
	$I_{IN\,(hold)}$	2.3	45	—		V_{IN} = 0.7 V
		2.3	–45	—		V_{IN} = 1.7 V
		3.0	75	—		V_{IN} = 0.8 V
		3.0	–75	—		V_{IN} = 2.0 V
		3.6	—	±500		V_{IN} = 0 to 3.6 V
Off state output current [*2]	I_{OZ}	3.6	—	±10	μA	V_{OUT} = V_{CC} or GND
Quiescent supply current	I_{CC}	3.6	—	40	μA	V_{IN} = V_{CC} or GND
	ΔI_{CC}	3.0 to 3.6	—	750	μA	V_{IN} = one input at (V_{CC}–0.6) V, other inputs at V_{CC} or GND

Notes: 1. For conditions shown as Min or Max, use the appropriate values under recommended operating conditions.

2. For I/O ports, the parameter I_{OZ} includes the input leakage current.

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Switching Characteristics (Ta = –40 to 85°C)

Item	Symbol	V_{cc} (V)	Min	Typ	Max	Unit	FROM (Input)	TO (Output)
Maximum clock frequency	f_{max}	2.5±0.2	150	—	—	MHz		
		2.7	150	—	—			
		3.3±0.3	150	—	—			
Propagation delay time	t_{PLH}	2.5±0.2	1.0	—	7.0	ns	CLK	Q
	t_{PHL}	2.7	—	—	6.2			
		3.3±0.3	1.0	—	5.4			
Output enable time	t_{ZH}	2.5±0.2	1.0	—	7.4	ns	$\overline{OE}$	Q
	t_{ZL}	2.7	—	—	6.8			
		3.3±0.3	1.0	—	5.6			
Output disable time	t_{HZ}	2.5±0.2	1.3	—	6.4	ns	$\overline{OE}$	Q
	t_{LZ}	2.7	—	—	5.5			
		3.3±0.3	1.0	—	5.0			
Setup time	t_{su}	2.5±0.2	1.7	—	—	ns		
		2.7	1.8	—	—			
		3.3±0.3	1.4	—	—			
Hold time	t_{h}	2.5±0.2	1.1	—	—	ns		
		2.7	1.1	—	—			
		3.3±0.3	1.0	—	—			
Pulse width	t_{w}	2.5±0.2	3.3	—	—	ns		
		2.7	3.3	—	—			
		3.3±0.3	3.3	—	—			
Input capacitance	C_{IN}	3.3	—	3.5	—	pF	Control inputs	
		3.3	—	6.0	—		Data inputs	
Output capacitance	C_{O}	3.3	—	7.0	—	pF		

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• **Test Circuit**

See under table

500 Ω   S1

○ OPEN

○ GND

*1
C_L = 50 pF ⪕ 500 Ω
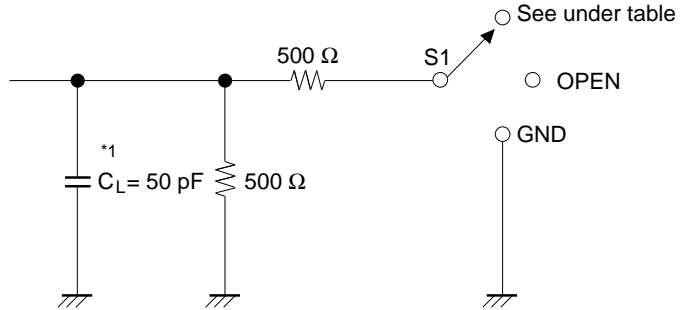
Load Circuit for Outputs

Symbol	Vcc=2.5±0.2V	Vcc=2.7V, 3.3±0.3V
t_{PLH}/ t_{PHL} t_{su} / t_h / t_w	OPEN	OPEN
t_{ZH}/ t_{HZ}	GND	GND
t_{ZL}/ t_{LZ}	4.6 V	6.0 V

Note: 1. C_L includes probe and jig capacitance.

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• **Waveforms – 1**

Input

t_r t_f

90 %   90 %

V_{ref} V_{ref}

10 %   10 %

V_{IH}

GND

t_{PLH} t_{PHL}

Output

V_{ref} V_{ref}

V_{OH}

V_{OL}

• **Waveforms – 2**

Timing Input

t_r

90 %

V_{ref}

10 %

V_{IH}

GND

t_{su} t_h

Data Input

V_{ref} V_{ref}

V_{IH}

GND

t_w

Input

V_{ref} V_{ref}

V_{IH}

GND

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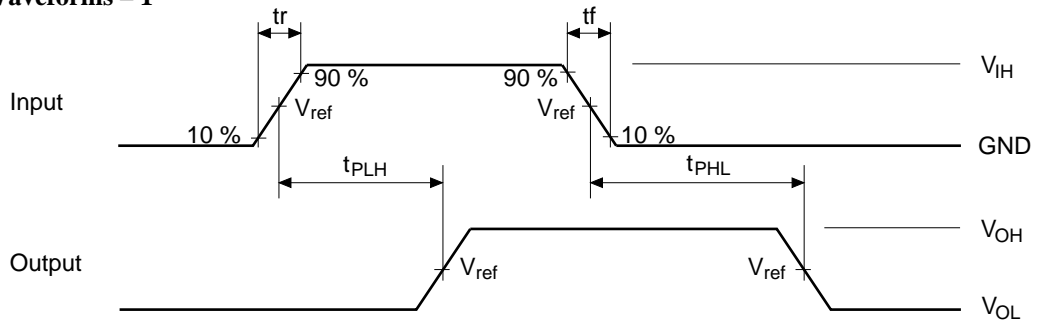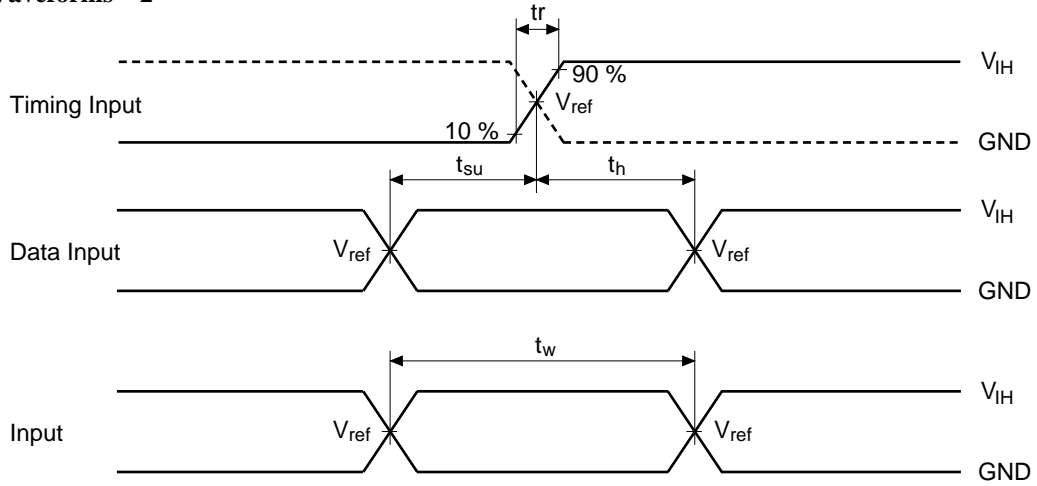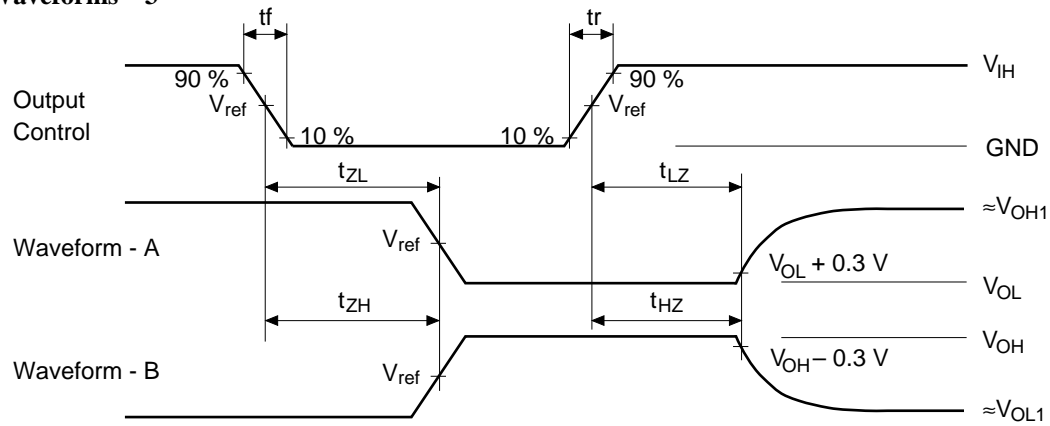
• **Waveforms – 3**

TEST	Vcc=2.5±0.2V	Vcc=2.7V, 3.3±0.3V
V_{IH}	2.3 V	2.7 V
V_{ref}	1.2 V	1.5 V
V_{OH1}	2.3 V	3.0 V
V_{OL1}	GND	GND

Notes: 1. All input pulses are supplied by generators having the following characteristics:
PRR ≤ 10 MHz, Zo = 50 Ω, tr ≤ 2.5 ns, tf ≤ 2.5 ns.
2. Waveform – A is for an output with internal conditions such that the output is low
except when disabled by the output control.
3. Waveform – B is for an output with internal conditions such that the output is high
except when disabled by the output control.
4. The output are measured one at a time with one transition per measurement.

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Package Dimensions/Unit : mm

14.00 $^{+0.3}_{-0.1}$

56   29

6.10 $^{+0.3}_{-0.1}$

1   28

0.50

0.20 $^{+0.1}_{-0.05}$ ⊕ | 0.08 Ⓜ

0.40 Max

0.10

0.05 Min

1.20 max

0.15 ± 0.05

8.10 ± 0.3

10° Max

0.50 ± 0.1

Hitachi code	TTP-56D
EIAJ code	—
JEDEC code	—

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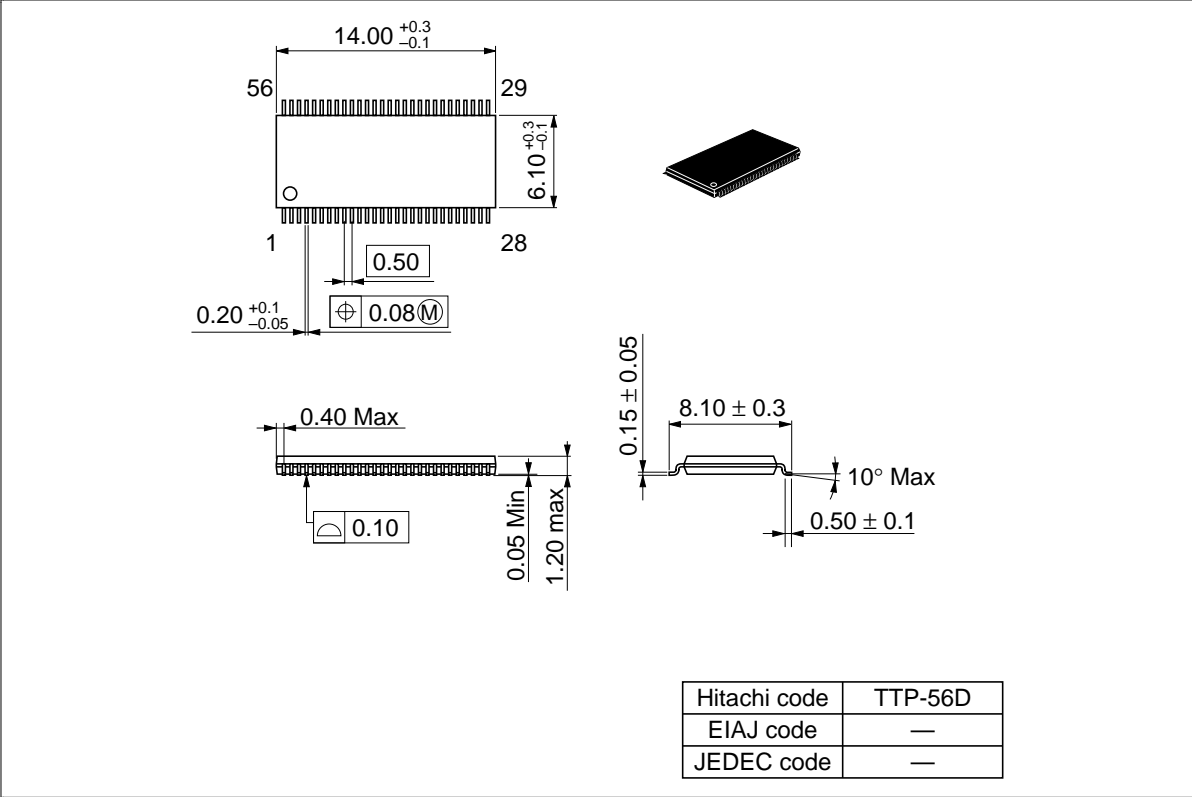
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