
HB56A140BR Series

1,048,576-word × 40-bit High Density Dynamic RAM Module

HITACHI

ADE-203-
Rev. 0.0
Dec. 1, 1995

Description

The HB56A140BR is a 1M × 40 dynamic RAM module, mounted 10 pieces of 4-Mbit DRAM (HM514400CS/CLS) sealed in SOJ package. An outline of the HB56A140BR is 72-pin single in-line package. Therefore, the HB56A140BR makes high density mounting possible without surface mount technology. The HB56A140BR provides common data inputs and outputs. Its module board has decoupling capacitors beneath the each SOJ.

Features

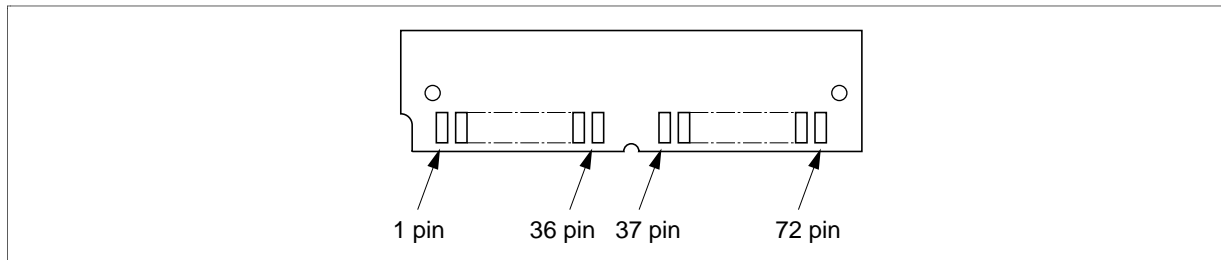
- 72-pin single in-line package
 - Lead pitch : 1.27 mm
- Single 5 V (± 5%) supply
- High speed
 - Access time : 60 ns/70 ns/80 ns (max)
- Low power dissipation
 - Operating : 5.78 W/5.25 W/4.73 W (max)
 - Standby : 105 mW (max)
5.25 mW (max) (L-version)
- Fast page mode capability
- 1,024 refresh cycle : 16 ms
: 128 ms (L-version)
- 2 variations of refresh
 - $\overline{\text{RAS}}$ -only refresh
 - $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh
- TTL compatible

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Ordering Information

Type No.	Access Time	Package	Contact Pad
HB56A140BR-6C	60 ns	72-pin SIP socket type	Gold
HB56A140BR-7C	70 ns		
HB56A140BR-8C	80 ns		
HB56A140BR-6CL	60 ns		
HB56A140BR-7CL	70 ns		
HB56A140BR-8CL	80 ns		

Pin Arrangement



Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	V_{SS}	19	\overline{OE}	37	DQ19	55	DQ28
2	DQ0	20	DQ8	38	DQ20	56	DQ29
3	DQ1	21	DQ9	39	V_{SS}	57	DQ30
4	DQ2	22	DQ10	40	$\overline{CAS0}$	58	DQ31
5	DQ3	23	DQ11	41	NC	59	V_{CC}
6	DQ4	24	DQ12	42	NC	60	DQ32
7	DQ5	25	DQ13	43	NC	61	DQ33
8	DQ6	26	DQ14	44	$\overline{RAS0}$	62	DQ34
9	DQ7	27	DQ15	45	NC	63	DQ35
10	V_{CC}	28	A7	46	DQ21	64	DQ36
11	PD4	29	DQ16	47	\overline{WE}	65	DQ37
12	A0	30	V_{CC}	48	X40 (V_{SS})	66	DQ38
13	A1	31	A8	49	DQ22	67	PD0
14	A2	32	A9	50	DQ23	68	PD1
15	A3	33	NC	51	DQ24	69	PD2
16	A4	34	NC	52	DQ25	70	PD3
17	A5	35	DQ17	53	DQ26	71	DQ39
18	A6	36	DQ18	54	DQ27	72	V_{SS}

Pin Description

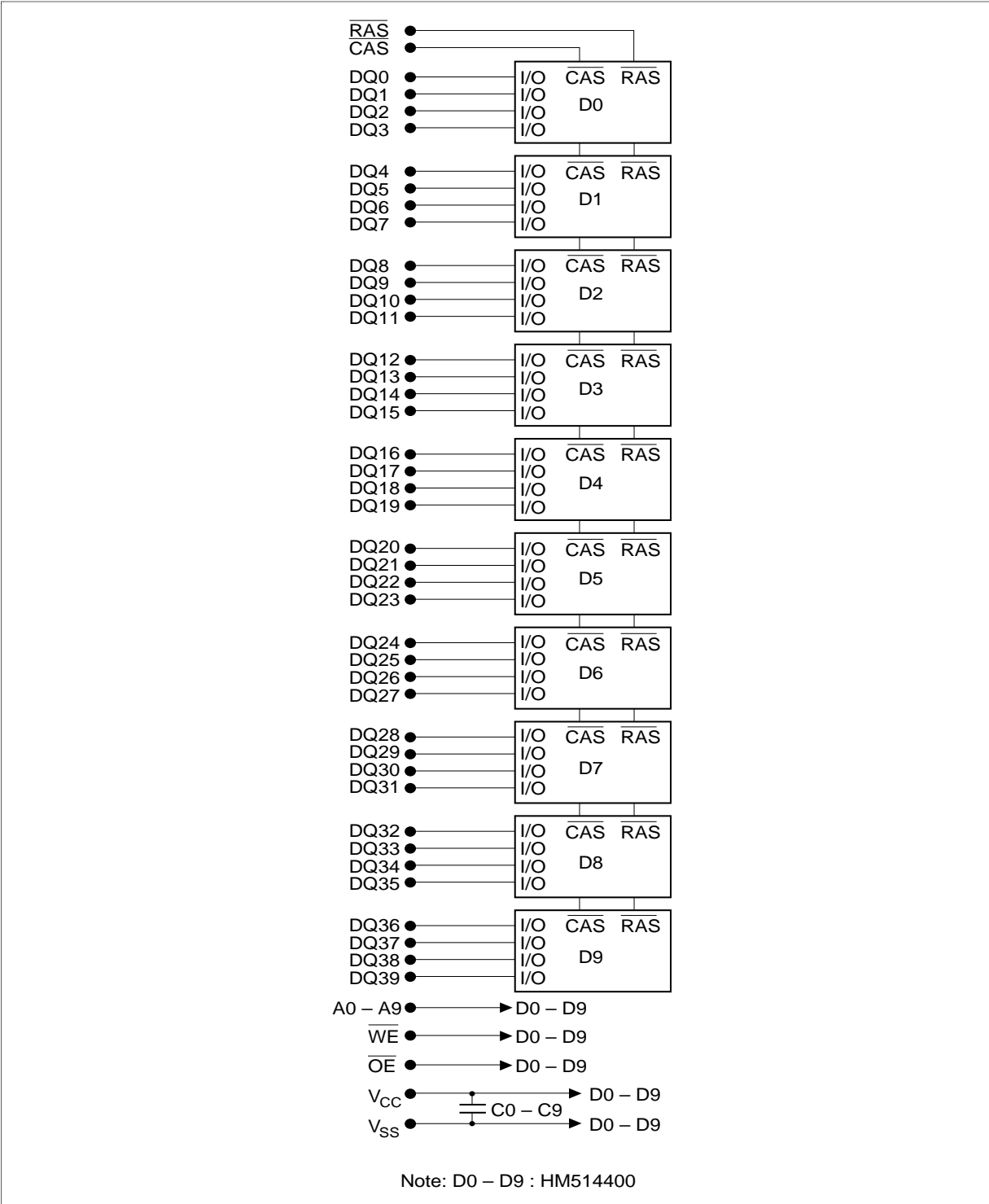
Pin Name	Function
A0–A9	Address input
A0–A9	Refresh address input
DQ0–DQ39	Data-in/data-out
$\overline{\text{CAS0}}$	Column address strobe
$\overline{\text{RAS0}}$	Row address strobe
$\overline{\text{WE}}$	Read/write enable
$\overline{\text{OE}}$	Output enable
V_{cc}	Power supply (+5 V)
V_{ss}	Ground
PD0–PD4	Presence detect pin
NC	No connection

Presence Detect Pin Arrangement

Pin No.	Pin Name	HB56A140BR		
		60 ns	70 ns	80 ns
67	PD0	V_{ss}	V_{ss}	V_{ss}
68	PD1	V_{ss}	V_{ss}	V_{ss}
69	PD2	NC	V_{ss}	NC
70	PD3	NC	NC	V_{ss}
11	PD4	NC	NC	NC

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Block Diagram



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Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_T	-1.0 to +7.0	V
Supply voltage relative to V_{SS}	V_{CC}	-1.0 to +7.0	V
Short circuit output current	I_{out}	50	mA
Power dissipation	P_T	10	W
Operating temperature	T_{opr}	0 to +70	°C
Storage temperature	T_{stg}	-55 to +125	°C

Recommended DC Operating Conditions ($T_a = 0$ to $+70^\circ\text{C}$)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{CC}	4.75	5.0	5.25	V	1
Input high voltage	V_{IH}	2.4	—	5.5	V	1
Input low voltage	V_{IL}	-1.0	—	0.8	V	1

Note: 1. All voltage referred to V_{SS} .

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DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 5%, V_{SS} = 0 V)

Parameter	Symbol	HB56A140BR						Unit	Test Conditions	Notes
		60 ns		70 ns		80 ns				
		Min	Max	Min	Max	Min	Max			
Operating current	I _{CC1}	—	1100	—	1000	—	900	mA	t _{RC} = min	1, 2
Standby current	I _{CC2}	—	20	—	20	—	20	mA	TTL interface R _{AS} , C _{AS} = V _{IH} Dout = High-Z	
		—	10	—	10	—	10	mA	CMOS interface R _{AS} , C _{AS} ≥ V _{CC} - 0.2V Dout = High-Z	
Standby current (L-version)	I _{CC2}	—	1	—	1	—	1	mA	CMOS interface R _{AS} , C _{AS} = V _{IH} WE, OE, address, Din = V _{IH} or V _{IL} Dout = High-Z	4
R _{AS} -only refresh current	I _{CC3}	—	1100	—	1000	—	900	mA	t _{RC} = min	2
Standby current	I _{CC5}	—	50	—	50	—	50	mA	R _{AS} = V _{IH} , C _{AS} = V _{IL} Dout = enable	1
C _{AS} -before-R _{AS} refresh current	I _{CC6}	—	1100	—	1000	—	900	mA	t _{RC} = min	
Fast page mode current	I _{CC7}	—	1100	—	1000	—	900	mA	t _{PC} = min	1, 3
Battery backup operation current (CBR refresh) (L-version)	I _{CC10}	—	2	—	2	—	2	mA	t _{RC} = 125 μs, t _{RAS} ≤ 1 μs WE = V _{IH} , C _{AS} = V _{IL} OE, address, Din = V _{IH} or V _{IL} , Dout = High-Z	4
Input leakage current	I _{LI}	-10	10	-10	10	-10	10	μA	0 V ≤ Vin ≤ 7 V	
Output leakage current	I _{LO}	-10	10	-10	10	-10	10	μA	0 V ≤ Vout ≤ 7 V Dout = disable	
Output high voltage	V _{OH}	2.4	V _{CC}	2.4	V _{CC}	2.4	V _{CC}	V	Iout = -5 mA	
Output low voltage	V _{OL}	0	0.4	0	0.4	0	0.4	V	Iout = 4.2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected. I_{CC} max is specified at the output open condition.

2. Address can be changed once or less while R_{AS} = V_{IL}.

3. Address can be changed once or less while C_{AS} = V_{IH}.

4. V_{CC} - 0.2 V ≤ V_{IH} ≤ 6.5 V, 0 V ≤ V_{IL} ≤ 0.2 V.

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Capacitance ($T_a = 25^\circ\text{C}$, $V_{CC} = 5\text{ V} \pm 5\%$)

Parameter	Symbol	Typ	Max	Unit	Notes
Input capacitance (Address A0–A9)	C_{I1}	—	90	pF	1
Input capacitance (\overline{WE} , \overline{OE})	C_{I2}	—	90	pF	1
Input capacitance (\overline{RAS} , \overline{CAS})	C_{I3}	—	90	pF	1
Input/Output capacitance (DQ0–DQ39)	$C_{I/O}$	—	20	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
 2. $\overline{CAS} = V_{IH}$ to disable Dout.

AC Characteristics

- Refer to the HM514400C Series data sheet.

Physical Outline

Unit : mm/inch

