HB56UW873EJN-5/6, HB56UW865EJN-5/6

64MB Unbuffered EDO DRAM DIMM
8-Mword × 72/64-bit, 4k Refresh, 1 Bank Module
(9/8 pcs of 8M × 8 components)

HITACHI

ADE-203-860A (Z)
Rev. 1.0
May 20, 1998

Description

The HB56UW873EJN, HB56UW865EJN belong to 8-byte DIMM (Dual in-line Memory Module) family , and have been developed an optimized main memory solution for 4 and 8-byte processor applications. The HB56UW873EJN is a 8 M × 72 Dynamic RAM Module, mounted 9 pieces of 64-Mbit DRAM (HM5165805) sealed in SOJ package and 1 piece of serial EEPROM for Presence Detect (PD). The HB56UW865EJN is a 8 M × 64 Dynamic RAM Module, mounted 8 pieces of 64-Mbit DRAM (HM5165805) sealed in SOJ package and 1 piece of serial EEPROM for Presence Detect (PD). The HB56UW873EJN, HB56UW865EJN offer Extended Data Out (EDO) Page Mode as a high speed access mode. An outline of the HB56UW873EJN, HB56UW865EJN are 168-pin socket type package (dual lead out). Therefore, the HB56UW873EJN, HB56UW865EJN make high density mounting possible without surface mount technology. The HB56UW873EJN, HB56UW865EJN provide common data inputs and outputs. Decoupling capacitors are mounted beside each SOJ on the its module board.

Features

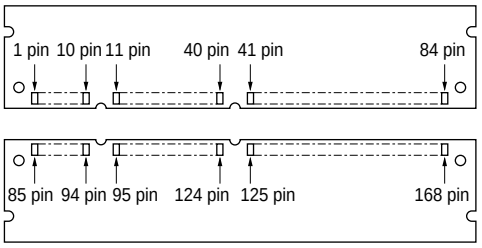
- 168-pin socket type package (Dual lead out)
  - Outline: 133.35 mm (Length) × 25.40 mm (Height) × 5.28 mm (Thickness)
  - Lead pitch : 1.27 mm
- Single 3.3 V supply: 3.3 V ± 0.3 V
- High speed
  - Access time: t_{RAC} = 50 ns/60 ns (max)
  - Access time: t_{CAC} = 13 ns/15 ns (max)

- Low power dissipation
  - Active mode: 4.37 W/3.73 W (max) (HB56UW873EJN Series)
  - Active mode: 3.89 W/3.31 W (max) (HB56UW865EJN Series)
  - Standby mode (TTL): 64.8 mW (max) (HB56UW873EJN Series)
  - Standby mode (TTL): 57.6 mW (max) (HB56UW865EJN Series)
  - Standby mode (CMOS): 16.2 mW (max) (HB56UW873EJN Series)
  - Standby mode (CMOS): 14.4 mW (max) (HB56UW865EJN Series)
- JEDEC standard outline unbuffered 8-byte DIMM
- EDO page mode capability
- 4096 refresh cycles: 64 ms
- 3 variations of refresh
  - $\overline{\text{RAS}}$-only refresh
  - $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh
  - Hidden refresh

Ordering Information

Type No.	Access time	Package	Contact pad
HB56UW873EJN-5	50 ns	168-pin dual lead out socket type	Gold
HB56UW873EJN-6	60 ns		
HB56UW865EJN-5	50 ns		
HB56UW865EJN-6	60 ns		

Pin Arrangement



Pin No.	Signal name	Pin No.	Signal name	Pin No.	Signal name	Pin No.	Signal name
1	V_{SS}	43	V_{SS}	85	V_{SS}	127	V_{SS}
2	DQ0	44	$\overline{OE}2$	86	DQ32	128	NC
3	DQ1	45	$\overline{RAS}2$	87	DQ33	129	NC
4	DQ2	46	$\overline{CAS}2$	88	DQ34	130	$\overline{CAS}6$
5	DQ3	47	$\overline{CAS}3$	89	DQ35	131	$\overline{CAS}7$
6	V_{CC}	48	$\overline{WE}2$	90	V_{CC}	132	NC
7	DQ4	49	V_{CC}	91	DQ36	133	V_{CC}
8	DQ5	50	NC	92	DQ37	134	NC
9	DQ6	51	NC	93	DQ38	135	NC
10	DQ7	52	CB2 (NC)*[3]	94	DQ39	136	CB6 (NC)*[7]
11	DQ8	53	CB3 (NC)*[4]	95	DQ40	137	CB7 (NC)*[8]
12	V_{SS}	54	V_{SS}	96	V_{SS}	138	V_{SS}
13	DQ9	55	DQ16	97	DQ41	139	DQ48
14	DQ10	56	DQ17	98	DQ42	140	DQ49
15	DQ11	57	DQ18	99	DQ43	141	DQ50
16	DQ12	58	DQ19	100	DQ44	142	DQ51
17	DQ13	59	V_{CC}	101	DQ45	143	V_{CC}
18	V_{CC}	60	DQ20	102	V_{CC}	144	DQ52
19	DQ14	61	NC	103	DQ46	145	NC
20	DQ15	62	NC	104	DQ47	146	NC
21	CB0 (NC)*[1]	63	NC	105	CB4 (NC)*[5]	147	NC
22	CB1 (NC)*[2]	64	V_{SS}	106	CB5 (NC)*[6]	148	V_{SS}
23	V_{SS}	65	DQ21	107	V_{SS}	149	DQ53
24	NC	66	DQ22	108	NC	150	DQ54
25	NC	67	DQ23	109	NC	151	DQ55

Pin Arrangement (cont)

Pin No.	Signal name	Pin No.	Signal name	Pin No.	Signal name	Pin No.	Signal name
26	V_{CC}	68	V_{SS}	110	V_{CC}	152	V_{SS}
27	$\overline{WE}0$	69	DQ24	111	NC	153	DQ56
28	$\overline{CAS}0$	70	DQ25	112	$\overline{CAS}4$	154	DQ57
29	$\overline{CAS}1$	71	DQ26	113	$\overline{CAS}5$	155	DQ58
30	$\overline{RAS}0$	72	DQ27	114	NC	156	DQ59
31	$\overline{OE}0$	73	V_{CC}	115	NC	157	V_{CC}
32	V_{SS}	74	DQ28	116	V_{SS}	158	DQ60
33	A0	75	DQ29	117	A1	159	DQ61
34	A2	76	DQ30	118	A3	160	DQ62
35	A4	77	DQ31	119	A5	161	DQ63
36	A6	78	V_{SS}	120	A7	162	V_{SS}
37	A8	79	NC	121	A9	163	NC
38	A10	80	NC	122	A11	164	NC
39	NC	81	NC	123	NC	165	SA0
40	V_{CC}	82	SDA	124	V_{CC}	166	SA1
41	V_{CC}	83	SCL	125	NC	167	SA2
42	NC	84	V_{CC}	126	NC	168	V_{CC}

Notes: 1. CB0: HB56UW873EJN, NC: HB56UW865EJN
2. CB1: HB56UW873EJN, NC: HB56UW865EJN
3. CB2: HB56UW873EJN, NC: HB56UW865EJN
4. CB3: HB56UW873EJN, NC: HB56UW865EJN
5. CB4: HB56UW873EJN, NC: HB56UW865EJN
6. CB5: HB56UW873EJN, NC: HB56UW865EJN
7. CB6: HB56UW873EJN, NC: HB56UW865EJN
8. CB7: HB56UW873EJN, NC: HB56UW865EJN

Pin Description

Pin name	Function
A0 to A11	Address input Row address A0 to A11 Column address A0 to A10 Refresh address A0 to A11
DQ0 to DQ63	Data input/output
$\overline{RAS}$0, $\overline{RAS}$2	Row address strobe
$\overline{CAS}$0 to $\overline{CAS}$7	Column address strobe
$\overline{WE}$0, $\overline{WE}$2	Read/Write enable
$\overline{OE}$0, $\overline{OE}$2	Output enable
SDA	Serial data out (bit0 to bit7)
SCL	Clock for presence detect
SA0 to SA2	Serial address input
CB0 to CB7*[1]	Check bit
V_{CC}	Power supply
V_{SS}	Ground
NC	No connection

Note: 1. This function is supported only HB56UW873EJN Series.

Serial PD Matrix*[1]

Byte No.	Function described	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Hex value	Comments
0	Number of bytes used by module manufacturer	1	0	0	0	0	0	0	0	80	128 byte
1	Total SPD memory size	0	0	0	0	1	0	0	0	08	256 byte
2	Memory type	0	0	0	0	0	0	1	0	02	EDO
3	Number of row addresses bits	0	0	0	0	1	1	0	0	0C	12
4	Number of column addresses bits	0	0	0	0	1	0	1	1	0B	11
5	Number of banks	0	0	0	0	0	0	0	1	01	1
6	Module data width										
	(HB56UW873EJN)	0	1	0	0	1	0	0	0	48	72
	(HB56UW865EJN)	0	1	0	0	0	0	0	0	40	64
7	Module data width (continued)	0	0	0	0	0	0	0	0	00	0 (+)
8	Module interface signal levels	0	0	0	0	0	0	0	1	01	LVTTL
9	$\overline{RAS}$ access time										
	-5	0	0	1	1	0	0	1	0	32	t_{RAC} = 50 ns
	-6	0	0	1	1	1	1	0	0	3C	t_{RAC} = 60 ns
10	$\overline{CAS}$ access time										
	-5	0	0	0	0	1	1	0	1	0D	t_{CAC} = 13 ns
	-6	0	0	0	0	1	1	1	1	0F	t_{CAC} = 15 ns
11	Module configuration type										
	(HB56UW873EJN)	0	0	0	0	0	0	1	0	02	ECC
	(HB56UW865EJN)	0	0	0	0	0	0	0	0	00	Non parity
12	Refresh rate/type	0	0	0	0	0	0	0	0	00	Normal (15.625 μs)
13	DRAM width	0	0	0	0	1	0	0	0	08	8M × 8
14	Error checking DRAM width										
	(HB56UW873EJN)	0	0	0	0	1	0	0	0	08	8M × 8
	(HB56UW865EJN)	0	0	0	0	0	0	0	0	00	—
15 to 31	Reserved for future offerings	0	0	0	0	0	0	0	0	00	
32 to 61	Superset information	0	0	0	0	0	0	0	0	00	Future offerings
62	SPD data revision code	0	0	0	0	0	0	0	1	01	Rev.1
63	Checksum for bytes 0 to 62										
	(HB56UW873EJN-5)	0	0	1	1	1	1	0	1	3D	
	(HB56UW873EJN-6)	0	1	0	0	1	0	0	1	49	
	(HB56UW865EJN-5)	0	0	1	0	1	0	1	1	2B	
	(HB56UW865EJN-6)	0	0	1	1	0	1	1	1	37	

Serial PD Matrix*[1](cont)

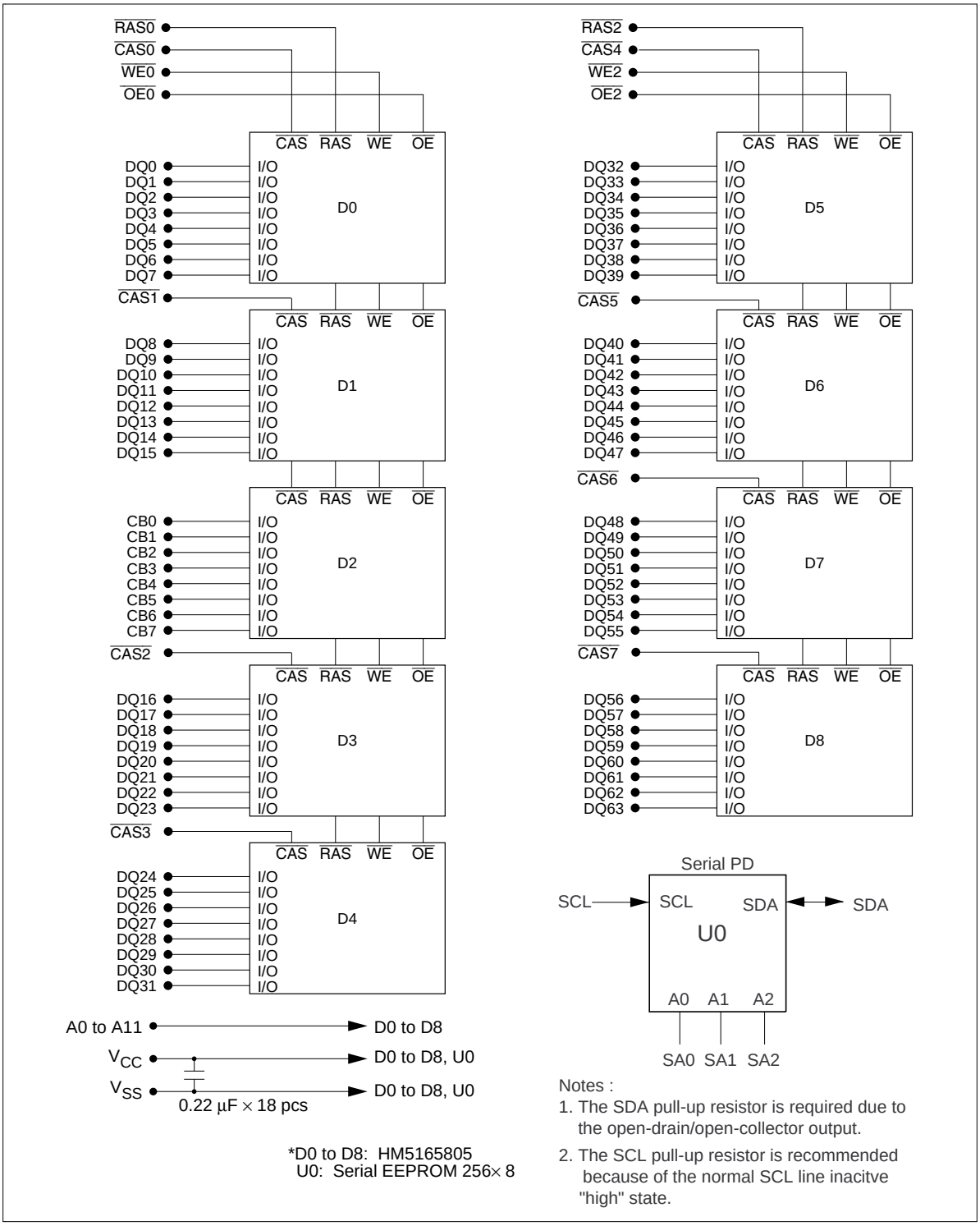
Byte No.	Function described	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Hex value	Comments
64	Manufacturer's JEDEC ID code	0	0	0	0	0	1	1	1	07	HITACHI
65 to 71	Manufacturer's JEDEC ID code	0	0	0	0	0	0	0	0	00	
72	Manufacturing location	×	×	×	×	×	×	×	×	××	*[2] (ASCII-8bit code)
73	Manufacturer's part number	0	1	0	0	1	0	0	0	48	H
74	Manufacturer's part number	0	1	0	0	0	0	1	0	42	B
75	Manufacturer's part number	0	0	1	1	0	1	0	1	35	5
76	Manufacturer's part number	0	0	1	1	0	1	1	0	36	6
77	Manufacturer's part number	0	1	0	1	0	1	0	1	55	U
78	Manufacturer's part number	0	1	0	1	0	1	1	1	57	W
79	Manufacturer's part number	0	0	1	1	1	0	0	0	38	8
80	Manufacturer's part number (HB56UW873EJN)	0	0	1	1	0	1	1	1	37	7
	(HB56UW865EJN)	0	0	1	1	0	1	1	0	36	6
81	Manufacturer's part number (HB56UW873EJN)	0	0	1	1	0	0	1	1	33	3
	(HB56UW865EJN)	0	0	1	1	0	1	0	1	35	5
82	Manufacturer's part number	0	1	0	0	0	1	0	1	45	E
83	Manufacturer's part number	0	1	0	0	1	0	1	0	4A	J
84	Manufacturer's part number	0	1	0	0	1	1	1	0	4E	N
85	Manufacturer's part number	0	0	1	0	1	1	0	1	2D	—
86	Manufacturer's part number -5	0	0	1	1	0	1	0	1	35	5
	-6	0	0	1	1	0	1	1	0	36	6
87	Manufacturer's part number	0	0	1	0	0	0	0	0	20	(Space)
88	Manufacturer's part number	0	0	1	0	0	0	0	0	20	(Space)
89	Manufacturer's part number	0	0	1	0	0	0	0	0	20	(Space)
90	Manufacturer's part number	0	0	1	0	0	0	0	0	20	(Space)
91	Revision code	0	0	1	1	0	0	0	0	30	Initial
92	Revision code	0	0	1	0	0	0	0	0	20	(Space)
93	Manufacturing date	×	×	×	×	×	×	×	×	××	Year code (binary) *[3]
94	Manufacturing date	×	×	×	×	×	×	×	×	××	Week code (binary) *[4]

Serial PD Matrix*[1](cont)

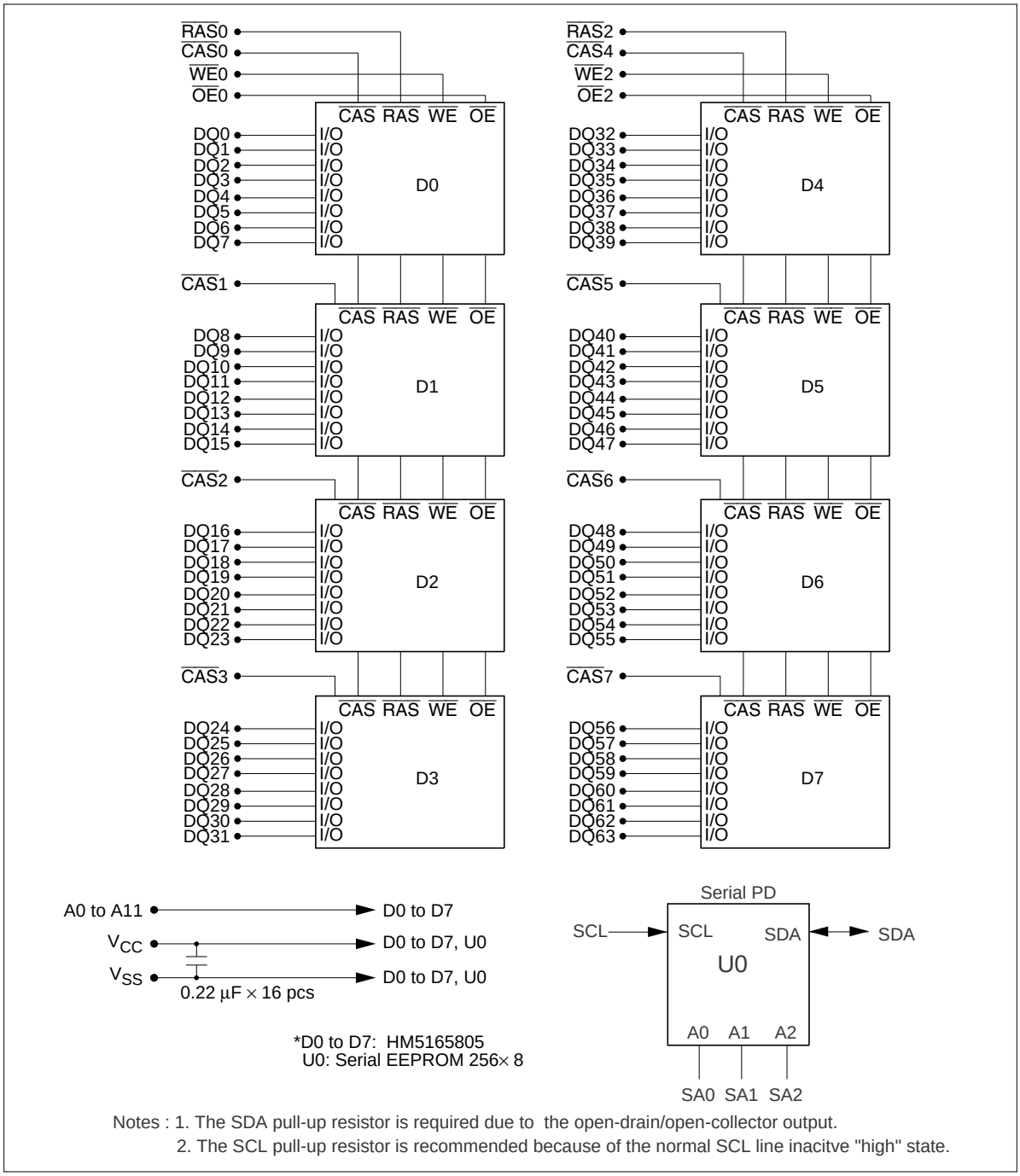
Byte No.	Function described	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Hex value	Comments
95 to 98	Assembly serial number	*[5]									
99 to 125	Manufacturer specific data	*[6]									
126	Reserved	0	0	0	0	0	0	0	0	00	Not use
127	Reserved	0	0	0	0	0	0	0	0	00	Not use

Notes: 1. All serial PD data are not protected. 0: Serial data, “driven Low”, 1: Serial data, “driven High”
2. Byte 72 is manufacturing location code. (ex: In case of Japan, byte 72 is 4Ah. 4Ah shows “J” on ASCII code.)
3. Byte 93 (Manufacturing date-year code) ex: 61h shows year ’97. 62h shows year’98.
4. Byte 94 (Manufacturing date-week code) ex: 0Bh shows week 11. 24h shows week 36.
5. Byte 95 through 98 are assembly serial number.
6. All bits of 99 through 125 are not defined (“1” or “0”).

Block Diagram (HB56UW873EJN)



Block Diagram (HB56UW865EJN)



Notes : 1. The SDA pull-up resistor is required due to the open-drain/open-collector output.
2. The SCL pull-up resistor is recommended because of the normal SCL line inacitve "high" state.

Absolute Maximum Ratings (HB56UW873EJN)

Parameter	Symbol	Value	Unit
Terminal voltage on any pin relative to V_{SS}	V_T	–0.5 to +4.6	V
Power supply voltage relative to V_{SS}	V_{CC}	–0.5 to +4.6	V
Short circuit output current	Iout	50	mA
Power dissipation	P_T	9.0	W
Storage temperature range	Tstg	–55 to +125	°C

Absolute Maximum Ratings (HB56UW865EJN)

Parameter	Symbol	Value	Unit
Terminal voltage on any pin relative to V_{SS}	V_T	–0.5 to +4.6	V
Power supply voltage relative to V_{SS}	V_{CC}	–0.5 to +4.6	V
Short circuit output current	Iout	50	mA
Power dissipation	P_T	8.0	W
Storage temperature	Tstg	–55 to +125	°C

DC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply voltage	V_{CC}	3.0	3.3	3.6	V	1, 2
	V_{SS}	0	0	0	V	2
Input high voltage	V_{IH}	2.0	—	V_{CC} + 0.3	V	1
Input low voltage	V_{IL}	–0.3	—	0.8	V	1
Ambient temperature range	Ta	0	—	70	°C	

Note: 1. All voltage referred to V_{SS}.
2. The supply voltage with all V_{CC} pins must be on the same level. The supply voltage with all V_{SS} pins must be on the same level.

DC Characteristics (HB56UW873EJN)

		HB56UW873EJN					
		50 ns		60 ns			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test conditions**
Operating current*1, *2	I_{CC1}	—	1215	—	1035	mA	t_{RC} = min
Standby current	I_{CC2}	—	18	—	18	mA	TTL interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH} Dout = High-Z
		—	4.5	—	4.5	mA	CMOS interface $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} – 0.2 V Dout = High-Z
$\overline{RAS}$-only refresh current*2	I_{CC3}	—	1215	—	1035	mA	t_{RC} = min
Standby current*1	I_{CC5}	—	45	—	45	mA	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL} Dout = enable
$\overline{CAS}$-before-$\overline{RAS}$ refresh current	I_{CC6}	—	1215	—	1035	mA	t_{RC} = min
EDO page mode current*1, *3	I_{CC7}	—	990	—	900	mA	$\overline{RAS}$ = V_{IL} , $\overline{CAS}$ cycle, t_{HPC} = t_{HPC} min
Input leakage current	I_{LI}	–5	5	–5	5	µA	0 V ≤ Vin ≤ V_{CC} + 0.3 V
Output leakage current	I_{LO}	–5	5	–5	5	µA	0 V ≤ Vout ≤ V_{CC} Dout = disable
Output high voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	V	High Iout = –2 mA
Output low voltage	V_{OL}	0	0.4	0	0.4	V	Low Iout = 2 mA

Notes : 1. I_{CC} depends on output load condition when the device is selected. I_{CC} max is specified at the output open condition.

2. Address can be changed once or less while $\overline{RAS}$ = V_{IL}.

3. Measured with one sequential address change per EDO cycle, t_{HPC}.

DC Characteristics (HB56UW865EJN)

		HB56UW865EJN					
		50 ns		60 ns			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test conditions**
Operating current*1, *2	I_{CC1}	—	1080	—	920	mA	t_{RC} = min
Standby current	I_{CC2}	—	16	—	16	mA	TTL interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH} Dout = High-Z
		—	4	—	4	mA	CMOS interface $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} – 0.2 V Dout = High-Z
$\overline{RAS}$-only refresh current*2	I_{CC3}	—	1080	—	920	mA	t_{RC} = min
Standby current*1	I_{CC5}	—	40	—	40	mA	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL} Dout = enable
$\overline{CAS}$-before-$\overline{RAS}$ refresh current	I_{CC6}	—	1080	—	920	mA	t_{RC} = min
EDO page mode current*1, *3	I_{CC7}	—	880	—	800	mA	$\overline{RAS}$ = V_{IL} , $\overline{CAS}$ cycle, t_{HPC} = t_{HPC} min
Input leakage current	I_{LI}	–5	5	–5	5	µA	0 V ≤ Vin ≤ V_{CC} + 0.3 V
Output leakage current	I_{LO}	–5	5	–5	5	µA	0 V ≤ Vout ≤ V_{CC} Dout = disable
Output high voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	V	High Iout = –2 mA
Output low voltage	V_{OL}	0	0.4	0	0.4	V	Low Iout = 2 mA

Notes : 1. I_{CC} depends on output load condition when the device is selected. I_{CC} max is specified at the output open condition.

2. Address can be changed once or less while $\overline{RAS}$ = V_{IL}.

3. Measured with one sequential address change per EDO cycle, t_{HPC}.

Capacitance (Ta = 25°C, V_{CC} = 3.3 V ± 0.3 V) (HB56UW873EJN)

Parameter	Symbol	Typ	Max	Unit	Notes
Input capacitance (Address)	C_{I1}	—	65	pF	1
Input capacitance ($\overline{CAS}$)	C_{I2}	—	34	pF	1
Input capacitance ($\overline{RAS}$, $\overline{WE}$, $\overline{OE}$)	C_{I3}	—	55	pF	1
I/O capacitance (DQ)	$C_{I/O}$	—	20	pF	1, 2

Notes : 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable Dout.

Capacitance (Ta = 25°C, V_{CC} = 3.3 V ± 0.3 V) (HB56UW865EJN)

Parameter	Symbol	Typ	Max	Unit	Notes
Input capacitance (Address)	C_{I1}	—	60	pF	1
Input capacitance ($\overline{CAS}$)	C_{I2}	—	27	pF	1
Input capacitance ($\overline{RAS}$, $\overline{WE}$, $\overline{OE}$)	C_{I3}	—	48	pF	1
I/O capacitance (DQ)	$C_{I/O}$	—	20	pF	1, 2

Notes : 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable Dout.

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 3.3 V ± 0.3 V, V_{SS} = 0 V) *[1], *[2], *[19]

Test Conditions

- Input rise and fall time: 2 ns
- Input levels: V_{IL} = 0 V, V_{IH} = 3 V
- Input timing reference levels: 0.8 V, 2.0 V
- Output timing reference levels: 0.8 V, 2.0 V
- Output load: 1 TTL gate + C_L (100 pF) (Including scope and jig)

Read, Write, Read-Modify-Write and Refresh Cycles (Common parameters)

		50 ns		60 ns			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Random read or write cycle time	t_{RC}	84	—	104	—	ns	
$\overline{RAS}$ precharge time	t_{RP}	30	—	40	—	ns	
$\overline{CAS}$ precharge time	t_{CP}	8	—	10	—	ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10000	60	10000	ns	
$\overline{CAS}$ pulse width	t_{CAS}	8	10000	10	10000	ns	
Row address setup time	t_{ASR}	0	—	0	—	ns	
Row address hold time	t_{RAH}	8	—	10	—	ns	
Column address setup time	t_{ASC}	0	—	0	—	ns	
Column address hold time	t_{CAH}	8	—	10	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	12	37	14	45	ns	3
$\overline{RAS}$ to column address delay time	t_{RAD}	10	25	12	30	ns	4
$\overline{RAS}$ hold time	t_{RSH}	13	—	15	—	ns	
$\overline{CAS}$ hold time	t_{CSH}	35	—	40	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5	—	5	—	ns	
$\overline{OE}$ to Din delay time	t_{OED}	13	—	15	—	ns	5
$\overline{OE}$ delay time from Din	t_{DZO}	0	—	0	—	ns	6
$\overline{CAS}$ delay time from Din	t_{DZC}	0	—	0	—	ns	6
Transition time (rise and fall)	t_T	2	50	2	50	ns	7

Read Cycle

		50 ns		60 ns			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Access time from $\overline{RAS}$	t_{RAC}	—	50	—	60	ns	8, 9
Access time from $\overline{CAS}$	t_{CAC}	—	13	—	15	ns	9, 10, 17
Access time from address	t_{AA}	—	25	—	30	ns	9, 11, 17
Access time from $\overline{OE}$	t_{OEA}	—	13	—	15	ns	9
Read command setup time	t_{RCS}	0	—	0	—	ns	
Read command hold time to $\overline{CAS}$	t_{RCH}	0	—	0	—	ns	12
Read command hold time from $\overline{RAS}$	t_{RCHR}	50	—	60	—	ns	
Read command hold time to $\overline{RAS}$	t_{RRH}	0	—	0	—	ns	12
Column address to $\overline{RAS}$ lead time	t_{RAL}	25	—	30	—	ns	
Column address to $\overline{CAS}$ lead time	t_{CAL}	15	—	18	—	ns	
$\overline{CAS}$ to output in low-Z	t_{CLZ}	0	—	0	—	ns	
Output data hold time	t_{OH}	3	—	3	—	ns	21
Output data hold time from $\overline{OE}$	t_{OHO}	3	—	3	—	ns	
Output buffer turn-off time	t_{OFF}	—	13	—	15	ns	13, 21
Output buffer turn-off to $\overline{OE}$	t_{OEZ}	—	13	—	15	ns	13
$\overline{CAS}$ to Din delay time	t_{CDD}	13	—	15	—	ns	5
Output data hold time from $\overline{RAS}$	t_{OHR}	3	—	3	—	ns	21
Output buffer turn-off to $\overline{RAS}$	t_{OFR}	—	13	—	15	ns	13, 21
Output buffer turn-off to $\overline{WE}$	t_{WEZ}	—	13	—	15	ns	13
$\overline{WE}$ to Din delay time	t_{WED}	13	—	15	—	ns	
$\overline{RAS}$ to Din delay time	t_{RDD}	13	—	15	—	ns	

Write Cycle

		50 ns		60 ns			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Write command setup time	t_{WCS}	0	—	0	—	ns	14
Write command hold time	t_{WCH}	8	—	10	—	ns	
Write command pulse width	t_{WP}	8	—	10	—	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	13	—	15	—	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	8	—	10	—	ns	
Data-in setup time	t_{DS}	0	—	0	—	ns	15
Data-in hold time	t_{DH}	8	—	10	—	ns	15

Read-Modify-Write Cycle

		50 ns		60 ns			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Read-modify-write cycle time	t_{RWC}	116	—	140	—	ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	t_{RWD}	67	—	79	—	ns	14
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	30	—	34	—	ns	14
Column address to $\overline{WE}$ delay time	t_{AWD}	42	—	49	—	ns	14
$\overline{OE}$ hold time from $\overline{WE}$	t_{OEH}	13	—	15	—	ns	

Refresh Cycle

		50 ns		60 ns			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
$\overline{CAS}$ setup time (CBR refresh cycle)	t_{CSR}	5	—	5	—	ns	
$\overline{CAS}$ hold time (CBR refresh cycle)	t_{CHR}	8	—	10	—	ns	
$\overline{WE}$ setup time (CBR refresh cycle)	t_{WRP}	0	—	0	—	ns	
$\overline{WE}$ hold time (CBR refresh cycle)	t_{WRH}	8	—	10	—	ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	5	—	5	—	ns	

EDO Page Mode Cycle

		50 ns		60 ns			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
EDO page mode cycle time	t_{HPC}	20	—	25	—	ns	20
EDO page mode $\overline{RAS}$ pulse width	t_{RASP}	—	100000	—	100000	ns	16
Access time from $\overline{CAS}$ precharge	t_{CPA}	—	28	—	35	ns	9, 17
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{CPRH}	28	—	35	—	ns	
Output data hold time from $\overline{CAS}$ low	t_{DOH}	3	—	3	—	ns	9, 22
$\overline{CAS}$ hold time referred $\overline{OE}$	t_{COL}	8	—	10	—	ns	
$\overline{CAS}$ to $\overline{OE}$ setup time	t_{COP}	5	—	5	—	ns	
Read command hold time from $\overline{CAS}$ precharge	t_{RCHC}	28	—	35	—	ns	
Write pulse width during $\overline{CAS}$ precharge	t_{WPE}	8	—	10	—	ns	
$\overline{OE}$ precharge time	t_{OEP}	8	—	10	—	ns	

EDO Page Mode Read-Modify-Write Cycle

		50 ns		60 ns			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
EDO page mode read- modify-write cycle time	t_{HPRWC}	57	—	68	—	ns	
$\overline{WE}$ delay time from $\overline{CAS}$ precharge	t_{CPW}	45	—	54	—	ns	14

Refresh

Parameter	**Symbol**	**Max**	**Unit**	**Notes**
Refresh period	t_{REF}	64	ms	4096 cycles

Notes:
1. AC measurements assume t_T = 2 ns.
2. An initial pause of 200 µs is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing $\overline{RAS}$-only refresh or $\overline{CAS}$-before-$\overline{RAS}$ refresh).
3. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, than the access time is controlled exclusively by t_{CAC}.
4. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
5. Either t_{OED} or t_{CDD} must be satisfied.
6. Either t_{DZO} or t_{DZC} must be satisfied.
7. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min) and V_{IL} (max).
8. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
9. Measured with a load circuit equivalent to 1 TTL loads and 100 pF.
10. Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RCD} + t_{CAC}$ (max) $\geq t_{RAD} + t_{AA}$ (max).
11. Assumes that $t_{RAD} \geq t_{RAD}$ (max) and $t_{RCD} + t_{CAC}$ (max) $\leq t_{RAD} + t_{AA}$ (max).
12. Either t_{RCH} or t_{RRH} must be satisfied for a read cycles.
13. t_{OFF} (max), t_{OEZ} (max), t_{WEZ} (max) and t_{OFR} (max) define the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.
14. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPW} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}$ (min), $t_{CWD} \geq t_{CWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), or $t_{CWD} \geq t_{CWD}$ (min), $t_{AWD} \geq t_{AWD}$ (min) and $t_{CPW} \geq t_{CPW}$ (min), the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
15. t_{DS} and t_{DH} are referred to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in delayed write or read-modify-write cycles.
16. t_{RASP} defines $\overline{RAS}$ pulse width in EDO page mode cycles.
17. Access time is determined by the longest among t_{AA}, t_{CAC} and t_{CPA}.

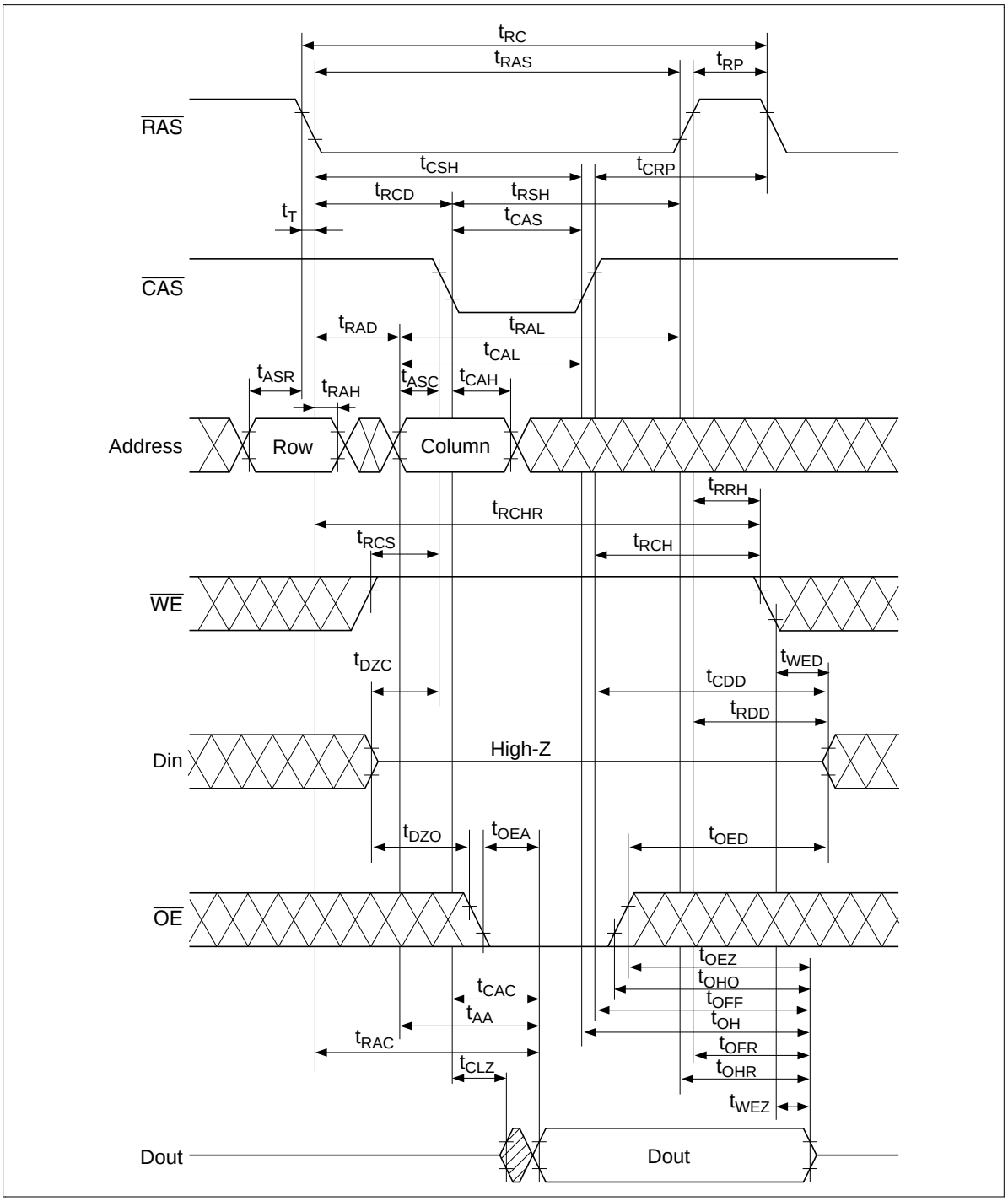
18. In delayed write or read-modify-write cycles, $\overline{OE}$ must disable output buffer prior to applying data to the device.
19. When output buffers are enabled once, sustain the low impedance state until valid data is obtained. When output buffer is turned on and off within a very short time, generally it causes large V_{CC}/V_{SS} line noise, which causes to degrade V_{IH} min/V_{IL} max level.
20. t_{HPC} (min) can be achieved during a series of EDO page mode write cycles or EDO page mode read cycles. If both write and read operation are mixed in a EDO page mode $\overline{RAS}$ cycle (EDO page mode mix cycle (1), (2)), minimum value of $\overline{CAS}$ cycle ($t_{CAS} + t_{CP} + 2\ t_T$) becomes greater than the specified t_{HPC} (min) value. The value of $\overline{CAS}$ cycle time of mixed EDO page mode is shown in EDO page mode mix cycle (1) and (2).
21. Data output turns off and becomes high impedance from later rising edge of $\overline{RAS}$ and $\overline{CAS}$. Hold time and turn off time are specified by the timing specifications of later rising edge of $\overline{RAS}$ and $\overline{CAS}$ between t_{OHR} and t_{OH} and between t_{OFR} and t_{OFF}.
22. t_{DOH} defines the time at which the output level go cross. V_{OL} = 0.8 V, V_{OH} = 2.0 V of output timing reference level.
23. XXX: H or L (H: V_{IH} (min) ≤ V_{IN} ≤ V_{IH} (max), L: V_{IL} (min) ≤ V_{IN} ≤ V_{IL} (max))

    ///////: Invalid Dout

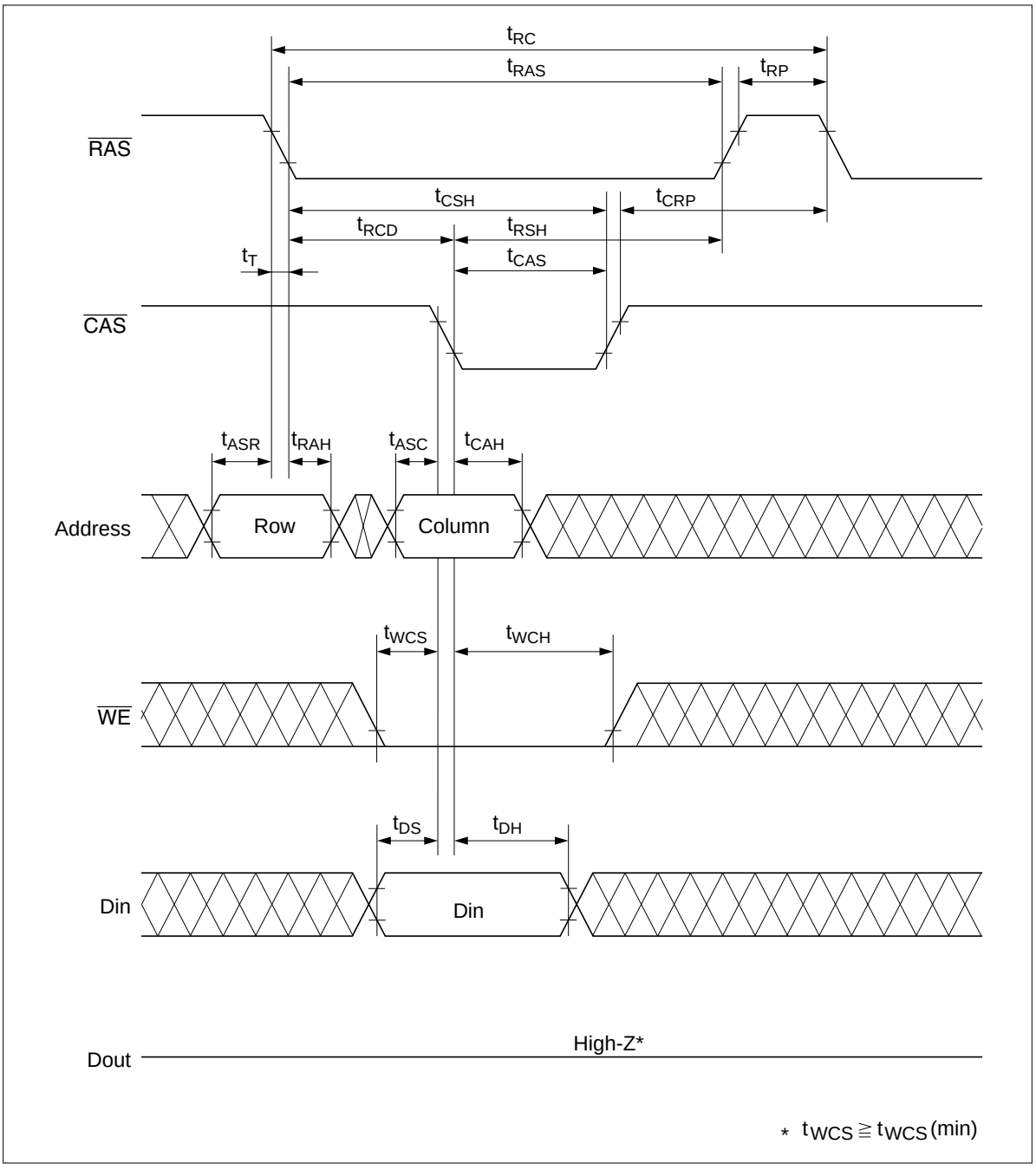
    When the address, clock and input pins are not described on timing waveforms, their pins must be applied V_{IH} or V_{IL}.

Timing Waveforms*[23]

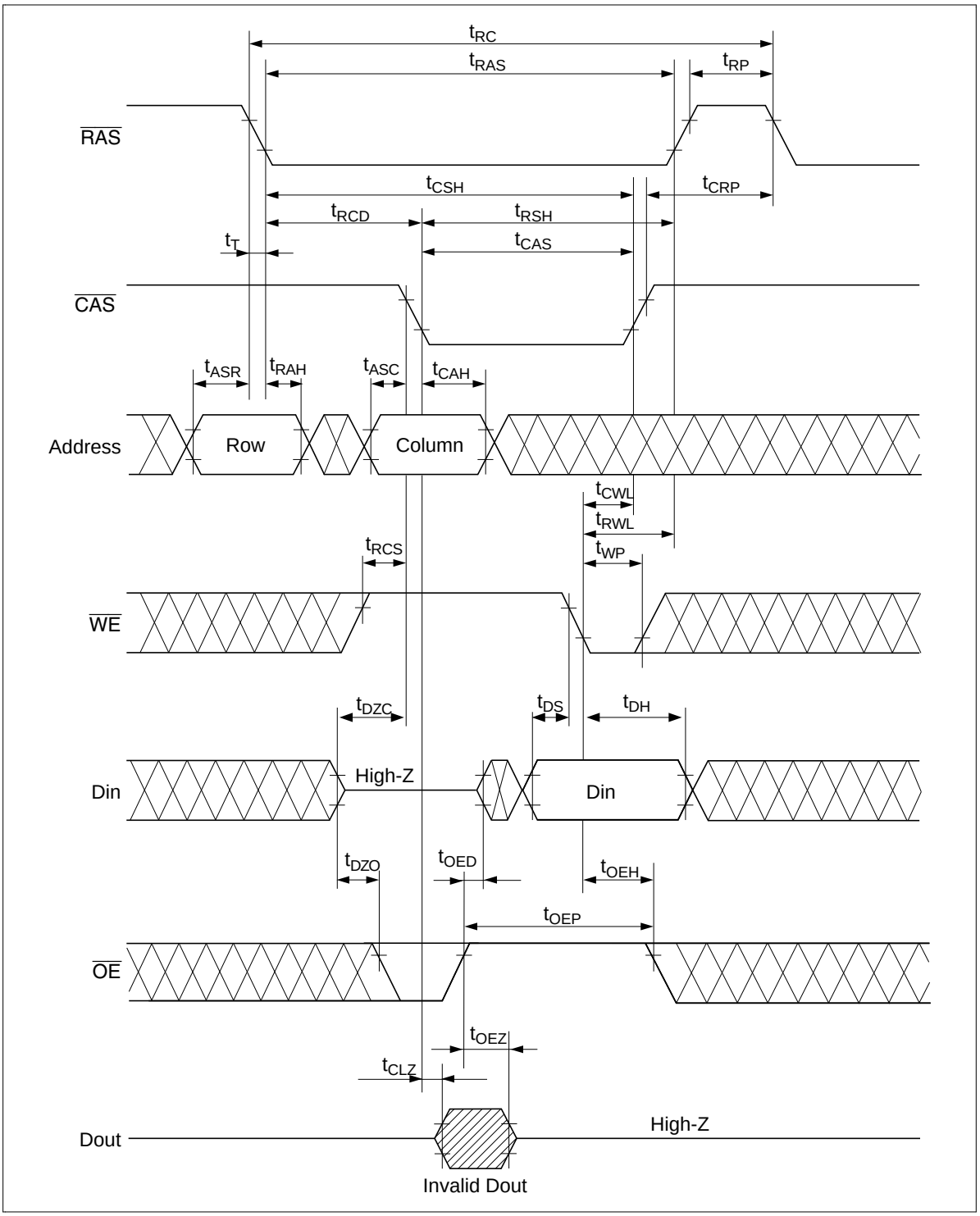
Read Cycle



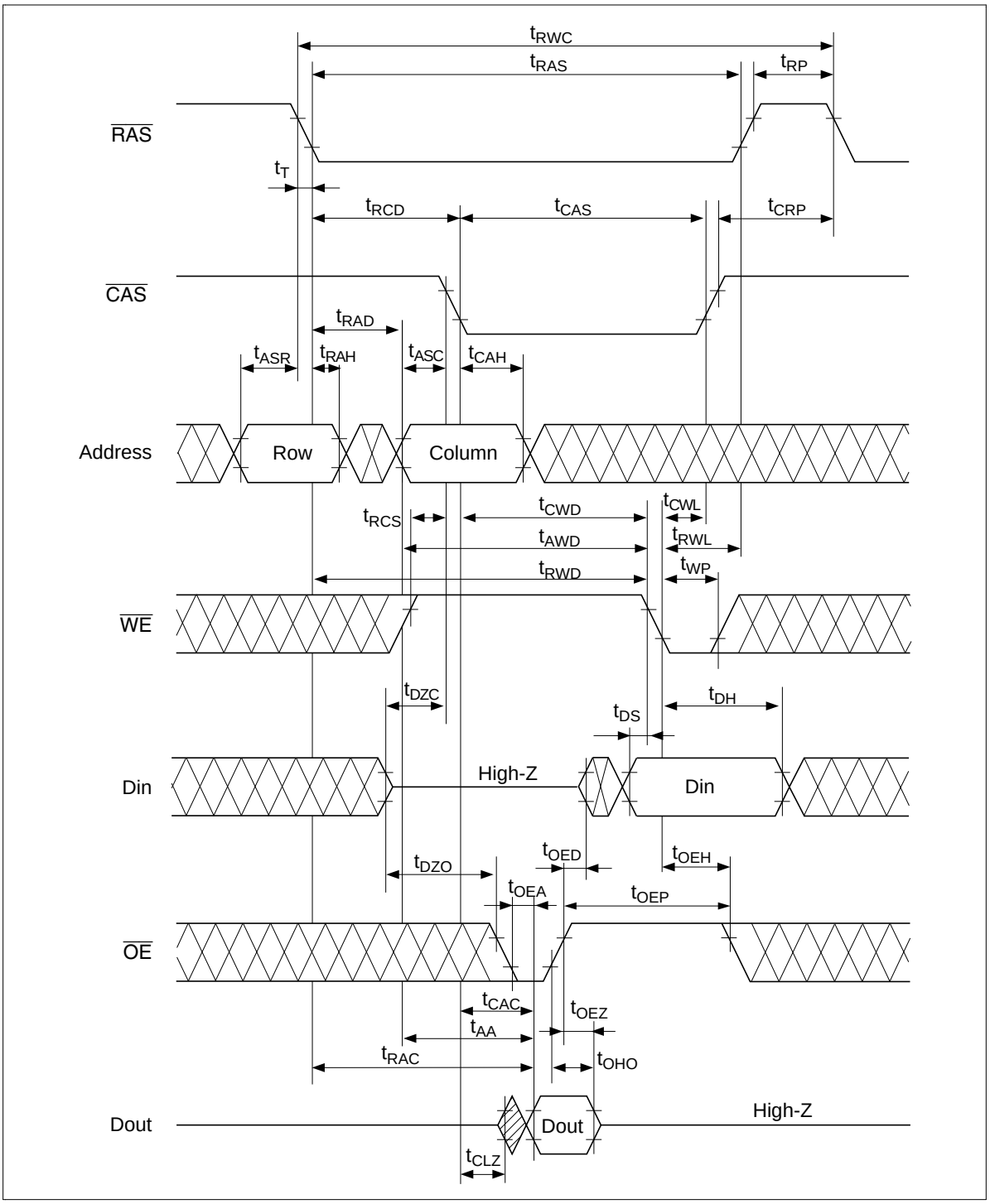
Early Write Cycle



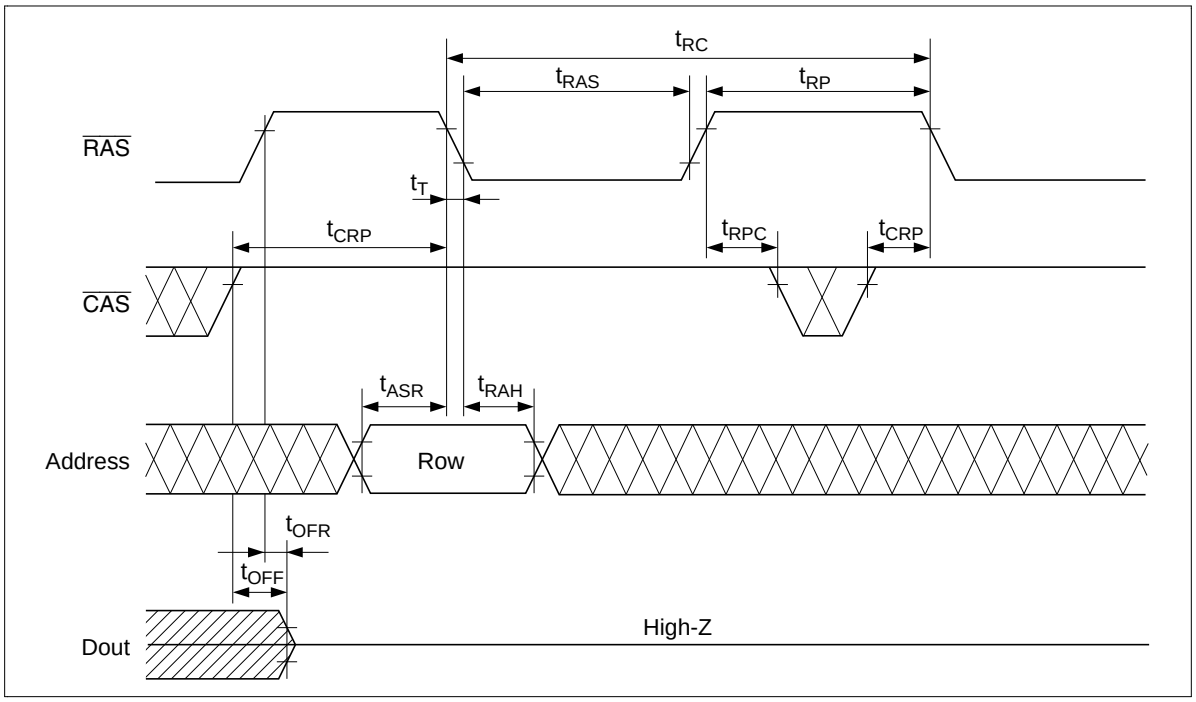
Delayed Write Cycle*[18]



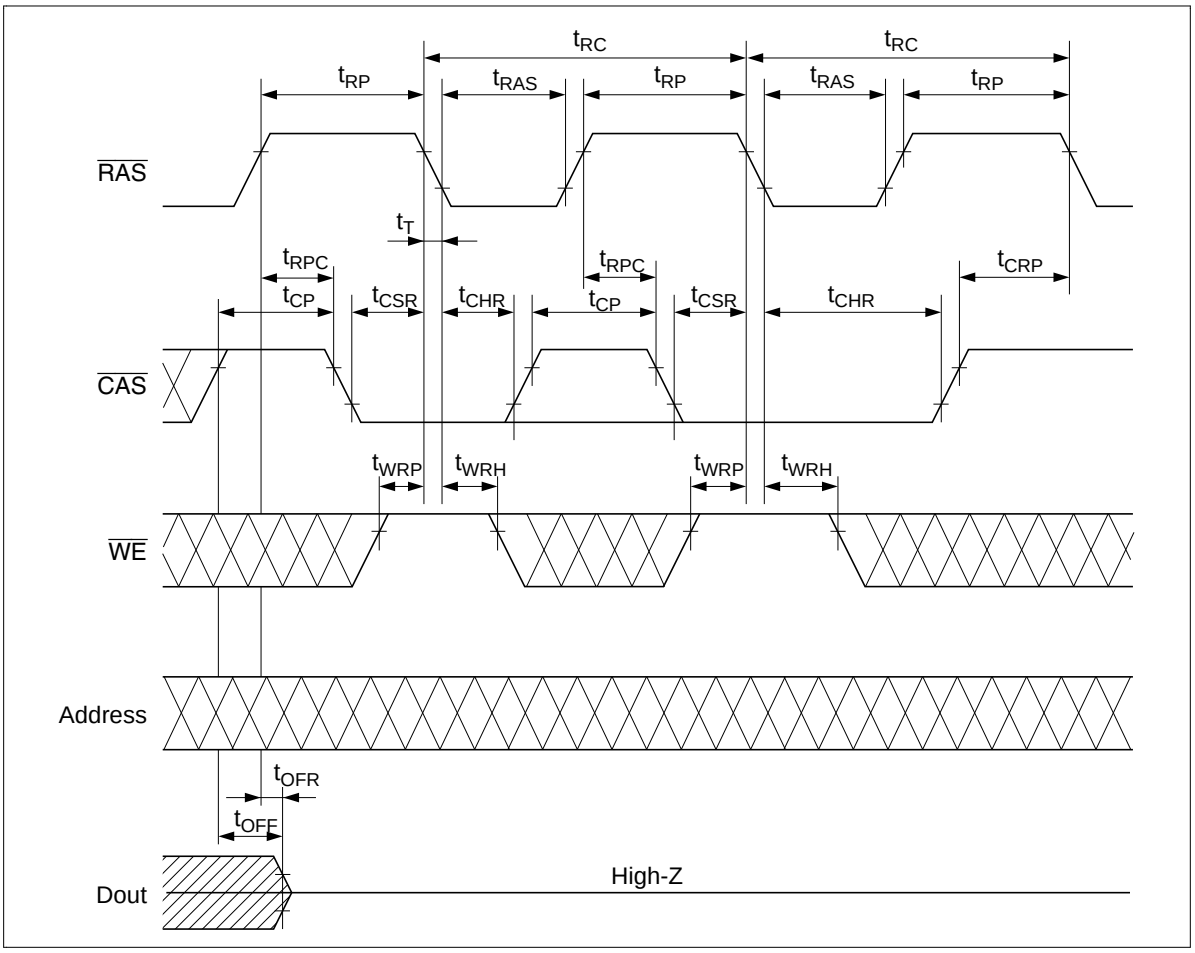
Read-Modify-Write Cycle*[18]



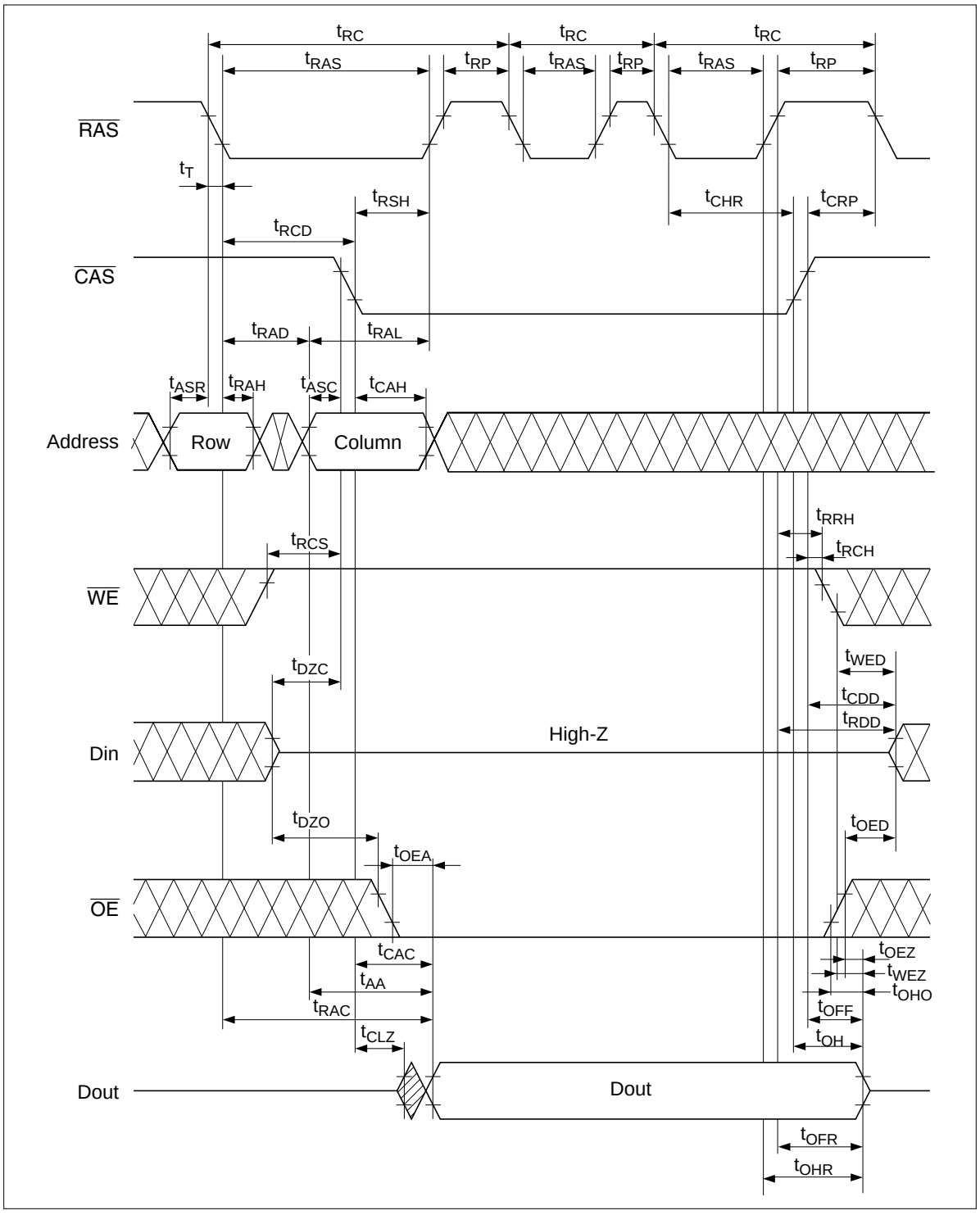
$\overline{\text{RAS}}$-Only Refresh Cycle



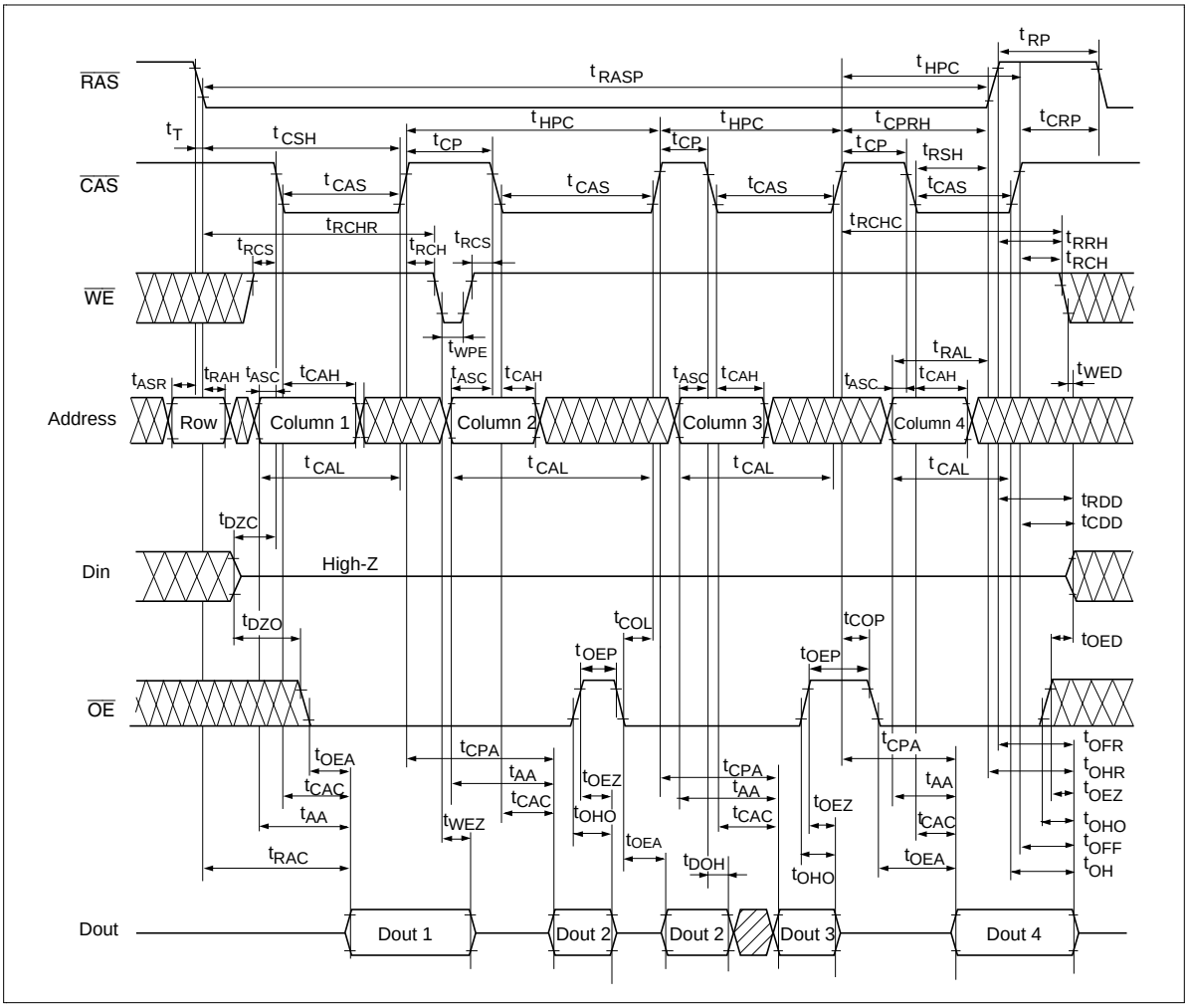
$\overline{\text{CAS}}$-Before-$\overline{\text{RAS}}$ Refresh Cycle



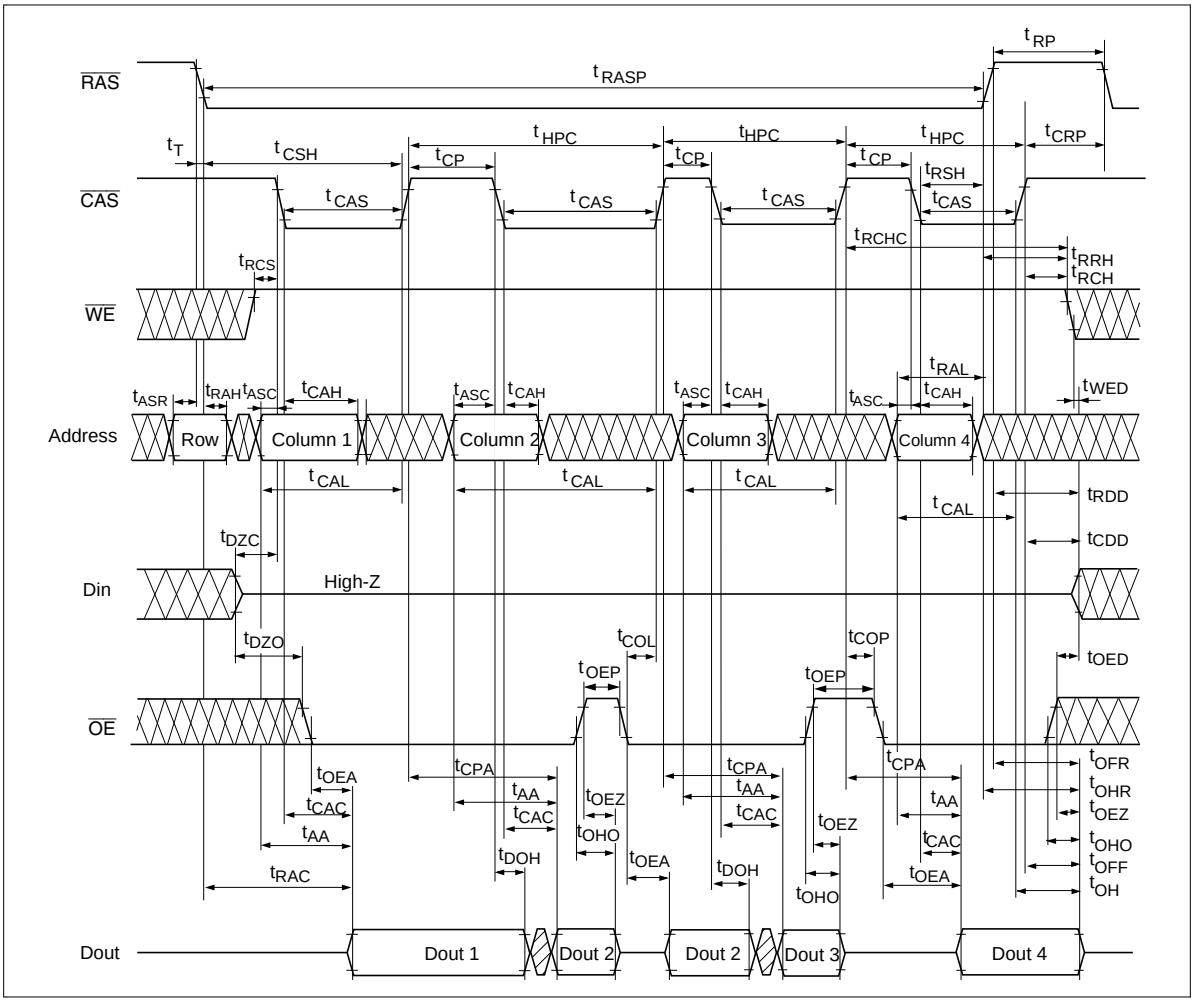
Hidden Refresh Cycle



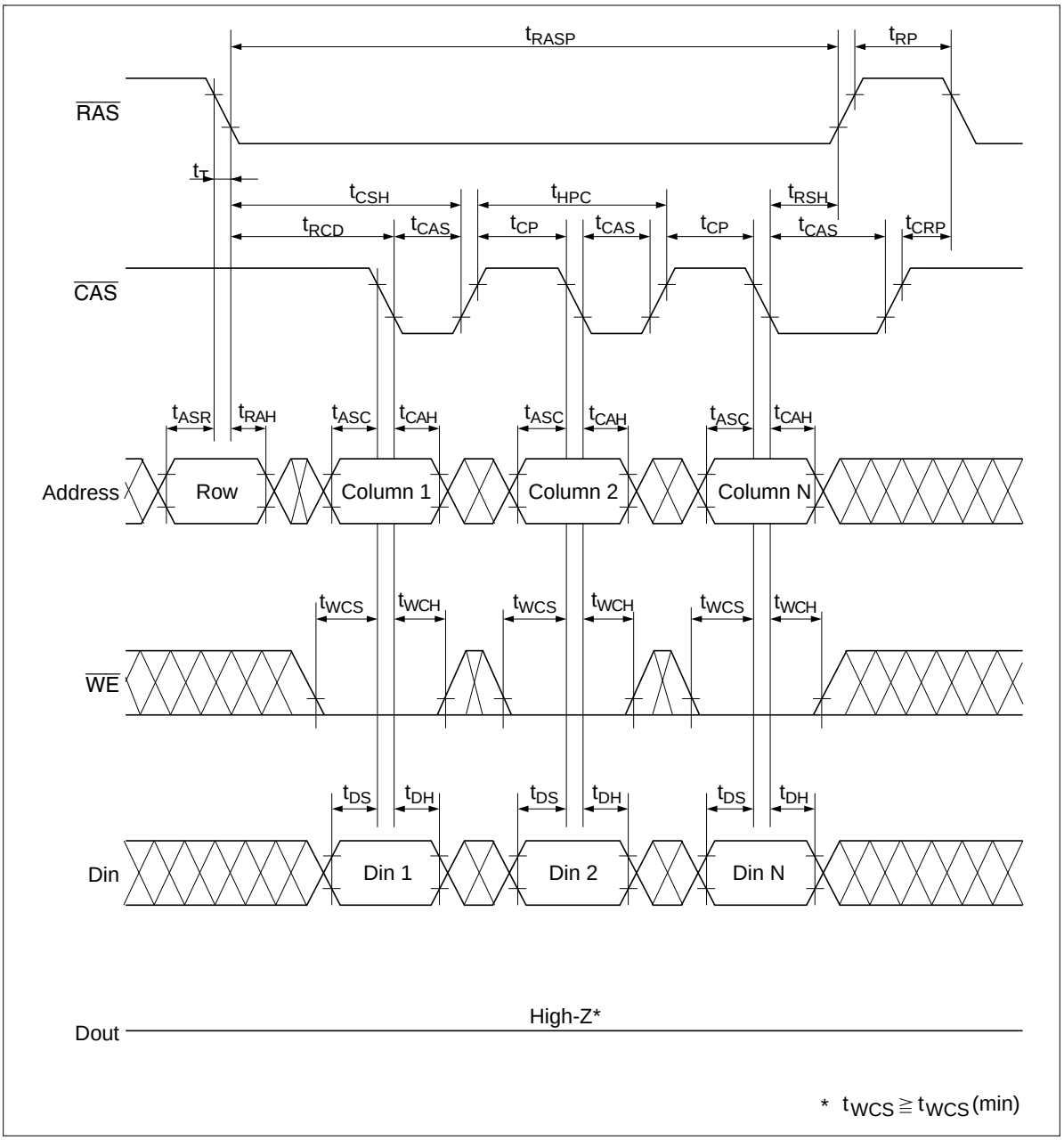
EDO Page Mode Read Cycle (1)



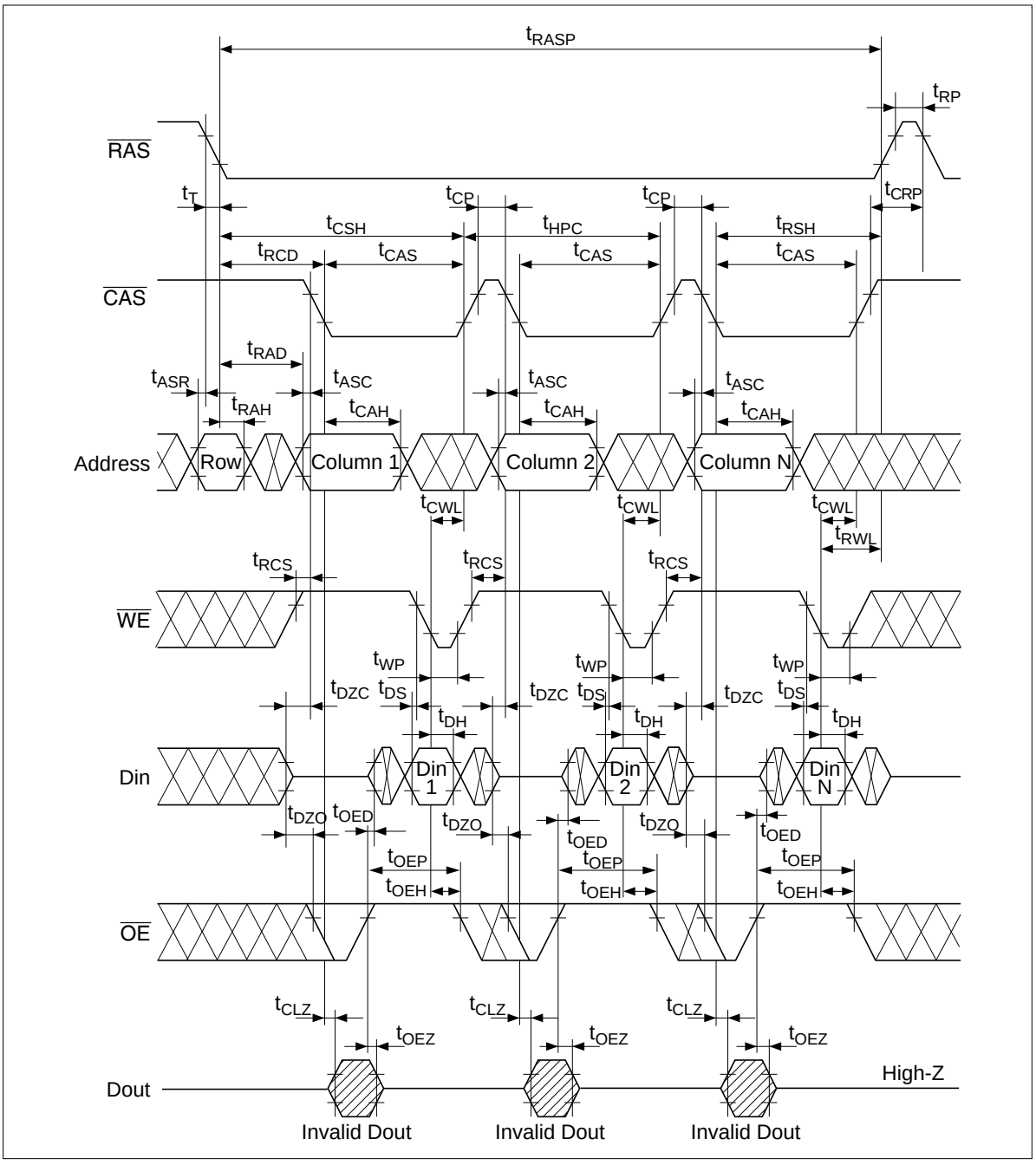
EDO Page Mode Read Cycle (2)



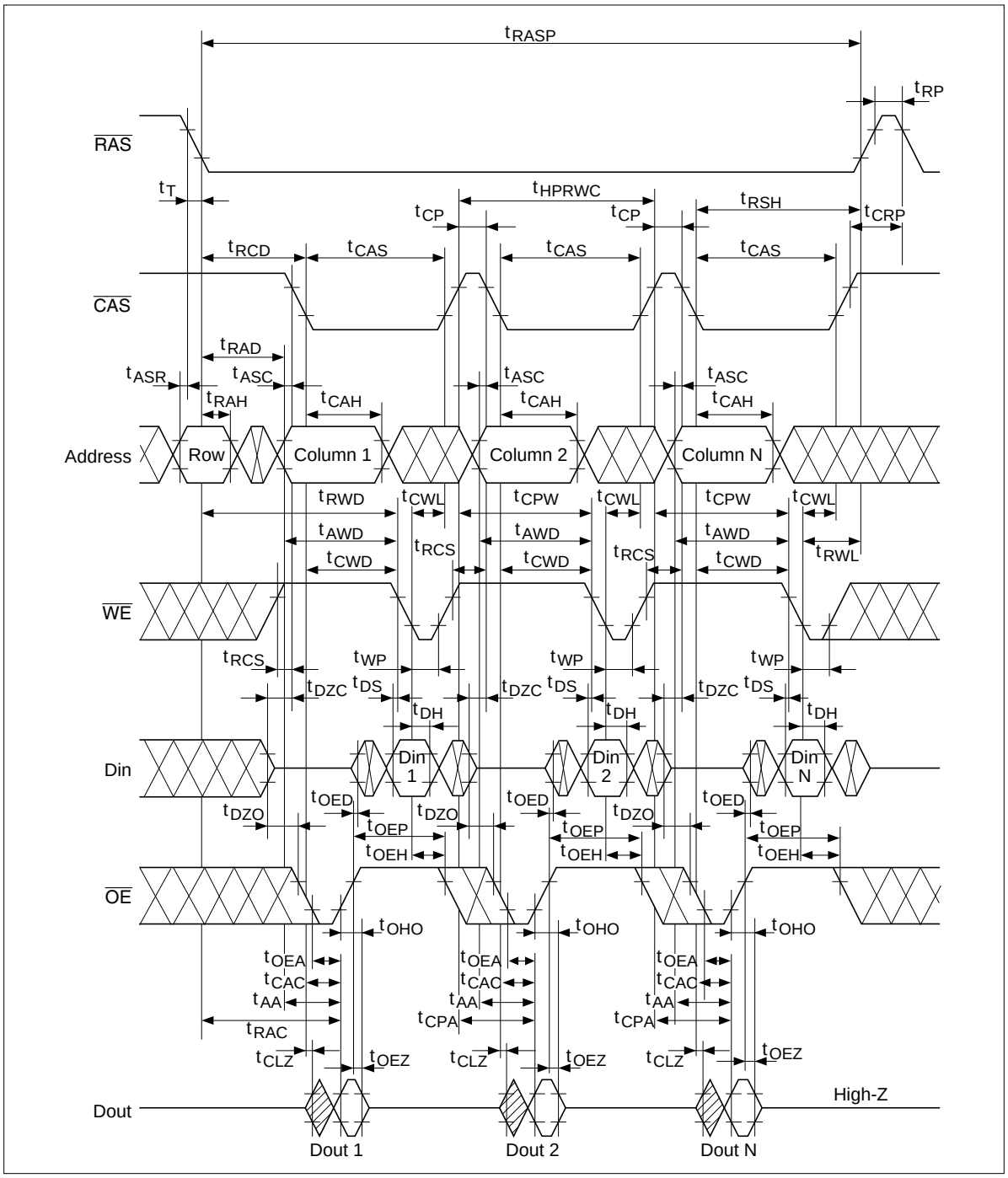
EDO Page Mode Early Write Cycle



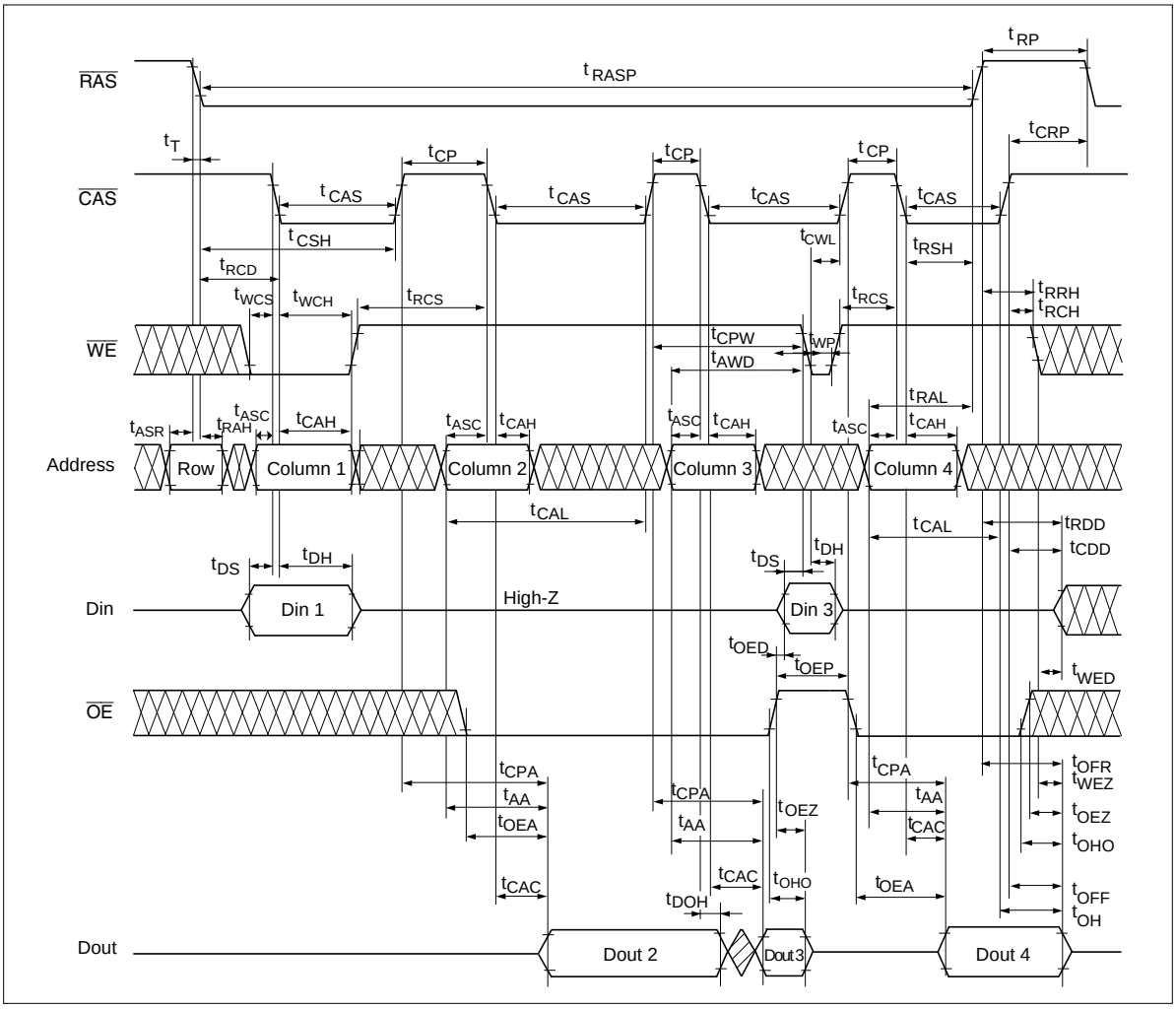
EDO Page Mode Delayed Write Cycle*[18]



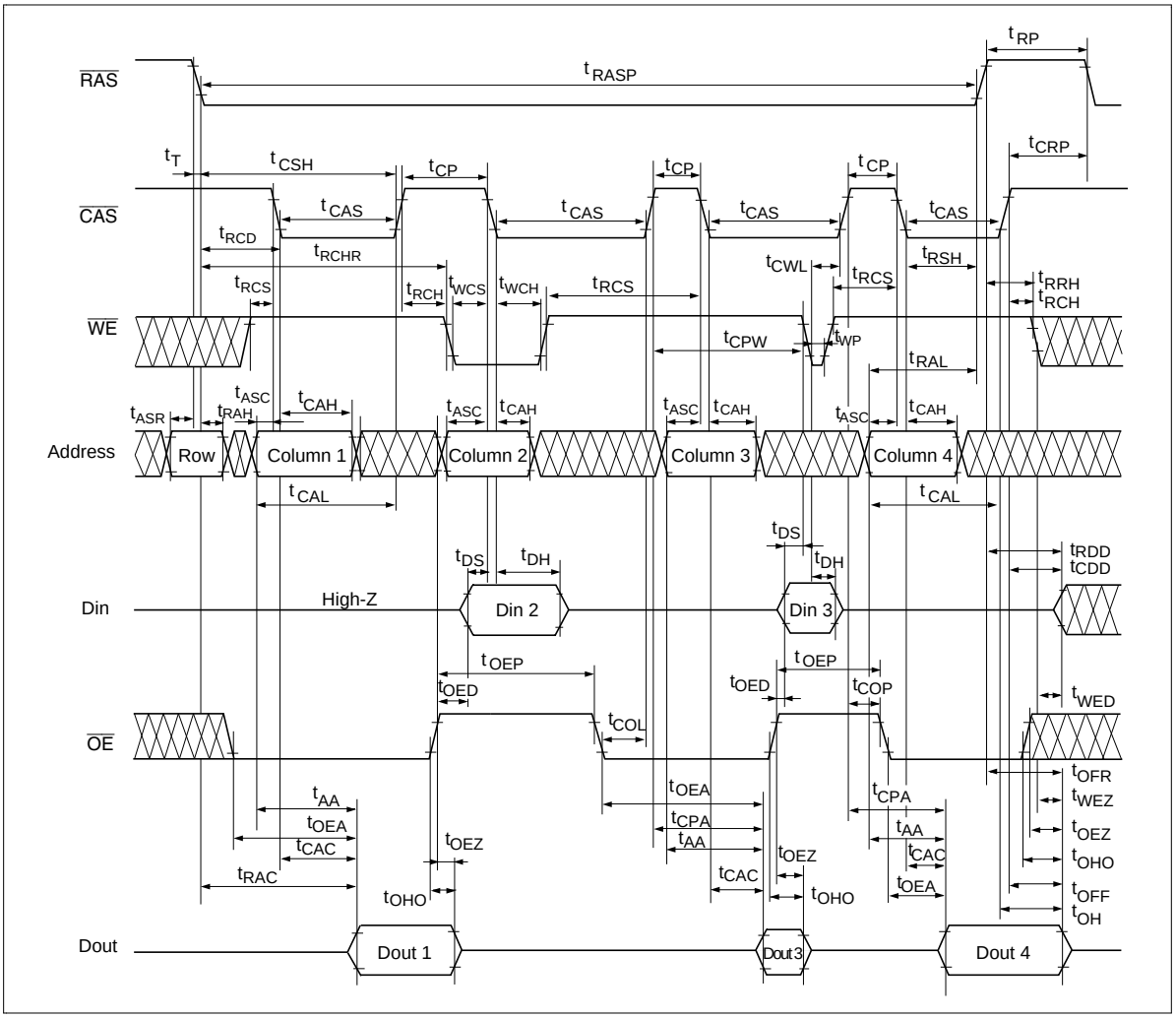
EDO Page Mode Read-Modify-Write Cycle*[18]



EDO Page Mode Mix Cycle (1) *[20]

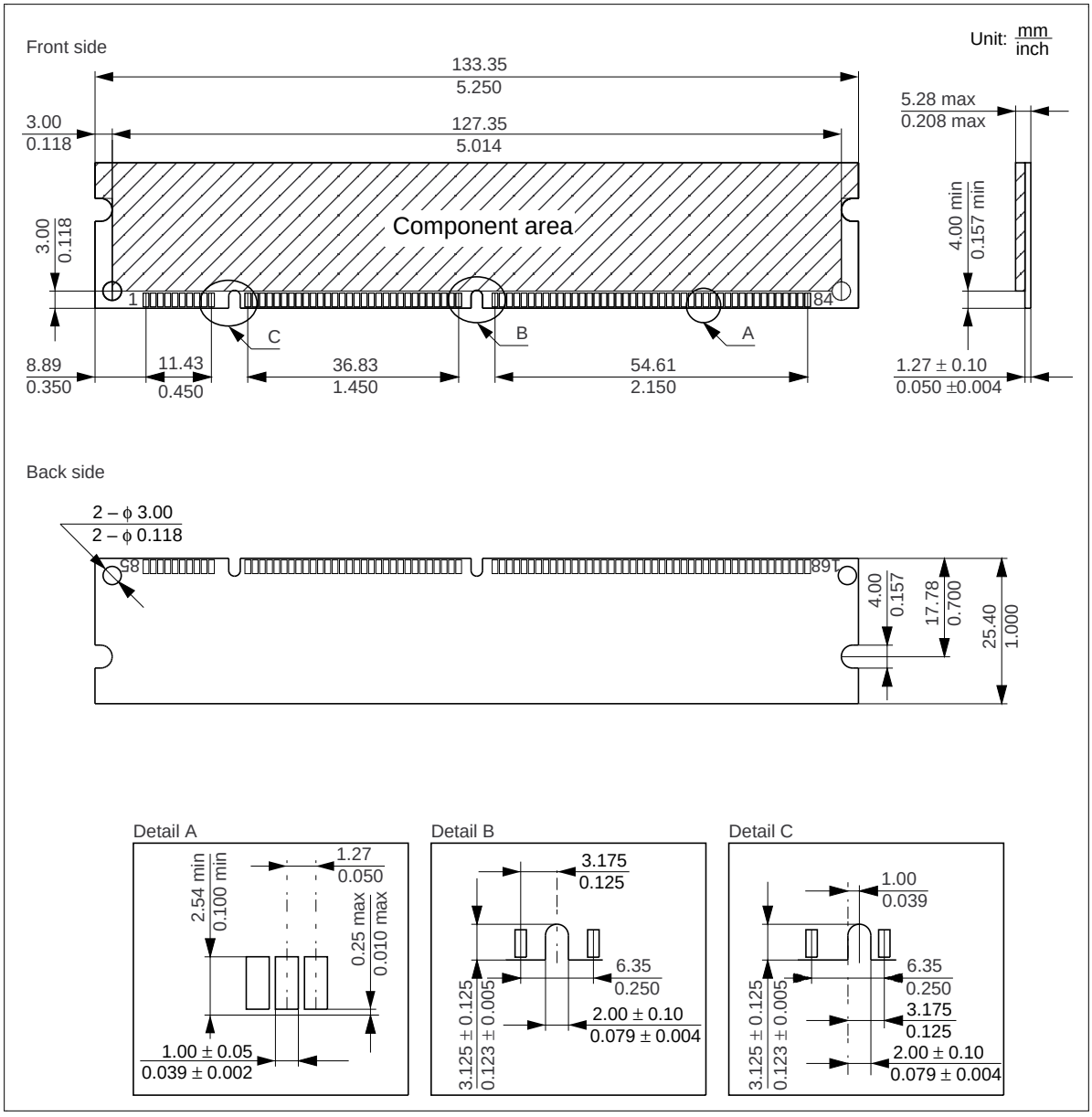


EDO Page Mode Mix Cycle (2) *[20]



Physical Outline

HB56UW873EJN Series,
HB56UW865EJN Series



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Revision Record

Rev.	Date	Contents of Modification	Drawn by	Approved by
0.0	Aug. 31, 1996	Initial issue	Y.Saitou	K.Tsuneda
1.0	May. 20, 1998	Deletion of Preliminary (referred to HM5164805/HM5165805 Series Rev.1.0) Refresh Cycle t_{WRH} min: 10/10 ns to 8/10 ns		