HB56A264EJ Series

2,097,152-word × 64-bit High Density Dynamic RAM Module

HITACHI

Preliminary

Description

The HB56A264EJ belongs to 8 byte DIMM (Dual In-line Memory Module) family, and has been developed as an optimized main memory solution for 4 and 8 Byte processor applications.

The HB56A264EJ is a 2 M × 64 dynamic RAM module, mounted 8 pieces of 16-Mbit DRAM (HM5117800BJ) sealed in SOJ package and 2 pieces of 16-bit BiCMOS line driver (74ABT16244) sealed in TSSOP package.

An outline of the HB56A264EJ is 168-pin socket type package (dual lead out). Therefore, the HB56A264EJ makes high density mounting possible without surface mount technology. The HB56A264EJ provides common data inputs and outputs. Decoupling capacitors are mounted beneath each SOJ on the module board.

Features

- 168-pin socket type package (Dual lead out)
  - — Lead pitch: 1.27 mm
- Single 5 V (±5%) supply
- High speed
  - — Access time: t_{RAC} = 60/70/80 ns (max)
  - — Access time: t_{CAC} = 20/23/25 ns (max)
- Low power dissipation
  - — Active mode: 5.38/4.96/4.54 W (max)
  - — Standby mode (TTL): 420 mW (max)
- Buffered input except $\overline{RAS}$ and DQ
- 4 byte interleave enabled, dual address input (A0/B0)
- Fast page mode capability
- 2,048 refresh cycle: 32 ms
- 2 variations of refresh
  - — $\overline{RAS}$-only refresh
  - — $\overline{CAS}$-before-$\overline{RAS}$ refresh

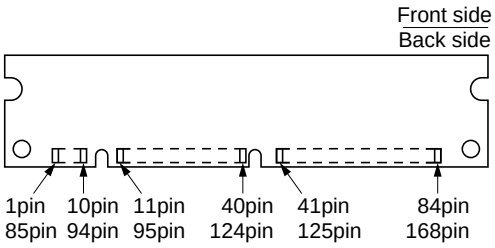
Note: The specifications of this device are subject to change without notice. Please contact your nearest Hitachi's Sales Dept. regarding specifications.

- TTL compatible

Ordering Infromation

Type No.	Access time	Package	Contact pad
HB56A264EJ-6B	60 ns	168-pin dual lead out socket type	gold
HB56A264EJ-7B	70 ns		
HB56A264EJ-8B	80 ns		

Pin Arrangement



Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	V_{SS}	16	DQ12	31	$\overline{OE0}$	46	$\overline{CE4}$
2	DQ0	17	DQ13	32	V_{SS}	47	$\overline{CE6}$
3	DQ1	18	V_{CC}	33	A0	48	$\overline{WE2}$
4	DQ2	19	DQ14	34	A2	49	V_{CC}
5	DQ3	20	DQ15	35	A4	50	NC
6	V_{CC}	21	DQ16	36	A6	51	NC
7	DQ4	22	NC	37	A8	52	DQ18
8	DQ5	23	V_{SS}	38	A10	53	DQ19
9	DQ6	24	NC	39	NC	54	V_{SS}
10	DQ7	25	NC	40	V_{CC}	55	DQ20
11	NC	26	V_{CC}	41	NC	56	DQ21
12	V_{SS}	27	$\overline{WE0}$	42	NC	57	DQ22
13	DQ9	28	$\overline{CE0}$	43	V_{SS}	58	DQ23
14	DQ10	29	$\overline{CE2}$	44	$\overline{OE2}$	59	V_{CC}
15	DQ11	30	$\overline{RE0}$	45	$\overline{RE2}$	60	DQ24

Pin Arrangement (cont)

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
61	NC	88	DQ38	115	NC	142	DQ59
62	NC	89	DQ39	116	V_{SS}	143	V_{CC}
63	NC	90	V_{CC}	117	A1	144	DQ60
64	NC	91	DQ40	118	A3	145	NC
65	DQ25	92	DQ41	119	A5	146	NC
66	NC	93	DQ42	120	A7	147	NC
67	DQ27	94	DQ43	121	A9	148	NC
68	V_{SS}	95	NC	122	NC	149	DQ61
69	DQ28	96	V_{SS}	123	NC	150	NC
70	DQ29	97	DQ45	124	V_{CC}	151	DQ63
71	DQ30	98	DQ46	125	NC	152	V_{SS}
72	DQ31	99	DQ47	126	B0	153	DQ64
73	V_{CC}	100	DQ48	178	V_{SS}	154	DQ65
74	DQ32	101	DQ49	128	NC	155	DQ66
75	DQ33	102	V_{CC}	129	NC	156	DQ67
76	DQ34	103	DQ50	130	$\overline{CE5}$	157	V_{CC}
77	NC	104	DQ51	131	$\overline{CE7}$	158	DQ68
78	V_{SS}	105	DQ52	132	$\overline{PDE}$	159	DQ69
79	PD1	106	NC	133	V_{CC}	160	DQ70
80	PD3	107	V_{SS}	134	NC	161	NC
81	PD5	108	NC	135	NC	162	V_{SS}
82	PD7	109	NC	136	DQ54	163	PD2
83	ID0 (V_{SS})	110	V_{CC}	137	DQ55	164	PD4
84	V_{CC}	111	NC	138	V_{SS}	165	PD6
85	V_{SS}	112	$\overline{CE1}$	139	DQ56	166	PD8
86	DQ36	113	$\overline{CE3}$	140	DQ57	167	ID1 (V_{SS})
87	DQ37	114	NC	141	DQ58	168	V_{CC}

Pin Description

Pin Name	Function
A0 to A10, B0	Address Input : A0 to A10, B0 Row Address : A0 to A10, B0 Column Address : A0 to A9, B0 Refresh Address : A0 to A10, B0
DQ0 to DQ7, DQ9 to DQ16 DQ18 to DQ25, DQ27 to DQ34 DQ36 to DQ43, DQ45 to DQ52 DQ54 to DQ61, DQ63 to DQ70	Data-in/Data-out
$\overline{RE0}$, $\overline{RE2}$	Row Address Strobe ($\overline{RAS}$)
$\overline{CE0}$ to $\overline{CE7}$	Column Address Strobe ($\overline{CAS}$)
$\overline{WE0}$, $\overline{WE2}$	Read/Write Enable
$\overline{OE0}$, $\overline{OE2}$	Output Enable
V_{CC}	Power Supply
V_{SS}	Ground
PD1 to PD8	Presence Detect
ID0, ID1	ID bit
$\overline{PDE}$	Presence Detect Enable
NC	No Connection

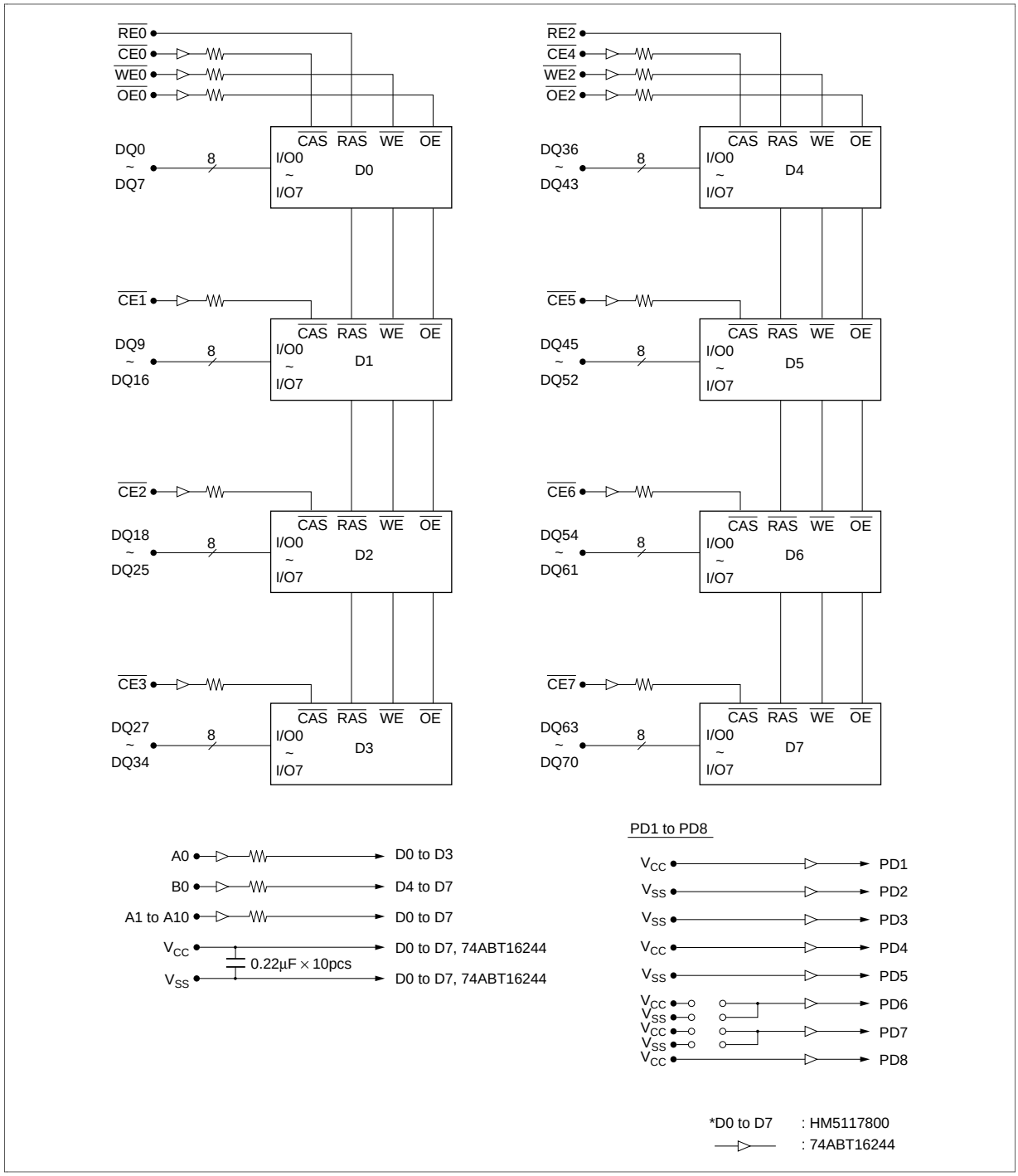
Presence Detect Pin Assignment

		$\overline{PDE}$ = Low			$\overline{PDE}$ = High
Pin Name	**Pin No.**	**60 ns**	**70 ns**	**80 ns**	**All**
PD1	79	1	1	1	High-Z
PD2	163	0	0	0	High-Z
PD3	80	0	0	0	High-Z
PD4	164	1	1	1	High-Z
PD5	81	0	0	0	High-Z
PD6	165	1	0	1	High-Z
PD7	82	1	1	0	High-Z
PD8	166	1	1	1	High-Z

1: High-Level (Driver Output)

0: Low Level (Driver Output)

Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_T	–0.5 to +7.0	V
Supply voltage relative to V_{SS}	V_{CC}	–0.5 to +7.0	V
Short circuit output current	Iout	50	mA
Power dissipation	Pt	9	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	–55 to +125	°C

Recommended DC Operating Conditions (Ta = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{SS}	0	0	0	V	
	V_{CC}	4.75	5.0	5.25	V	1
Input high voltage	V_{IH}	2.4	—	5.5	V	1
Input low voltage	V_{IL}	–0.5	—	0.8	V	1

Note: 1. All voltage referred to V_{SS}.

DC Characteristics (Ta = 0 to 70°C, V_{CC} = 5 V ± 5%, V_{SS} = 0 V)

		HB56A264EJ								
		60 ns		70 ns		80 ns				
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test Conditions	Notes
Operating current	I_{CC1}	—	1024	—	944	—	864	mA	t_{RC} = min	1, 2
Standby current	I_{CC2}	—	80	—	80	—	80	mA	TTL interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH} Dout = High-Z	
		—	72	—	72	—	72	mA	CMOS interface $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} – 0.2 V Dout = High-Z	
$\overline{RAS}$-only refresh current	I_{CC3}	—	1024	—	944	—	864	mA	t_{RC} = min	2
Standby current	I_{CC5}	—	104	—	104	—	104	mA	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL} Dout = enable	1
$\overline{CAS}$-before-$\overline{RAS}$ refresh current	I_{CC6}	—	1024	—	944	—	864	mA	t_{RC} = min	
Fast page mode current	I_{CC7}	—	784	—	704	—	664	mA	t_{PC} = min	1, 3
Input leakage current	I_{LI}	–10	10	–10	10	–10	10	µA	0 V ≤ Vin ≤ 5.5 V	
Output leakage current	I_{LO}	–10	10	–10	10	–10	10	µA	0 V ≤ Vout ≤ 5.5 V Dout = disable	
Output high voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	High Iout = –5 mA	
Output low voltage	V_{OL}	0	0.4	0	0.4	0	0.4	V	Low Iout = 4.2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected, I_{CC} max is specified at the output open condition.
2. Address can be changed once or less while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.

Capacitance (Ta = 25°C, V_{CC} = 5 V ± 5%)

Parameter	Symbol	Typ	Max	Unit	Notes
Input capacitance (Address)	C_{I1}	—	20	pF	1
Input capacitance ($\overline{CAS}$, $\overline{WE}$, $\overline{OE}$)	C_{I2}	—	20	pF	1
Input capacitance ($\overline{RAS}$)	C_{I3}	—	48	pF	1
I/O capacitance (DQ)	$C_{I/O}$	—	20	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CE}$ = V_{IH} to disable Dout.

AC characteristics

Refer to the HB56A272E Series data sheet.

Physical Outline

Unit: mm/inch