HB56SW832DZJ Series

32 MB EDO DRAM S.O.DIMM
8-Mword × 32-bit, 2 k Refresh, 2-Bank Module
(16 pcs of 4 M × 4 Components)

HITACHI

ADE-203-790B (Z)
Rev.2.0
Nov. 1997

Description

The HB56SW832DZJ is a 8M × 32 dynamic RAM Small Outline Dual In-line Memory Module (S.O.DIMM), mounted 16 pieces of 16-Mbit DRAM (HM51W17405) sealed in TCP package. An outline of the HB56SW832DZJ is 72-pin Zig Zag Dual tabs socket type compact and thin package. Therefore, the HB56SW832DZJ makes high density mounting possible without surface mount technology. The HB56SW832DZJ provides common data inputs and outputs. Decoupling capacitors are mounted on the module board.

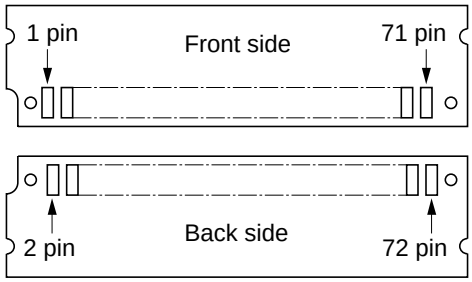
Features

- 72-pin Zig Zag Dual tabs socket type
  - Outline: 59.69 mm (Length) × 25.40 mm (Height) × 3.80 mm (Thickness)
  - Lead pitch: 1.27 mm
- Single 3.3 V (+0.3 V, –0.15 V) supply
- High speed
  - Access time: t_{RAC} = 60/70 ns (max)
    t_{CAC} = 15/18 ns (max)
- Low power dissipation
  - Active mode: 2.74/2.45 W (max)
  - Standby mode (TTL): 115.2 mW (max)
    (CMOS): 8.64 mW (max) (L/LS-version)
- EDO mode capability
- Refresh period
  - 2048 refresh cycles: 32 ms
    128 ms (L/LS-version)
- 3 variations of refresh
  - $\overline{\text{RAS}}$-only refresh
  - $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh
  - Self refresh (LS-version)

Ordering Information

Type No.	Access time	Package	Contact pad
HB56SW832DZJ-6	60 ns	72-pin small outline DIMM	Gold
HB56SW832DZJ-7	70 ns		
HB56SW832DZJ-6L	60 ns		
HB56SW832DZJ-7L	70 ns		
HB56SW832DZJ-6LS	60 ns		
HB56SW832DZJ-7LS	70 ns		

Pin Arrangement



Pin Arrangement

Front side				Back side			
Pin No.	**Pin name**	**Pin No.**	**Pin name**	**Pin No.**	**Pin name**	**Pin No.**	**Pin name**
1	V_{SS}	37	DQ18	2	DQ0	38	DQ19
3	DQ1	39	V_{SS}	4	DQ2	40	$\overline{CE0}$
5	DQ3	41	$\overline{CE2}$	6	DQ4	42	$\overline{CE3}$
7	DQ5	43	$\overline{CE1}$	8	DQ6	44	$\overline{RE0}$
9	DQ7	45	$\overline{RE1}$	10	V_{CC}	46	NC
11	PD1	47	$\overline{WE}$	12	A0	48	NC
13	A1	49	DQ20	14	A2	50	DQ21
15	A3	51	DQ22	16	A4	52	DQ23
17	A5	53	DQ24	18	A6	54	DQ25
19	A10	55	NC	20	NC	56	DQ27
21	DQ9	57	DQ28	22	DQ10	58	DQ29
23	DQ11	59	DQ31	24	DQ12	60	DQ30
25	DQ13	61	V_{CC}	26	DQ14	62	DQ32
27	DQ15	63	DQ33	28	A7	64	DQ34
29	NC	65	NC	30	V_{CC}	66	PD2
31	A8	67	PD3	32	A9	68	PD4
33	$\overline{RE3}$	69	PD5	34	$\overline{RE2}$	70	PD6
35	DQ16	71	PD7	36	NC	72	V_{SS}

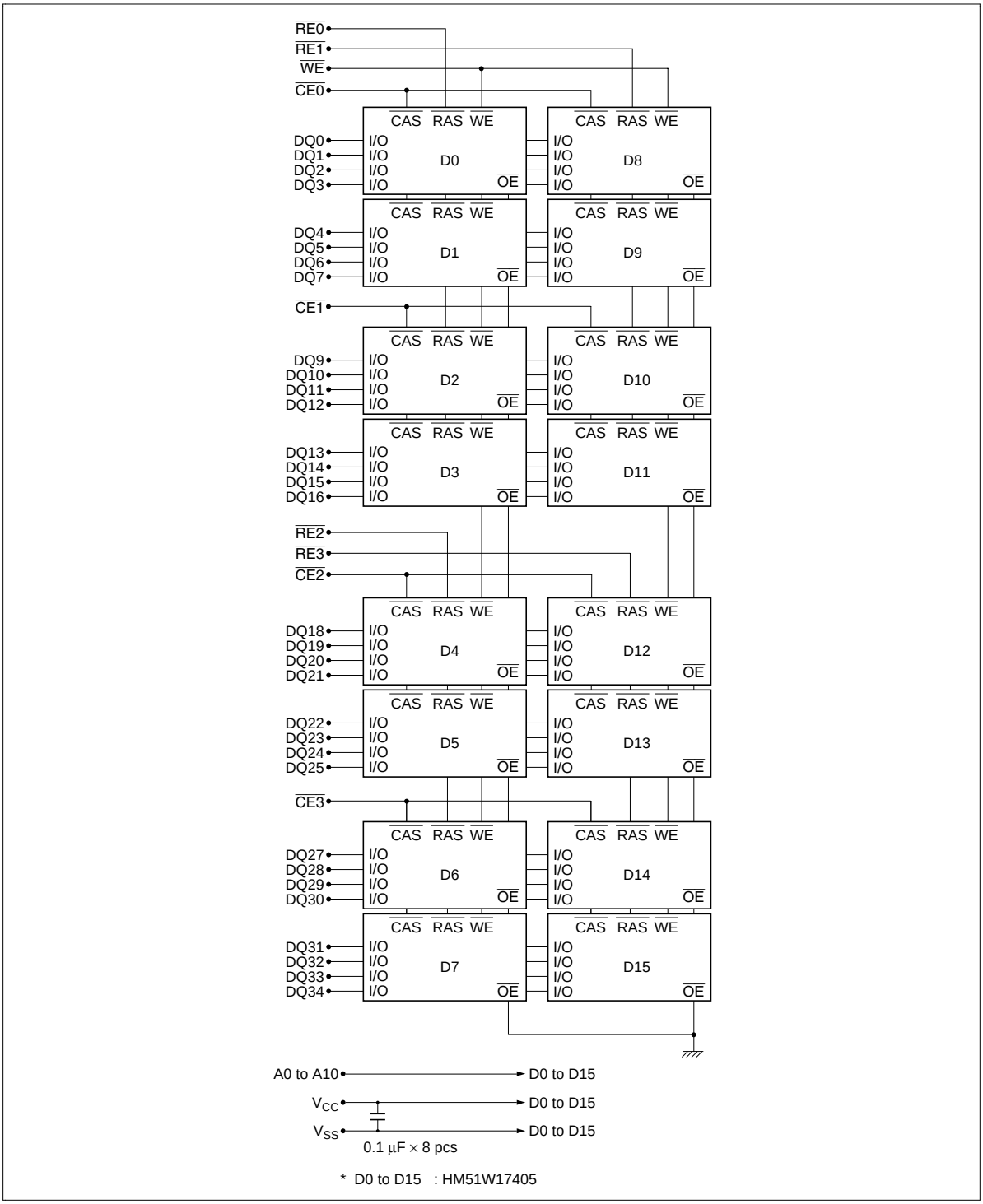
Pin Description

Pin name	Function
A0 to A10	Address inputs: Row address: A0 to A10 Column address: A0 to A10 Refresh address: A0 to A10
DQ0 to DQ7, DQ9 to DQ16, DQ18 to DQ25, DQ27 to DQ34	Data-in/Data-out
$\overline{RE0}$ to $\overline{RE3}$	Row address strobe ($\overline{RAS}$)
$\overline{CE0}$ to $\overline{CE3}$	column address strobe ($\overline{CAS}$)
$\overline{WE}$	Read/Write enable
V_{CC}	Power supply
V_{SS}	Ground
PD1 to PD7	Presence detect
NC	No connection

Presence Detect Pin Arrangement

		Function	
Pin No.	**Pin name**	**60 ns**	**70 ns**
11	PD1	NC	NC
66	PD2	NC	NC
67	PD3	V_{SS}	V_{SS}
68	PD4	V_{SS}	V_{SS}
69	PD5	NC	V_{SS}
70	PD6	NC	NC
71	PD7	NC	NC
	PD7 (LS-version)	V_{SS}	V_{SS}

Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_T	–0.5 to +4.6	V
Supply voltage relative to V_{SS}	V_{CC}	–0.5 to +4.6	V
Short circuit output current	Iout	50	mA
Power dissipation	Pt	8	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	–55 to +125	°C

Recommended DC Operating Conditions (Ta = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{SS}	0	0	0	V	
	V_{CC}	3.15	3.3	3.6	V	1
Input high voltage	V_{IH}	2.0	—	V_{CC} +0.3	V	1
Input low voltage	V_{IL}	–0.3	—	0.8	V	1

Note: 1. All voltage referred to V_{SS}.

DC Characteristics (Ta = 0 to 70°C, V_{CC} = 3.3 V +0.3 V, –0.15 V, V_{SS} = 0 V)

		60 ns		70 ns				
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test conditions**	**Notes**
Operating current	I_{CC1}	—	760	—	680	mA	t_{RC} = min	1, 2
Standby current	I_{CC2}	—	32	—	32	mA	TTL interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH} Dout = High-Z	
		—	16	—	16	mA	CMOS interface $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} – 0.2 V Dout = High-Z	
Standby current (L/LS-version)	I_{CC2}	—	2.4	—	2.4	mA	CMOS interface $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} – 0.2 V Dout = High-Z	
$\overline{RAS}$-only refresh current	I_{CC3}	—	760	—	640	mA	t_{RC} = min	2
Standby current	I_{CC5}	—	80	—	80	mA	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL} Dout = enable	1
$\overline{CAS}$-before-$\overline{RAS}$ refresh current	I_{CC6}	—	760	—	680	mA	t_{RC} = min	
EDO page mode current	I_{CC7}	—	680	—	640	mA	t_{HPC} = min	1, 3
Battery backup current (Standby with CBR refresh) (L/LS-version)	I_{CC10}	—	6.4	—	6.4	mA	CMOS interface Dout = High-Z CBR refresh: t_{RC} = 62.5 µs t_{RAS} ≤ 0.3 µs	
Self refresh mode current (LS-version)	I_{CC11}	—	4.0	—	4.0	mA	CMOS interface $\overline{RAS}$, $\overline{CAS}$ ≤ 0.2 V Dout = High-Z	
Input leakage current	I_{LI}	–10	10	–10	10	µA	0 V ≤ Vin ≤ 4.6 V	
Output leakage current	I_{LO}	–10	10	–10	10	µA	0 V ≤ Vout ≤ 4.6 V Dout = disable	
Output high voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	V	High Iout = –2 mA	
Output low voltage	V_{OL}	0	0.4	0	0.4	V	Low Iout = 2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected, I_{CC} max is specified at the output open condition.
2. Address can be changed once or less while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.

Capacitance (Ta = 25°C, V_{CC} = 3.3 V +0.3 V, –0.15 V)

Parameter	Symbol	Typ	Max	Unit	Notes
Input capacitance (Address)	C_{I1}	—	100	pF	1
Input capacitance ($\overline{WE}$)	C_{I2}	—	132	pF	1
Input capacitance ($\overline{CAS}$)	C_{I3}	—	48	pF	1
Input capacitance ($\overline{RAS}$)	C_{I4}	—	48	pF	1
I/O capacitance (DQ)	$C_{I/O}$	—	25	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable Dout.

AC Characteristics (Ta = 0 to 70°C, V_{CC} = 3.3 V +0.3 V, –0.15 V, V_{SS} = 0 V) *[1], *[2], *[18]

Test Conditions

- Input rise and fall times: 2 ns
- Input levels: 0 V, 3.0 V
- Input timing reference levels: 0.8 V, 2.0 V
- Output timing reference levels: 0.8 V, 2.0 V
- Output load: 1 TTL gate + C_L (100 pF) (Including scope and jig)

Read, Write, and Refresh Cycles (Common parameters)

		60 ns		70 ns			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Random read or write cycle time	t_{RC}	104	—	124	—	ns	
$\overline{RAS}$ precharge time	t_{RP}	40	—	50	—	ns	
$\overline{CAS}$ precharge time	t_{CP}	10	—	13	—	ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10000	70	10000	ns	
$\overline{CAS}$ pulse width	t_{CAS}	10	10000	13	10000	ns	
Row address setup time	t_{ASR}	0	—	0	—	ns	
Row address hold time	t_{RAH}	10	—	10	—	ns	
Column address setup time	t_{ASC}	0	—	0	—	ns	
Column address hold time	t_{CAH}	10	—	13	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	14	45	14	52	ns	3
$\overline{RAS}$ to column address delay time	t_{RAD}	12	30	12	35	ns	4
$\overline{RAS}$ hold time	t_{RSH}	13	—	13	—	ns	
$\overline{CAS}$ hold time	t_{CSH}	40	—	45	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5	—	5	—	ns	
$\overline{CAS}$ delay time from Din	t_{DZC}	0	—	0	—	ns	
Transition time (rise and fall)	t_T	2	50	2	50	ns	5
Refresh period (2,048 cycles)	t_{REF}	—	32	—	32	ms	
Refresh period (2,048 cycles) (L/LS-version)	t_{REF}	—	128	—	128	ms	

Read Cycle

		60 ns		70 ns			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Access time from $\overline{RAS}$	t_{RAC}	—	60	—	70	ns	6, 7
Access time from $\overline{CAS}$	t_{CAC}	—	15	—	18	ns	7, 8, 15
Access time from address	t_{AA}	—	30	—	35	ns	7, 9, 15
Read command setup time	t_{RCS}	0	—	0	—	ns	
Read command hold time to $\overline{CAS}$	t_{RCH}	0	—	0	—	ns	10
Read command hold time from $\overline{RAS}$	t_{RCHR}	60	—	70	—	ns	
Read command hold time to $\overline{RAS}$	t_{RRH}	5	—	5	—	ns	10
Column address to $\overline{RAS}$ lead time	t_{RAL}	30	—	35	—	ns	
Column address to $\overline{CAS}$ lead time	t_{CAL}	18	—	23	—	ns	
$\overline{CAS}$ to output in low-Z	t_{CLZ}	0	—	0	—	ns	
Output data hold time	t_{OH}	3	—	3	—	ns	19
Output buffer turn-off time	t_{OFF}	—	15	—	15	ns	11, 19
$\overline{CAS}$ to Din delay time	t_{CDD}	15	—	18	—	ns	
Output data hold time from $\overline{RAS}$	t_{OHR}	3	—	3	—	ns	19
Output buffer turn-off time to $\overline{RAS}$	t_{OFR}	—	15	—	15	ns	19
Output buffer turn-off to $\overline{WE}$	t_{WEZ}	—	15	—	15	ns	
$\overline{WE}$ to Din delay time	t_{WED}	15	—	18	—	ns	
$\overline{RAS}$ to Din delay time	t_{RDD}	15	—	18	—	ns	
$\overline{RAS}$ to next $\overline{CAS}$ delay time	t_{RNCD}	60	—	70	—	ns	

Write Cycle

		60 ns		70 ns			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Write command setup time	t_{WCS}	0	—	0	—	ns	12
Write command hold time	t_{WCH}	10	—	13	—	ns	
Write command pulse width	t_{WP}	10	—	10	—	ns	
Data-in setup time	t_{DS}	0	—	0	—	ns	13
Data-in hold time	t_{DH}	10	—	13	—	ns	13

Refresh Cycle

		60 ns		70 ns			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
$\overline{CAS}$ setup time (CBR refresh cycle)	t_{CSR}	5	—	5	—	ns	
$\overline{CAS}$ hold time (CBR refresh cycle)	t_{CHR}	10	—	10	—	ns	
$\overline{WE}$ setup time (CBR refresh cycle)	t_{WRP}	0	—	0	—	ns	
$\overline{WE}$ hold time (CBR refresh cycle)	t_{WRH}	10	—	10	—	ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	5	—	5	—	ns	

EDO Page Mode Cycle

		60 ns		70 ns			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
EDO page mode cycle time	t_{HPC}	25	—	30	—	ns	16
EDO page mode $\overline{RAS}$ pulse width	t_{RASP}	—	100000	—	100000	ns	14
Access time from $\overline{CAS}$ precharge	t_{CPA}	—	35	—	40	ns	7, 15
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{CPRH}	35	—	40	—	ns	
Output data hold time from $\overline{CAS}$ low	t_{DOH}	3	—	3	—	ns	7, 15
Read command hold time from $\overline{CAS}$ precharge	t_{RCHC}	35	—	40	—	ns	

Self Refresh Mode (L/LS-version)

		60 ns		70 ns			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
$\overline{RAS}$ pulse width (Self refresh)	t_{RASS}	100	—	100	—	µs	
$\overline{RAS}$ precharge time (Self refresh)	t_{RPS}	110	—	130	—	ns	
$\overline{CAS}$ hold time (Self refresh)	t_{CHS}	–50	—	–50	—	ns	

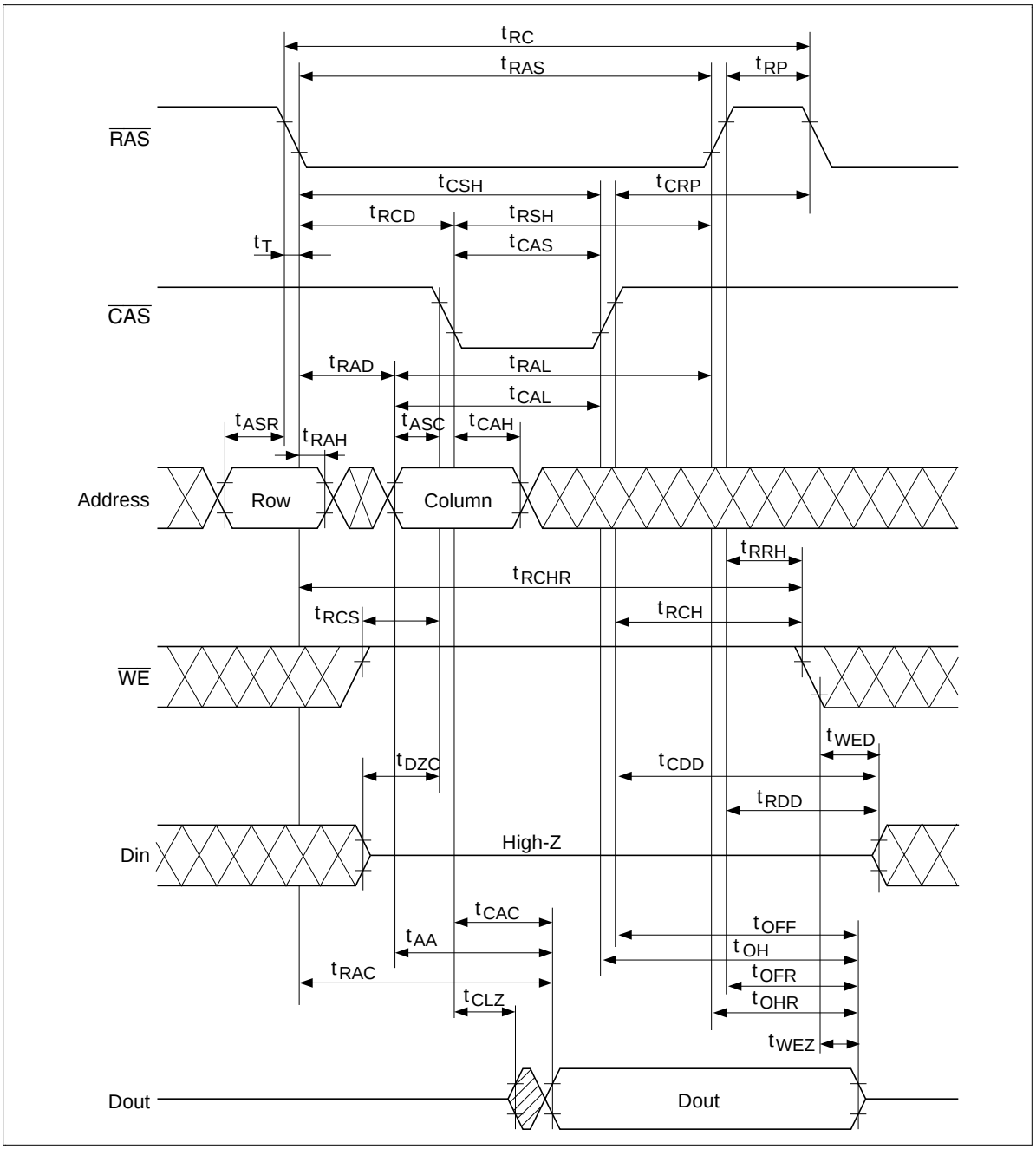
Notes:
1. AC measurements assume t_T = 2 ns.
2. An initial pause of 200 µs is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing $\overline{RAS}$-only refresh cycle or $\overline{CAS}$-before-$\overline{RAS}$ refresh). If the internal refresh counter is used, a minimum of eight $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles are required.
3. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only; if $t_{RCD} \geq t_{RCD}$ (max) + t_{AA} (max) - t_{CAC} (max), then access time is controlled exclusively by t_{CAC}.
4. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
5. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min) and V_{IL} (max).
6. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
7. Measured with a load circuit equivalent to 1 TTL loads and 100 pF.
8. Assumes that $t_{RCD} \geq t_{RCD}$ (max) and t_{RCD} + t_{CAC} (max) $\geq t_{RAD}$ + t_{AA} (max).
9. Assumes that $t_{RAD} \geq t_{RAD}$ (max) and t_{RCD} + t_{CAC} (max) $\leq t_{RAD}$ + t_{AA} (max).
10. Either t_{RCH} or t_{RRH} must be satisfied for a read cycles.
11. t_{OFF} (max) defines the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.
12. Early write cycle only ($t_{WCS} \geq t_{WCS}$ (min)).
13. These parameters are referred to $\overline{CAS}$ leading edge in early write cycles.
14. t_{RASP} defines $\overline{RAS}$ pulse width in EDO page mode cycles.
15. Access time is determined by the longest among t_{AA}, t_{CAC} and t_{CPA}.
16. t_{HPC} (min) can be achieved during a series of EDO page mode write cycles or EDO page mode read cycles.
17. When output buffers are enabled once, sustain the low impedance state until valid data is obtained. When output buffer is turned on and off within a very short time, generally it causes large V_{CC} / V_{SS} line noise, which causes to degrade V_{IH} min./ V_{IL} max level.
18. All the V_{CC} and V_{SS} pins shall be supplied with the same voltages.
19. Data output turns off and becomes high impedance from later rising edge of $\overline{RAS}$ and $\overline{CAS}$. Hold time and turn off time are specified by the timing specifications of later rising edge of $\overline{RAS}$ and $\overline{CAS}$ between t_{OHR} and t_{OH}, and between t_{OFR} and t_{OFF}.
20. Please do not use t_{RASS} timing, 10 µs $\leq t_{RASS} \leq$ 100 µs. During this period, the device is in transition state from normal operation mode to self refresh mode. If $t_{RASS} \geq$ 100 µs, then $\overline{RAS}$ precharge time should use t_{RPS} instead of t_{RP}.
21. If you use distributed CBR refresh mode with 15.6 µs interval in normal read/write cycle, CBR refresh should be executed within 15.6 µs immediately after exiting from and before entering into self refresh mode.
22. If you use $\overline{RAS}$ only refresh or CBR burst refresh mode in normal read/write cycle, 2048 cycles of distributed CBR refresh with 15.6 µs interval should be executed within 32 ms immediately after exiting from and before entering into the self refresh mode.
23. XXX: H or L (H: V_{IH} (min) $\leq V_{IN} \leq V_{IH}$ (max), L: V_{IL} (min) $\leq V_{IN} \leq V_{IL}$ (max))

    ///////: Invalid Dout

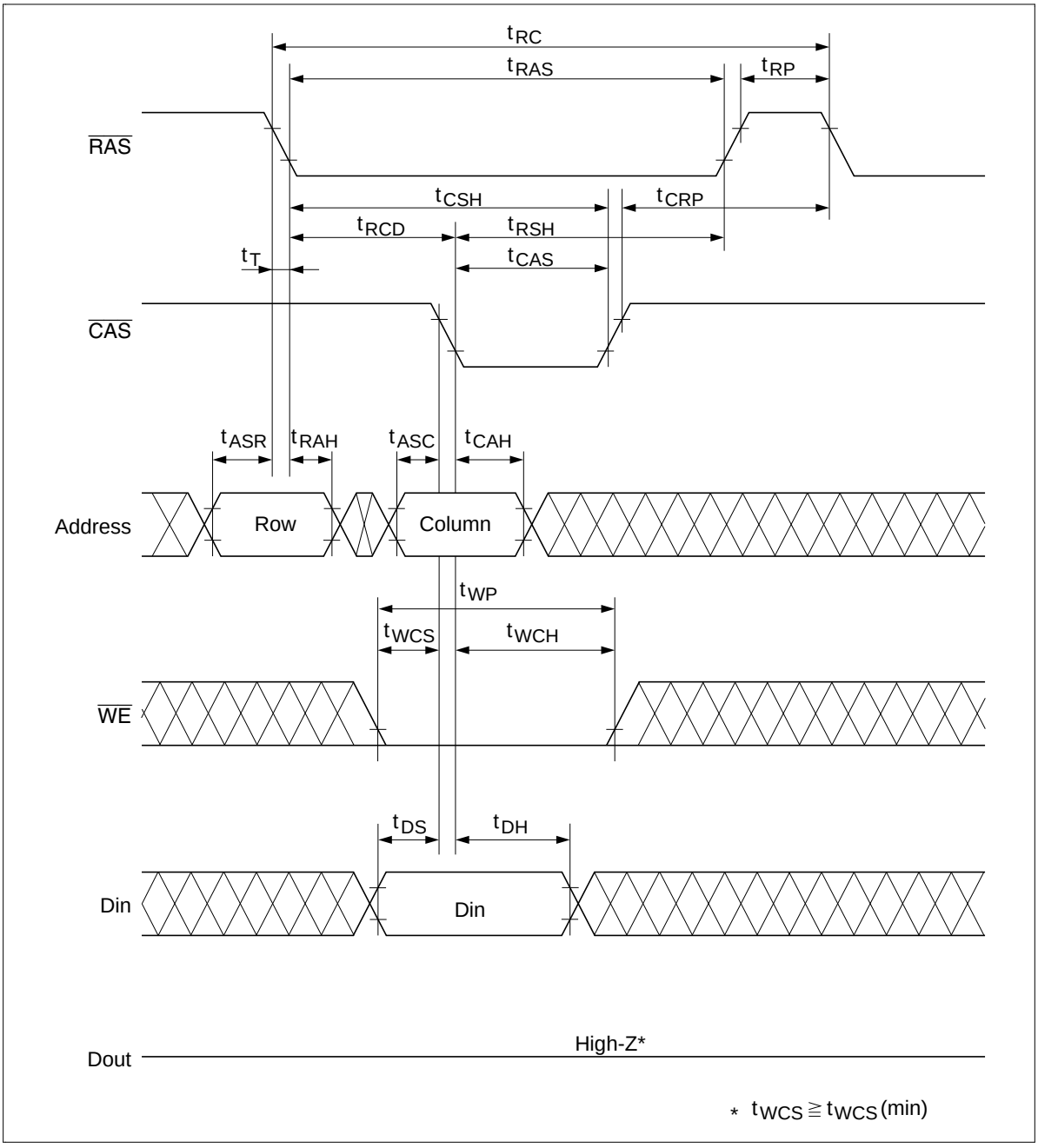
    When the address, clock and input pins are not described on timing waveforms, their pins must be applied V_{IH} or V_{IL}.

Timing Waveforms*[23]

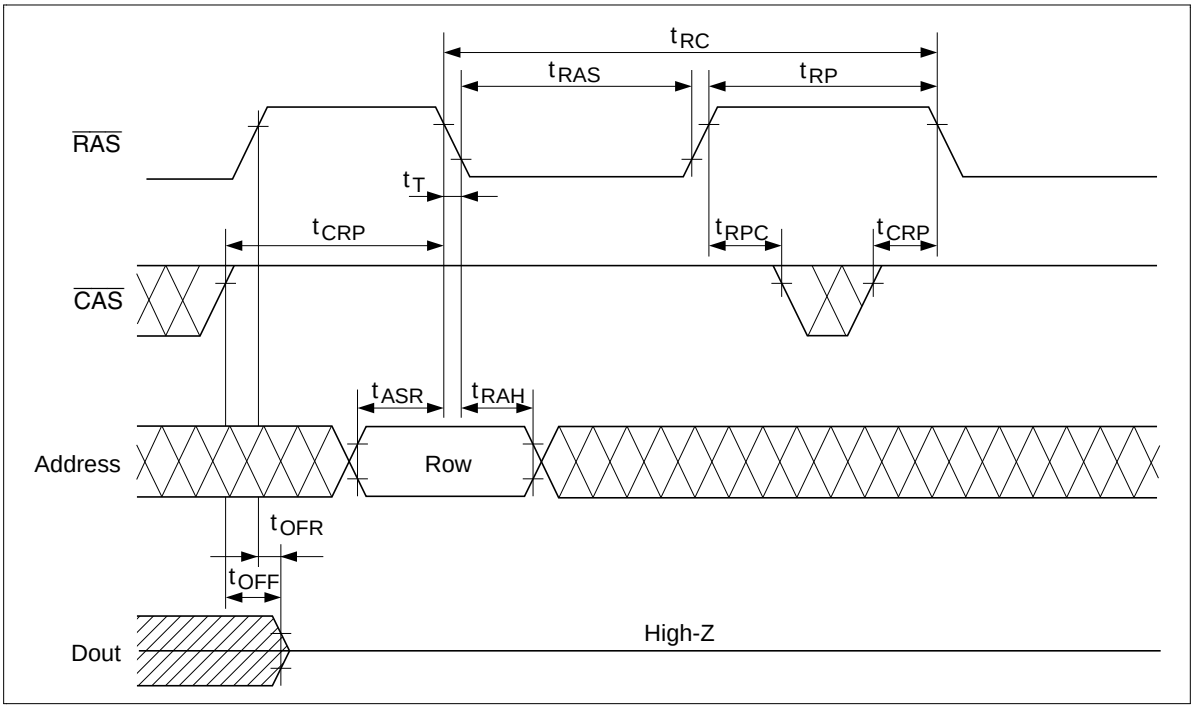
Read Cycle



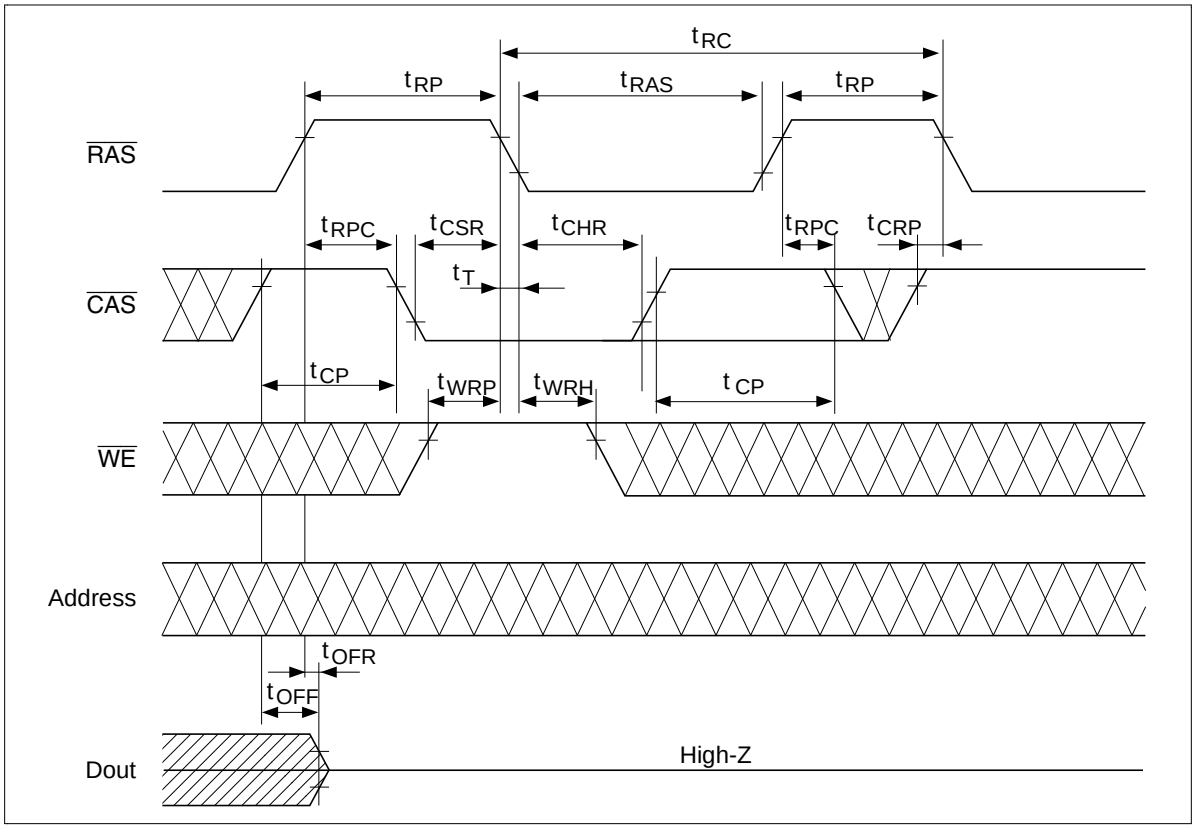
Early Write Cycle



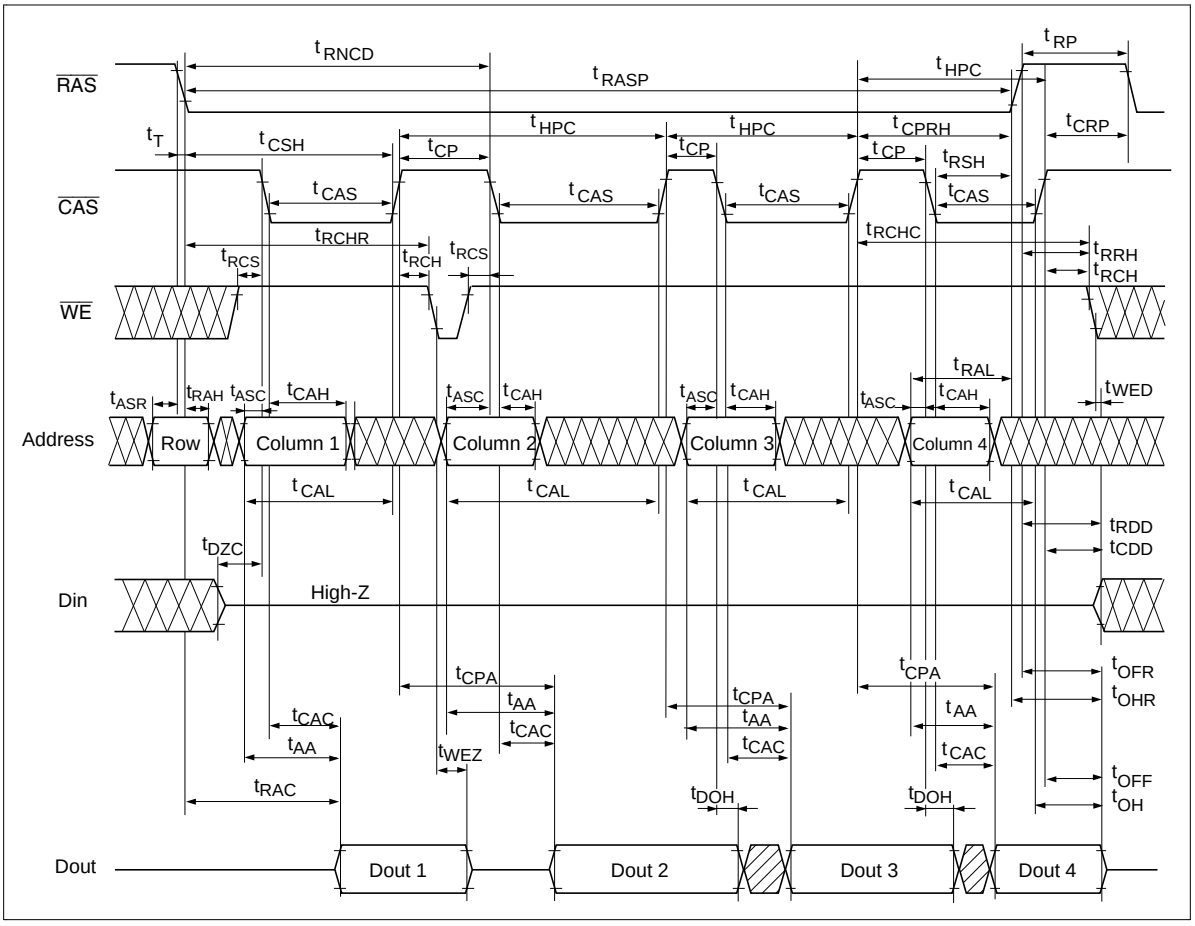
$\overline{\text{RAS}}$-Only Refresh Cycle



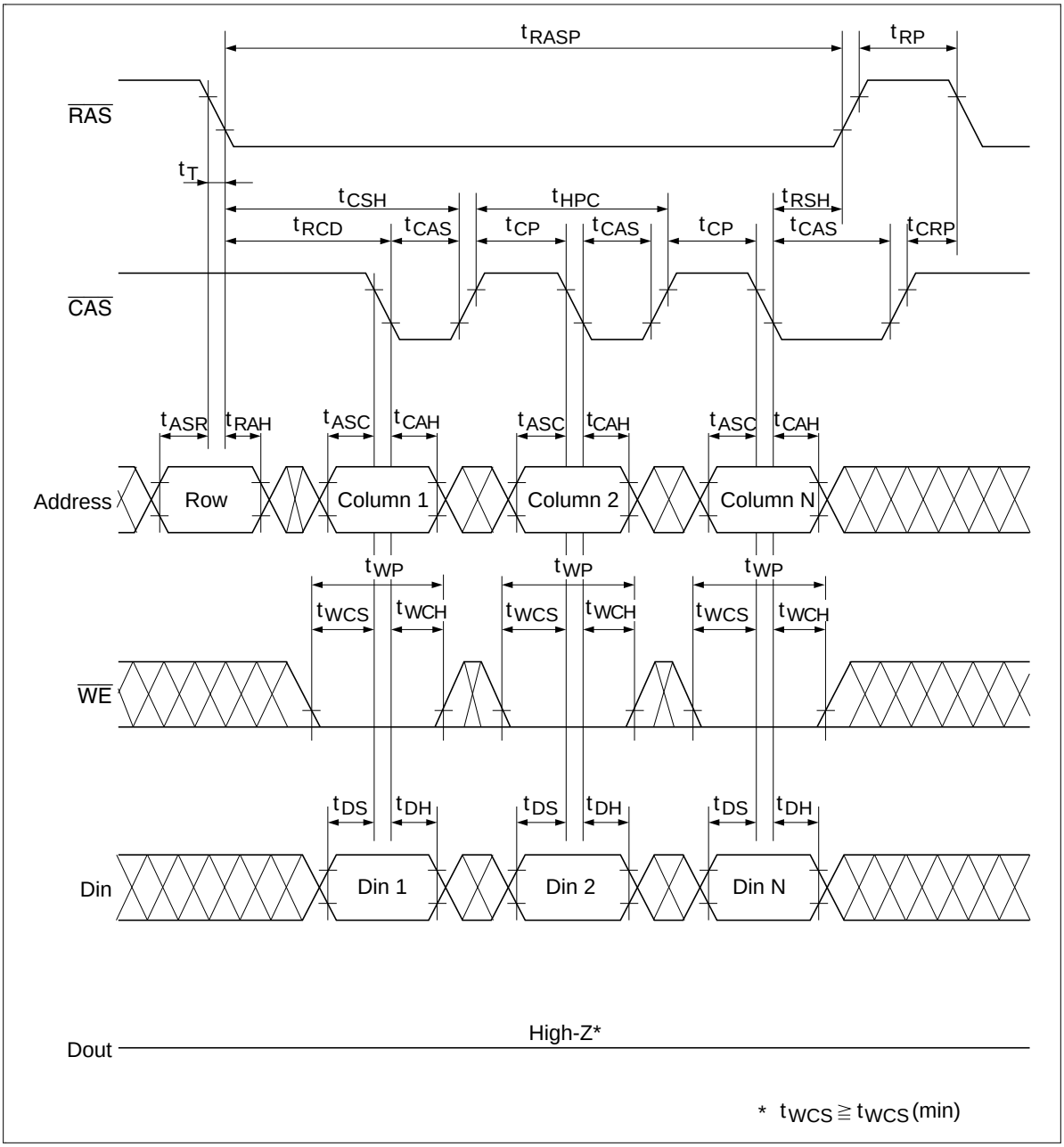
$\overline{\text{CAS}}$-Before-$\overline{\text{RAS}}$ Refresh Cycle



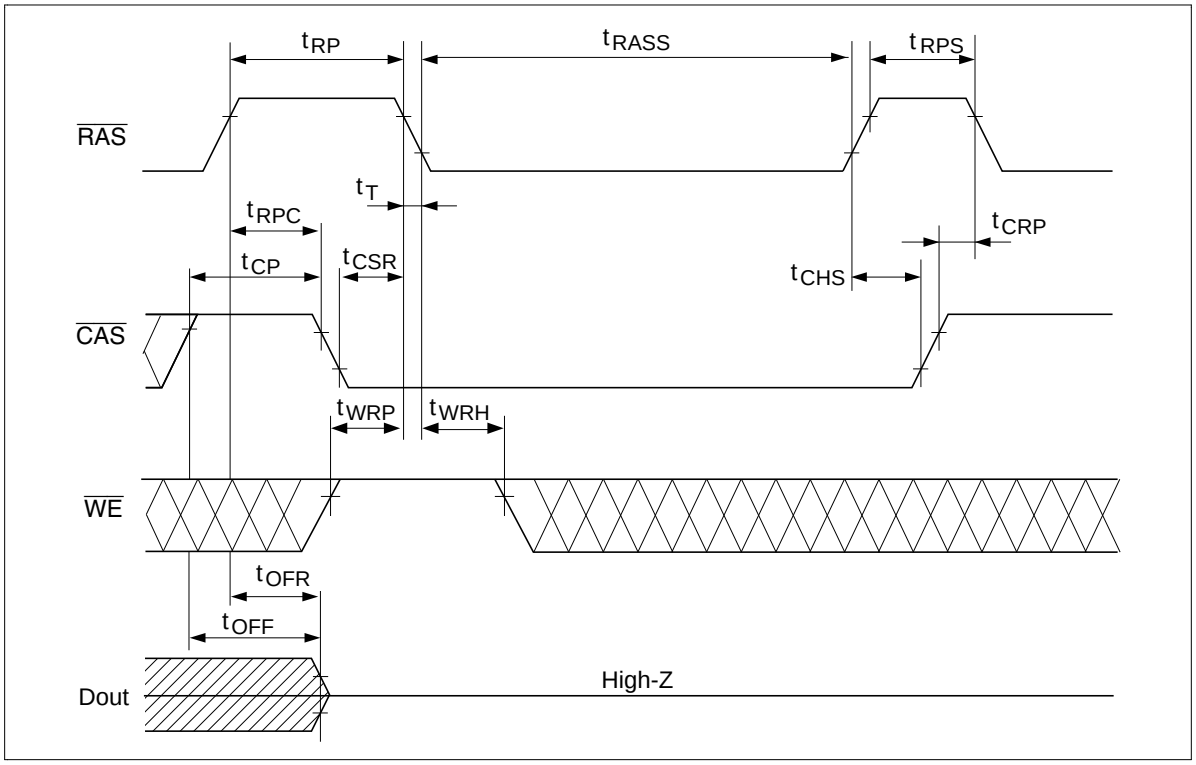
EDO Page Mode Read Cycle



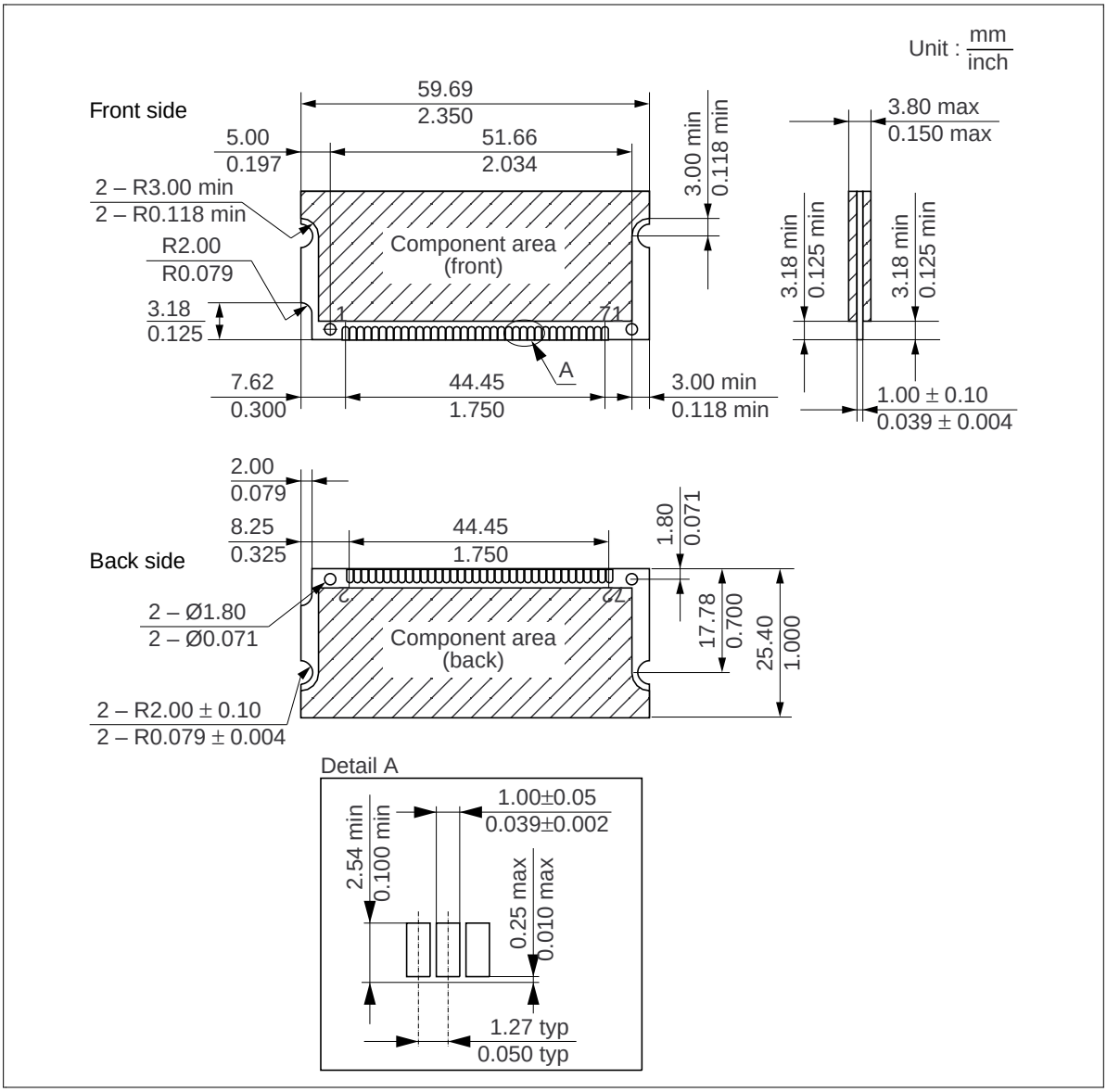
EDO Page Mode Early Write Cycle



Self Refresh Cycle (LS-version)*[20, 21, 22]



Physical Outline



When using this document, keep the following in mind:

1. This document may, wholly or partially, be subject to change without notice.
2. All rights are reserved: No one is permitted to reproduce or duplicate, in any form, the whole or part of this document without Hitachi's permission.
3. Hitachi will not be held responsible for any damage to the user that may result from accidents or any other reasons during operation of the user's unit according to this document.
4. Circuitry and other examples described herein are meant merely to indicate the characteristics and performance of Hitachi's semiconductor products. Hitachi assumes no responsibility for any intellectual property claims or other problems that may result from applications based on the examples described herein.
5. No license is granted by implication or otherwise under any patents or other rights of any third party or Hitachi, Ltd.
6. MEDICAL APPLICATIONS: Hitachi's products are not authorized for use in MEDICAL APPLICATIONS without the written consent of the appropriate officer of Hitachi's sales company. Such use includes, but is not limited to, use in life support systems. Buyers of Hitachi's products are requested to notify the relevant Hitachi sales offices when planning to use the products in MEDICAL APPLICATIONS.

HITACHI

Hitachi, Ltd.
Semiconductor & IC Div.
Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100, Japan
Tel: Tokyo (03) 3270-2111
Fax: (03) 3270-5109

For further information write to:

Hitachi Semiconductor
(America) Inc.
2000 Sierra Point Parkway
Brisbane, CA. 94005-1897
U S A
Tel: 800-285-1601
Fax:303-297-0447

Hitachi Europe GmbH
Continental Europe
Dornacher Straße 3
D-85622 Feldkirchen
München
Tel: 089-9 91 80-0
Fax: 089-9 29 30-00

Hitachi Europe Ltd.
Electronic Components Div.
Northern Europe Headquarters
Whitebrook Park
Lower Cookham Road
Maidenhead
Berkshire SL6 8YA
United Kingdom
Tel: 01628-585000
Fax: 01628-585160

Hitachi Asia Pte. Ltd.
16 Collyer Quay #20-00
Hitachi Tower
Singapore 049318
Tel: 535-2100
Fax: 535-1533

Hitachi Asia (Hong Kong) Ltd.
Unit 706, North Tower,
World Finance Centre,
Harbour City, Canton Road
Tsim Sha Tsui, Kowloon
Hong Kong
Tel: 27359218
Fax: 27306071

Revision Record

Rev.	Date	Contents of Modification	Drawn by	Approved by
1.0	Jun. 12, 1997	Initial issue (referred to HM51W16405/HM51W17405 rev. 3.0)	S. Tsukui	K. Yoshizaki
2.0	Nov. 1997	Change of Subtitle		