Preliminary Data Sheet

155.52 Mb/s Clock and Data Recovery Units

Features

- Recovers Clock and Data at STS-3 (155.52 Mb/s) Data Rate.
- No External Components Required.
- Available in One-channel (VSC8101) or Eight-channel (VSC8102) Versions.
- Recovers Data from NRZ or NRZI Data Streams.
- No Output Clock Drift in Absence of Data Transitions Once Lock is Acquired.
- ECL or Psuedo ECL (PECL) Differential Inputs and Outputs.
- Maximum Power Dissipation: VSC8101: 400mW, VSC8102: 3W.
- Single 2V Power Supply
- Available in 28PLCC (VSC8101) and 100PQFP (VSC8102)

Functional Description

The VSC8101 and VSC8102 are clock and data recovery units for STS-3 (155.52 Mb/s) applications. They implement the complete clock and data recovery functions and require no external components. The one-channel device, VSC8101, accepts serial data in NRZ or NRZI format and re-times the data using a sampling clock extracted from the input data stream. The recovered clock (RCLK+/-) and re-timed data (RDAT+/-) are presented at the serial output ports, aligned such that the falling edge of the recovered clock (RCLK+) coincides with the center of the data eye (see figure 4). The VSC8102 is an octal version of the VSC8101. A single reference clock input (REFCK+/-) at the STS-3 data rate (155.52MHz) is required for either device. The data and reference clock inputs, and the recovered data and clock outputs are differential ECL levels referenced to the V_{CC} supply. Only one supply, +2V or -2V, is required for operation.

Both the VSC8101 and VSC8102 employ a digital clock extraction technique, and do not contain a conventional PLL. As a result, the spectrum of the jitter in the recovered clock and data is non-Gaussian. Peak-to-peak jitter of RCLK+/- is ± 400 ps or less. The data input rate to the devices is required to be within ± 30 ppm from the reference clock frequency. The devices have data input jitter accommodation up to 3.2ns, half the data period. The VSC8101and VSC8102 also provide an input which control the loop bandwidth of the clock extraction function.

Tracking Frequency Bandwidth Control

The tracking of the recovered clock and data to the frequency variation of the input data stream can be adjusted in the VSC8101 and VSC8102. In particular, the FILTER0 input controls the degree to which the internal clock can track the input data frequency. The effect is equivalent to controlling the loop bandwidth of a conventional PLL-based clock recovery system. Equivalent bandwidths of 150 KHz and 10 KHz can be selected. The FILTER0 input truth data is shown in the AC Characteristic Table.

Jitter Tolerance

The VSC8101 and VSC8102 are designed to meet the BellcoreGR-253-CORE, section 5.6.2.2.2 Jitter Tolerance specification.

Figure 1: Jitter Tolerance Mask for STS-3

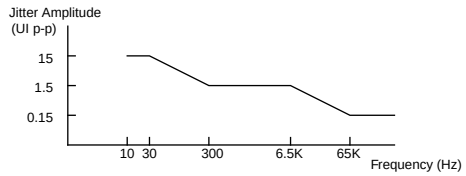


Figure 2: VSC8101 Block Diagram

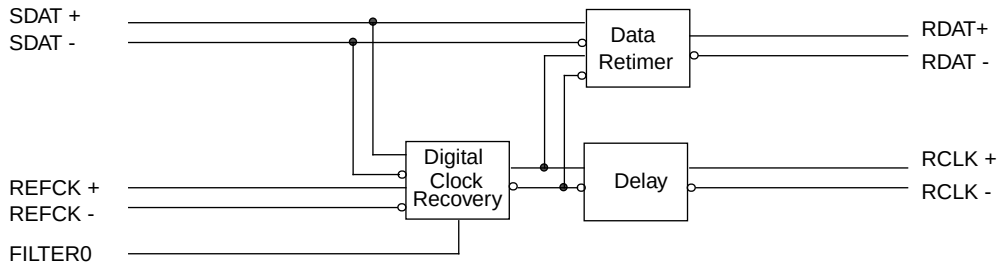
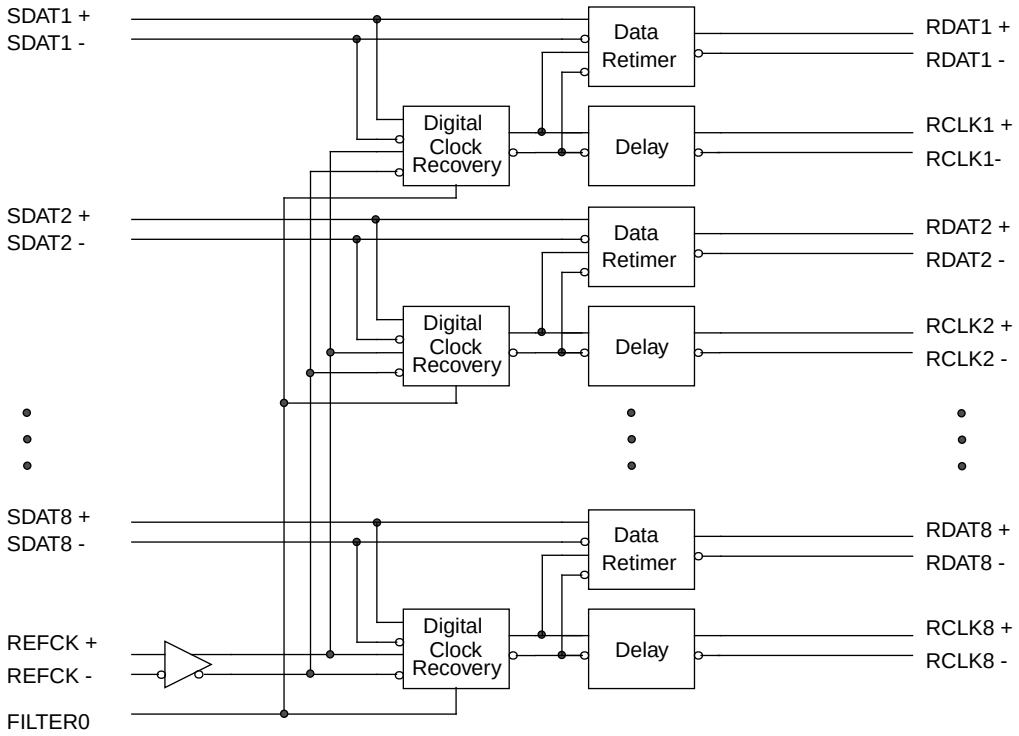


Figure 3: VSC8102 Block Diagram



VSC8101/8102 AC Characteristics *(Over recommended operating range*

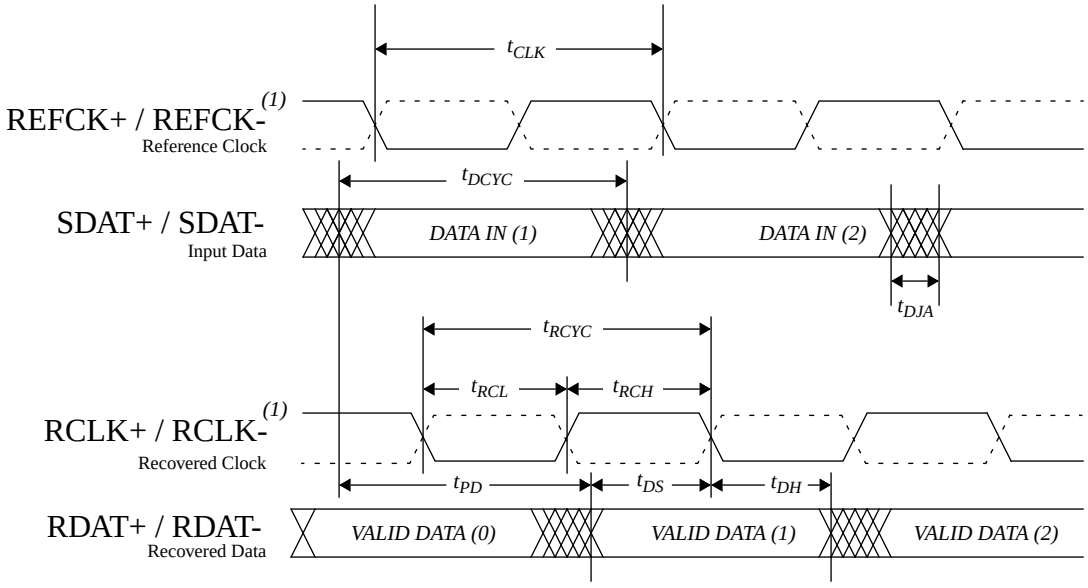
Parameter	Description	Min	Typ	Max	Units
t_{CLK}	REFCK+/- Input Clock period(1)	—	6.43	—	ns
t_{DCYC}	SDAT +/- Input data period	t_{CLK} - 30 ppm	—	t_{CLK} + 30 ppm	
Δf_{DC}	SDAT+/- Input Rate Difference with respect to REFCK+/-	-30	—	+30	ppm
t_{CDC}	REFCK+/- Duty Cycle	40	—	60	%
t_{DH}	Recovered Data hold time from falling edge of Recovered Clock(2)	2.5	—	3.9	ns
t_{DS}	Recovered Data setup time to falling edge of Recovered Clock(2)	2.5	—	3.9	ns
t_{RCH}	RCLK+/- Recovered Clock Output High Pulse Width	2.6	—	—	ns
t_{RCL}	RCLK+/- Recovered Clock Output Low Pulse Width	2.6	—	—	ns
t_{RCYC}	RCLK+/- Recovered Clock Period	6.0	—	6.8	ns
t_{DJA}	SDAT+/- Input Jitter Accommodation (DC to 20 MHz) Peak-to-peak	—	—	3.2	ns
t_{LA}	Lock Acquisition Time (3)	—	—	5.0	µ s
f_{BW}	Loop Bandwidth: a) at FILTER0 = Lo b) at FILTER0 = Hi	—	—	 150 10	KHz
t_{RCJ}	RCLK+/- Recovered Clock Jitter	-400		400	ps
t_{PD}	Propagation Delay from SDATA+/- Input to RDAT+/- Output	—	—	TBD	ps
t_{Cr}, t_{Cf}	REFCK+/- Input rise and fall time, 20% to 80%	—	—	1.2	ns
t_{SDr}, t_{SDf}	SDATA+/- Input rise and fall time, 20% to 80%	—	—	1.2	ns
t_{RCr}, t_{RCf}	RCLK+/- Recovered Clock Output rise and fall time, 20% to 80%	300	—	800	ps
t_{RDr}, t_{RDf}	RDAT+/- Recovered Data Output rise and fall time, 20% to 80%	300	—	800	ps

Notes: (1) The part is designed to operate at 155.52 MHz. A reference clock with frequency variation of +/- 50 ppm or better is recommended. Consult the factory for applications other than this frequency.

(2) With minimum 50% Input Data Eye opening at 155.52 Mb/s.

. (3) With a jitter-free data input and minimum transition density of 50%.

Figure 4: VSC8101/8102 AC Timing Waveform



Note: (1) Solid line indicates the true sense and dotted line indicates the complementary sense of the signal.

Absolute Maximum Ratings (1)

Power Supply Voltage (V_{CC} -V_{TT}).....-0.5V to +3.0V
Input Voltage (V_{IN}) ..... V_{CC} -2.5V to V_{CC} + 0.5V
Output Current, I_{OUT} (DC, Output HI) .....-50mA
Case Temperature Under Bias, T_C..... -55° to +125°C
Storage Temperature (T_{STG}).....-65°C to +135°C

Recommended Operating Conditions

The VSC8101 and VSC8102 can be powered by:
a) connecting V_{CC} to +2V and V_{TT} to GND, or
b) connecting V_{CC} to GND and V_{TT} to -2V.

Power Supply Voltage (V_{CC} -V_{TT})..... 2.0V ± 5%
Operating Temperature Range(2) ..... 0° to +70°C

Notes:
(1) CAUTION: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing pe manent damage. Functionality at or above the values listed is not implied. Exposure to these values for extended periods may affect device reliability.
(2) Lower limit is ambient temperature and upper limit is case temperature.

VSC8101/8102 DC Characteristics *(Over recommended operating conditions)*

Table 1: Inputs and Outputs

Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
V_{IH}	Input HIGH voltage	V_{CC} - 1150	—	V_{CC} - 600	mV	Guaranteed HIGH signal for all inputs
V_{IL}	Input LOW voltage	V_{TT}	—	V_{CC}- 1500	mV	Guaranteed LOW signal for all inputs
V_{OH}	Output HIGH voltage	V_{CC} - 1020	—	V_{CC} - 700	mV	$V_{IN} = V_{IH}$ (max) or V_{IL} (min). Outputs terminated identically into V_{TT} with 50 ohms.
V_{OL}	Output LOW voltage	V_{TT}	—	V_{CC} - 1620	mV	$V_{IN} = V_{IH}$ (max) or V_{IL} (min). Outputs terminated identically into V_{TT} with 50 ohms.
ΔV_I	Input voltage swing for REFCK+/- and SDAT+/-	450	—	—	mV	(1) For AC-Coupling: input swing at the pin. (2) For DC-Coupling: input swing referenced to the common mode voltage;
V_{OCM}	Output common mode voltage for RDAT+/- and RCLK+/-	.5 + V_{TT}	—	.8 + V_{TT}		Differential Outputs terminated identically into V_{TT} with 50 ohms.
ΔV_O	Output voltage swing for RDAT+/- and RCLK+/-	600	—	—	mV	Differential Outputs terminated identically into V_{TT} with 50 ohms.

Table 2: Power Dissipation

Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
P_D	Power dissipation (VSC8101)	—	—	400	mW	Outputs open, V_{CC} = 2.1V
P_D	Power dissipation (VSC8102)	—	—	3.0	W	same as above
I_{CC}	Supply current (VSC8101)	—	—	190	mA	same as above
I_{CC}	Supply current (VSC8102)	—	—	1430	mA	same as above

Generation of 2V Supply for the VSC8101/VSC8102

In a ECL system, -2V will be one of the standard supplies and the VSC8101/VSC8102 can be powered with GND and -2V. However, for typical TTL systems, 2V is generally not available. In these applications, the 2V supply can be generated easily from a 5V or 3.3V supply. There are several manufacturers who supply complete single-chip linear regulators. Examples are:

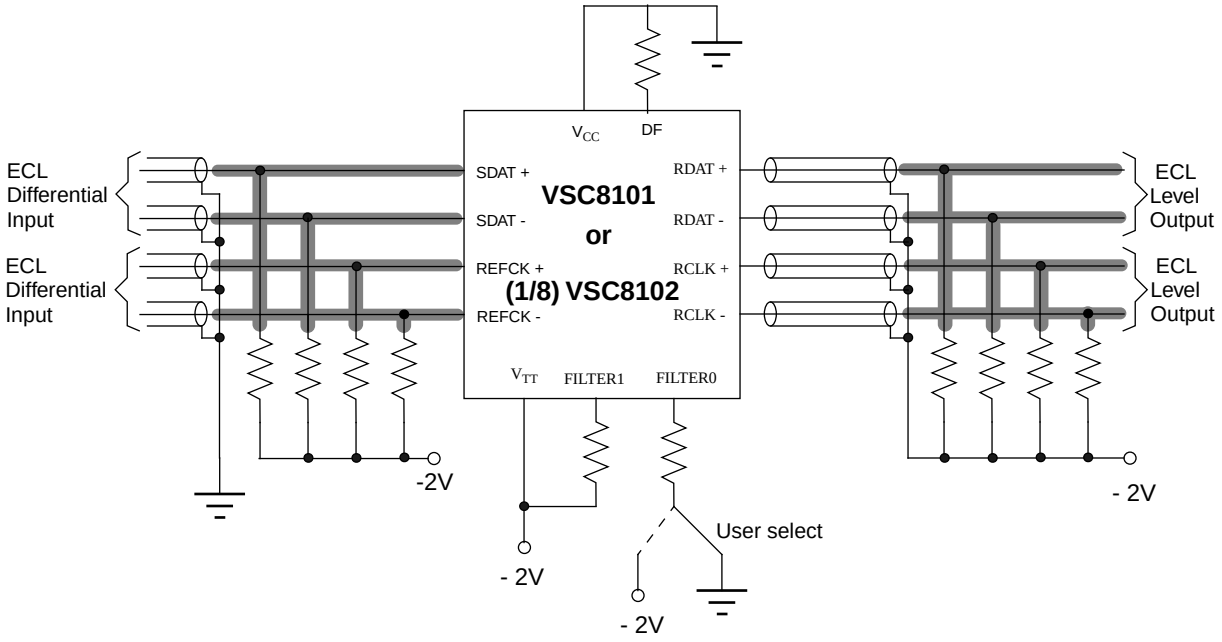
Table 3: Linear Regulators and Suppliers

Device	*Regulator Recommended*	*Maximum Supply Current*	*Manufacturer's Information*
VSC8101	REG1117	800mA	Burr Brown, 800-548-6132
VSC8102	LT1086	1.5A	Linear Tech, 408-432-1900

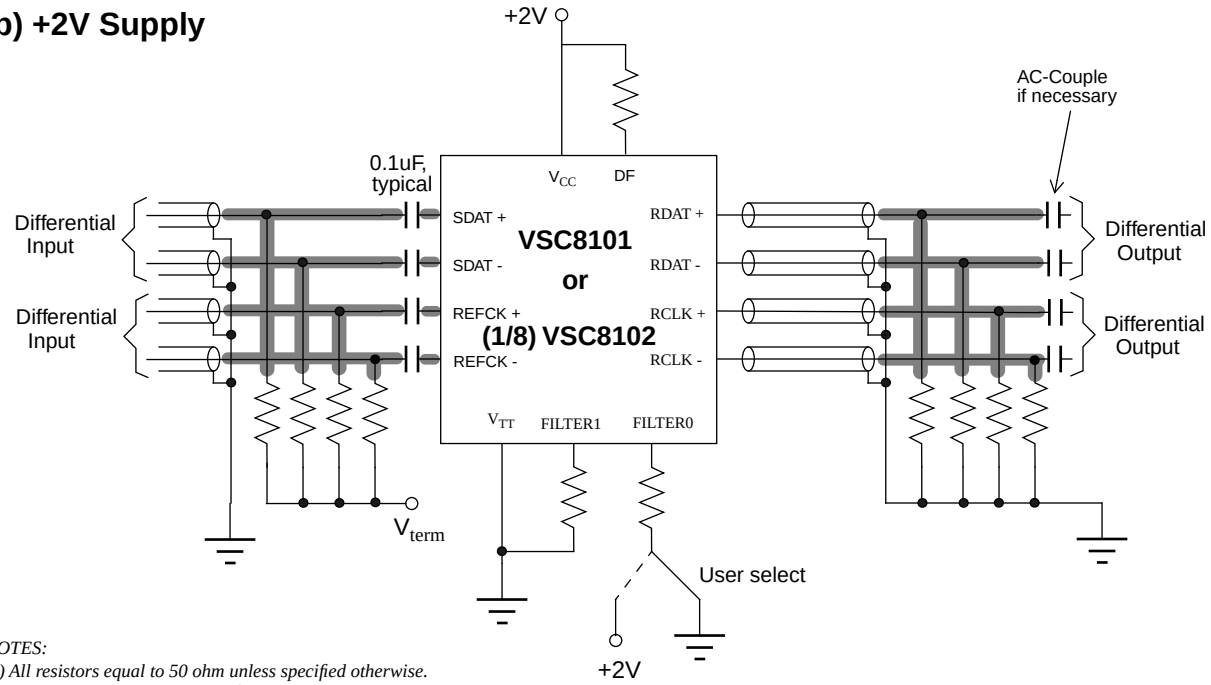
Note: (1) Complete data sheets for these regulators can be obtained from the manufacturers.

Figure 5: Typical Applications

(a) -2V Supply



(b) +2V Supply



NOTES:
(1) All resistors equal to 50 ohm unless specified otherwise.
(2) Shaded lines represent stubs of transmission lines. They should have the corresponding traces on board be as short as possible to minimize reflection.

Table 4: VSC8101 Pin Description

Signal Name	*Pin*	*Level*	*Description*
REFCK+	5	ECL	Reference Clock input true
REFCK-	6	ECL	Reference Clock input complement
SDAT+	9	ECL	Data input true
SDAT-	10	ECL	Data input complement
RCLK+	25	ECL	Recovered Clock true
RCLK-	23	ECL	Recovered Clock complement
RDAT+	21	ECL	Recovered Data true
RDAT-	19	ECL	Recovered Data complement
FILTER0	16	V_{CC}/V_{TT}	Selects the Loop Bandwidth: (1) FILTER0 = LO, Bandwidth = 150 KHz (2) FILTER0 = HI, Bandwidth = 10 KHz
FILTER1	17	V_{TT}	For normal operation, connect to V_{TT} thru 50 ohm resistor
DF	14	V_{CC}	For normal operation, connect to V_{CC} thru 50 ohm resistor
NC	1-3,7,11,13, 15,27,28		Do not connect, leave open
VCC	8,20,22,24		Positive supply, V_{CC}
VTT	4,12,18,26		Negative supply, V_{TT}

Figure 6: VSC8101 Pin Diagram

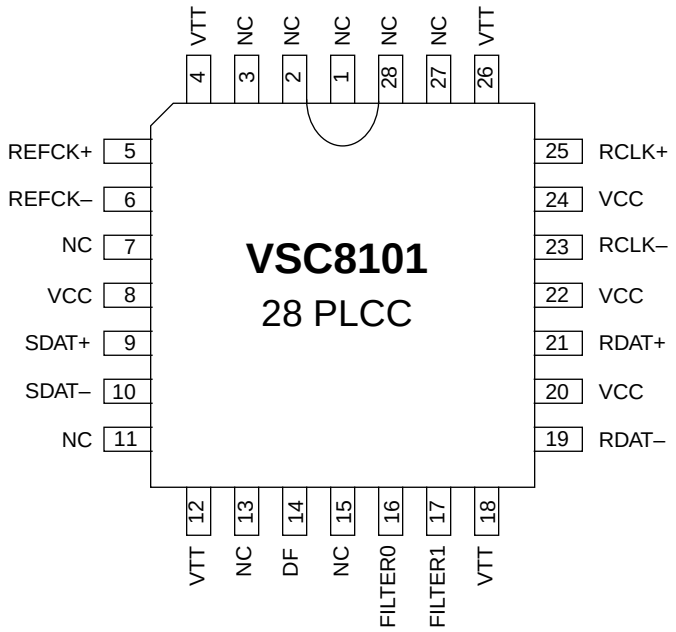
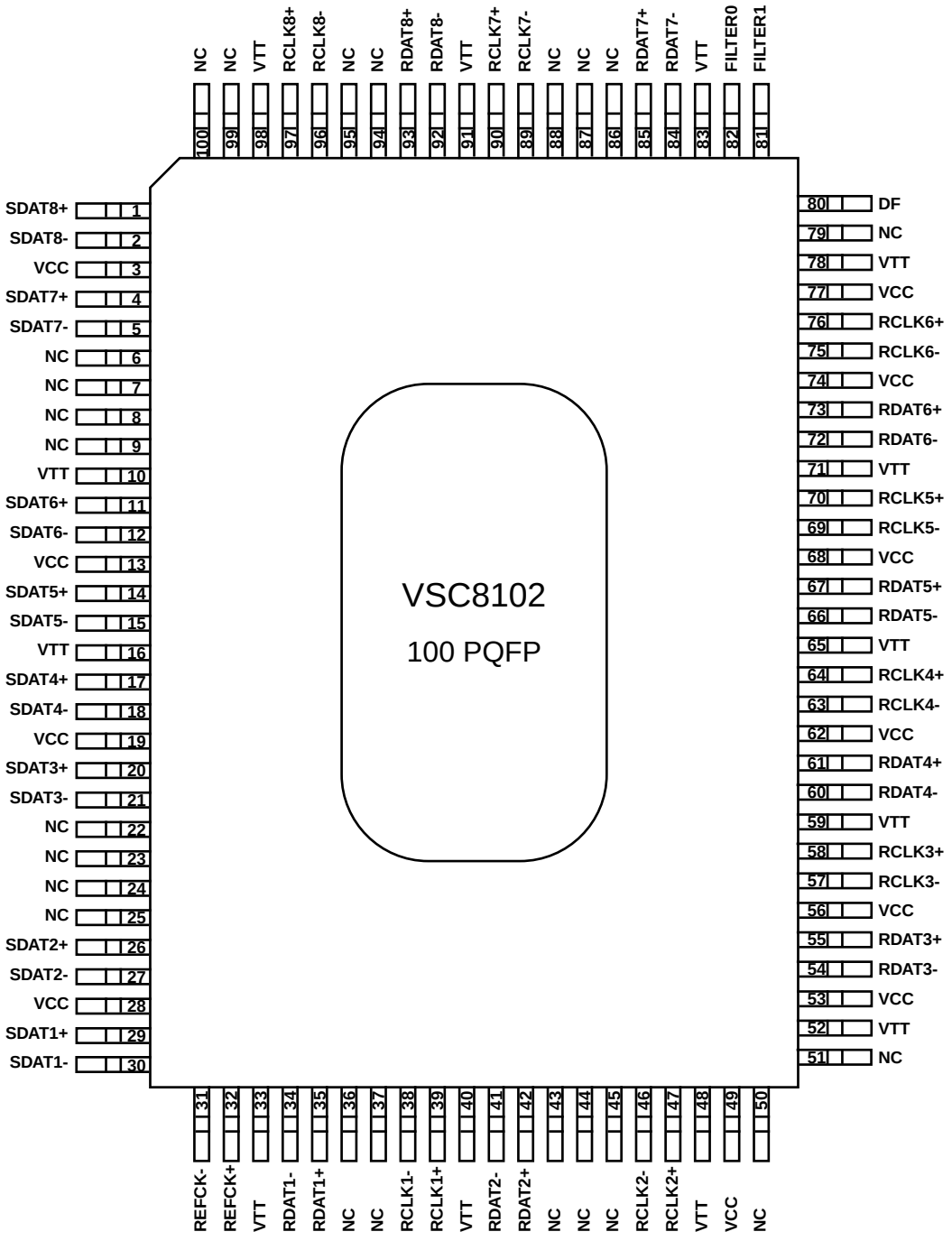


Table 5: VSC8102 Pin Description

Signal Name	*Pin*	*Level*	*Description*
REFCK+	32	ECL	Reference Clock Input True
REFCK-	31	ECL	Reference Clock input complement
SDAT+	29,26,20,17, 14,11,4,1	ECL	Data input true
SDAT-	30,27,21,18, 15,12,5,2	ECL	Data input complement
RCLK+	39,47,58,64, 70,76,90,97	ECL	Recovered Clock true
RCLK-	38,46,57,63, 69,75,89,96	ECL	Recovered Clock complement
RDAT+	35,42,55,61, 67,73,85,93	ECL	Recovered Data true
RDAT-	34,41,54,60, 66,72,84,92	ECL	Recovered Data complement
FILTER0	82	V_{CC}/V_{TT}	Selects the Loop Bandwidth: (1) FILTER0 = LO, Bandwidth = 150 KHz (2) FILTER0 = HI, Bandwidth = 10 KHz
FILTER1	81	V_{TT}	For normal operation, connect to V_{TT} thru 50 ohm resistor
DF	80	V_{CC}	For normal operation, connect to V_{CC} thru 50 ohm resistor
NC	6-9,22-25,36,37,43-45,50,51,79, 86-88,94,95, 99,100		Do not connect, leave open
VCC	3,13,19,28,49,53,56, 62,68, 74,77		Positive supply, V_{CC}
VTT	10,16,33,40, 48,52,59,65, 71,78,83,91, 98		Negative supply, V_{TT}

Figure 7: VSC8102 Pin Diagram

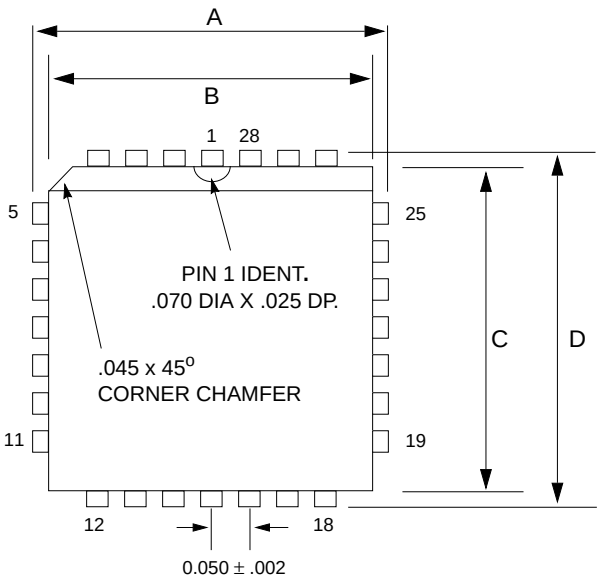


DRAWING IS HEAT SINK UP

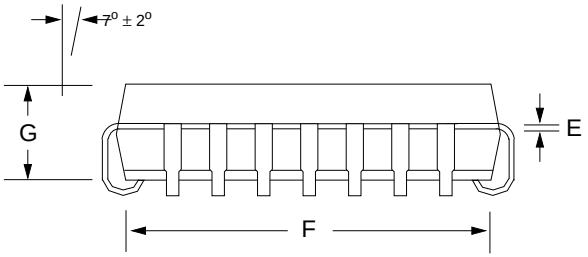
Package Information

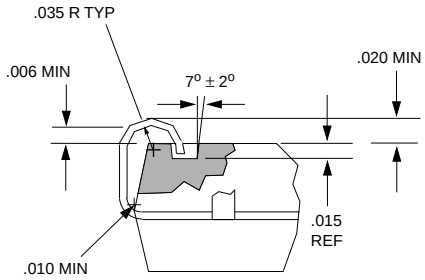
The VSC8101 is packaged in a 28-pin Plastic Leaded Chip Carrier (PLCC), 0.454 x 0.454 in.^{2} body size. The VSC8102 is packaged in a 100-pin Plastic Quad Flat Pack (PQFP), 20 x 14 mm^2 body size).

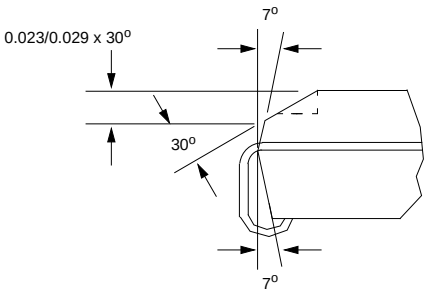
Figure 8: VSC8101 Package Drawings (28PLCC-JEDEC)



Item	inch	Tol.
A	.490	± .005
B	.454	± .002
C	.454	± .002
D	.490	± .005
E	.010	± .0003
F	.420	±.010
G	.152	± .002

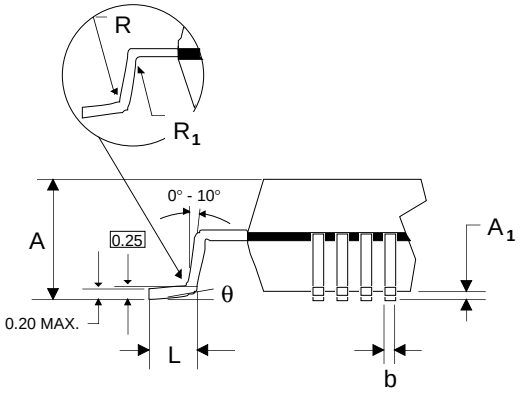




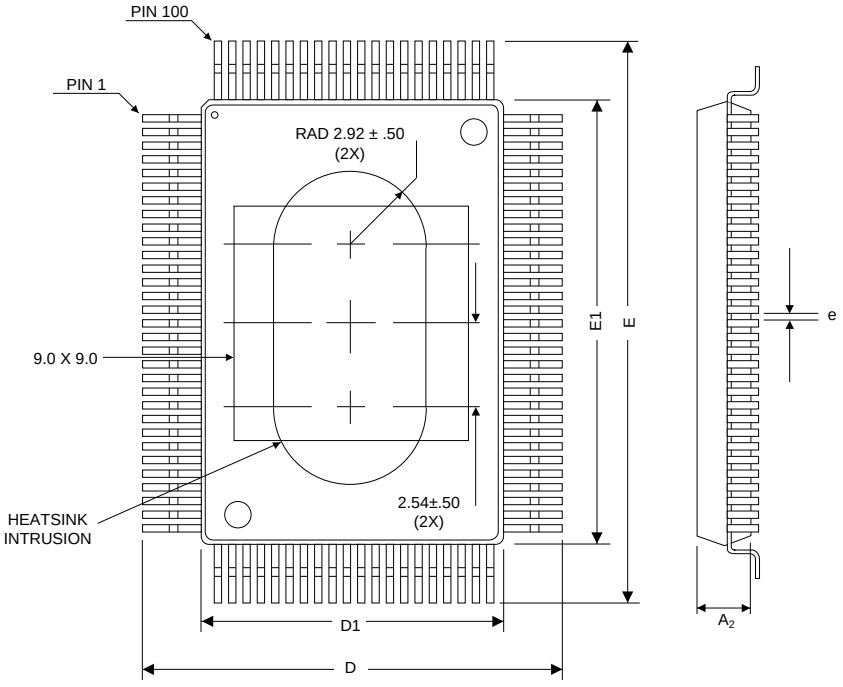


NOTES:
(1) Drawings not to scale.
(2) All units in inch unless otherwise noted.

Figure 9: VSC8102 Package Drawings (100PQFP)



Dims.	mm	Tolerance
A	3.40	MAX
A1	0.60	MAX
A2	2.7	±.10
D	17.20	±.40
D1	14.00	±.10
E	23.20	±.40
E1	20.00	±.10
L	0.80	±.2
e	0.65	NOM
b	0.30	±.10
θ	0-10°	
R	.25	NOM
R1	.2	NOM



NOTES:

(1) Drawings not to scale.

(2) Two styles of exposed heat spreaders may be used; square or oval.

(3) All units in millimeters

Thermal Characteristics of the VSC8101 and VSC8102 Packages

VSC8101

The VSC8101 is packaged in a 28PLCC, with an internal heat spreader for improved heat dissipation. With natural convection, the Case to Air Thermal Resistance (θ_{CA})is estimated to be 65^{o}C/W.

VSC8102

The VSC8102 is packaged in a thermally enhanced 100PQFP with an embedded heat spreader. The heat spreader surface area is shown in figure 9. With natural convection, the Case to Air Thermal Resistance (θ_{CA})is estimated to be 27.5^{o}C/W. The Air Flow versus Thermal Resistance relationship is shown in the following table:

Table 6: θ_{CA} Versus Air Velocity for the VSC8102 Package

Air Velocity (LFPM)	*Case to Air Thermal Resistance (^{o}C/W)*
0	27.5
100	23.1
200	19.8
400	17.6
600	16

Ordering Information

The order numbers for this product family are:

Part Number	Device Type
VSC8101JA:	1-Channel Clock and Data Recovery Unit in 28 Pin PLCC
VSC8102QB:	8-Channel Clock and Data Recovery Unit in 100 Pin PQFP

Notice

This document contains information about a product during its preproduction phase of development. The information in this document is based on test results and initial product characterization. Characteristic data and other specifications are subject to change without notice. Therefore the reader is cautioned to confirm that this datasheet is current prior to design or order placement.

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