

Technical Data

NCC Series



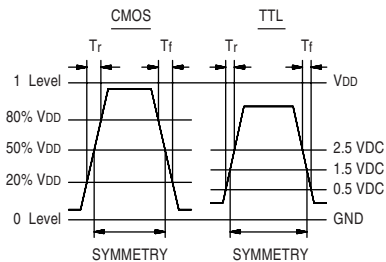
Description

A crystal controlled, low current hybrid oscillator providing precise rise and fall times to drive CMOS and NMOS micro-processors. Compatible with both CMOS and TTL. Can drive up to 2 LSTTL loads. Device is packaged in 14-pin or an 8-pin DIP compatible full size or half size, resistance welded, all metal case. Pin 7 (pin 4 for 1/2 size) is grounded to the case to reduce RFI.

Applications & Features

- Low power
- CMOS and TTL compatible output
- Enable/disable feature available
- Grounded, all metal full size and half size case

Output Waveform



Frequency Range:	62.5 kHz to 24 MHz (1/2 size - 250 kHz to 24 MHz)
Frequency Stability:	±25, ±50 or ±100 ppm over all conditions: calibration tolerance, operating temperature, input voltage change, load change, aging, shock and vibration.
Temperature Range:	Operating: 0°C to +70°C Storage: -55°C to +125°C
Supply Voltage:	Recommended Operating: 5V ±10%
Supply Current:	(See Input Current vs. Frequency Graph, page 2)
Output Drive:	
<u>CMOS</u>	Symmetry see part numbering guide Rise & Fall Times: 12ns max, 20% to 80% VDD Logic 0: 10% VDD max Logic 1: 90% VDD min Output Load: 2 CMOS
<u>TTL</u>	Symmetry see part numbering guide Rise & Fall Times: 12ns max, 0.5V to 2.5V Logic 0: 0.5V max Logic 1: 2.5V min (VCC -0.6 typ) Output Load: 2 LSTTL

Mechanical:

Shock:	MIL-STD-883, Method 2002, Condition B
Solderability:	MIL-STD-883, Method 2003
Terminal Strength:	MIL-STD-883, Method 2004, Condition B2
Vibration:	MIL-STD-883, Method 2007, Condition A
Solvent Resistance:	MIL-STD-202, Method 215
Resistance to Soldering Heat:	MIL-STD-202, Method 210, Condition A, B or C

Environmental:

Gross Leak Test:	MIL-STD-883, Method 1014, Condition C
Fine Leak Test:	MIL-STD-883, Method 1014, Condition A2
Thermal Shock:	MIL-STD-883, Method 1011, Condition A
Moisture Resistance:	MIL-STD-883, Method 1004

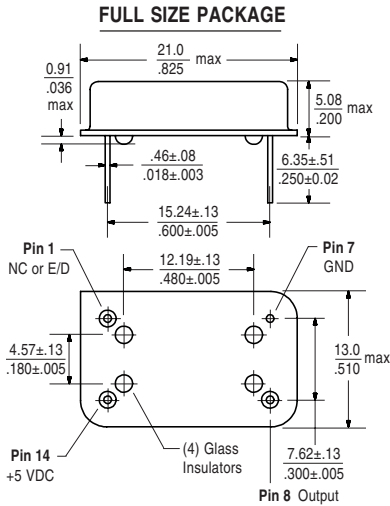
Part Numbering Guide

Series		NCC 0 6 0 C E - 4.0000		Frequency (MHz)	
Symmetry & Temperature Range		Blank = No Enable/Disable		E = Enable/ Disable	
0 = 40/60% max, 0 to 70°C		Stability Tolerance		A = ±25 ppm, 0 to +70°C only	
2 = 40/60% max, -40 to 85°C		A = ±25 ppm, 0 to +70°C only		B = ±50 ppm	
4 = 45/55% max, -40 to 85°C, TTL to 7.1590MHz		B = ±50 ppm		C = ±100 ppm	
6 = 45/55% max, 0 to 70°C, TTL to 7.1590MHz		C = ±100 ppm		Package Type	
A = 45/55% max, 0 to 70°C, CMOS to 7.1590MHz		0 = Full Size		9 = Half Size	
C = 45/55% max, -40 to 85°C, CMOS to 7.1590MHz		Frequency Range			
3 = 62.5 kHz to 4 MHz, Full Size		3 = 62.5 kHz to 4 MHz, Full Size			
250 kHz to 4 MHz, Half Size		250 kHz to 4 MHz, Half Size			
6 = 4+ MHz to 24 MHz		6 = 4+ MHz to 24 MHz			

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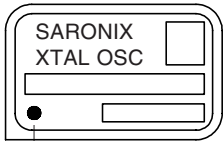
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Package Details

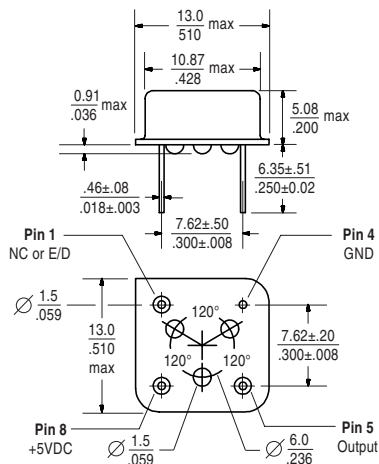


Marking Format *

Includes Date Code, Frequency & Model



HALF SIZE PACKAGE



Marking Format *

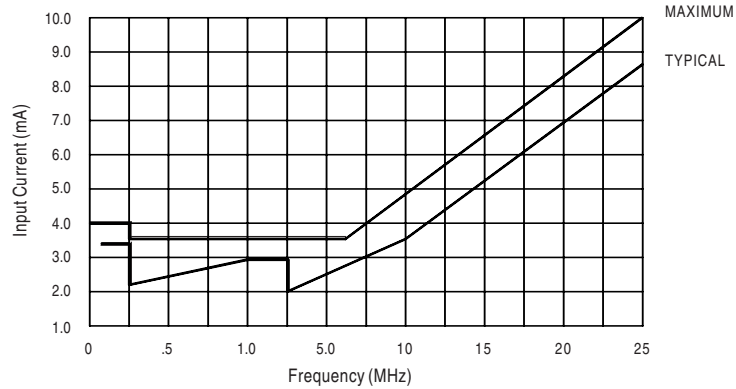
Includes Date Code, Frequency & Model



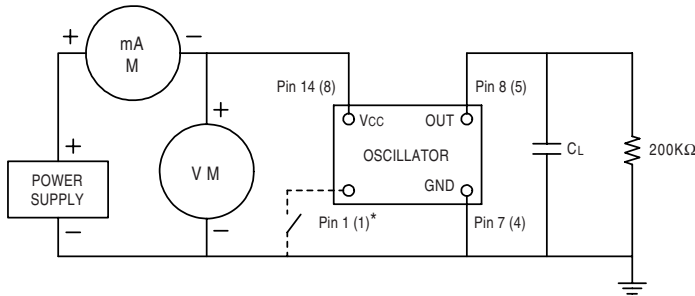
* Exact location of items may vary

Scale: None (Dimensions in $\frac{mm}{inches}$)

Input Current vs. Frequency at +5.0V



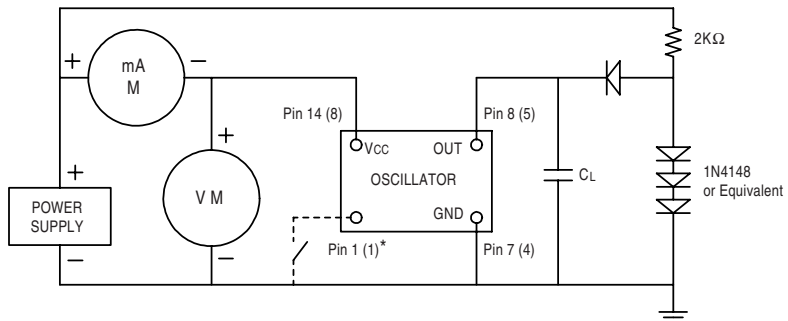
Test Circuits



NOTE:

$C_L = 15 \text{ pF}$ max (Includes probe and fixture capacitance)
Pin 1 = No connection or Enable/Disable function optional (Enable = "1" level, Disable = "0" level).
*() Indicates pin numbers for half-size package

CMOS TEST CIRCUIT



NOTE:

$C_L = 15 \text{ pF}$ max (Includes probe and fixture capacitance)
Pin 1 = No connection or Enable/Disable function optional (Enable = "1" level, Disable = "0" level).
*() Indicates pin numbers for half-size package

TTL TEST CIRCUIT

All specifications are subject to change without notice.

DS-133 REV C