Document Title

16M x 8 Bit NAND Flash Memory

Revision History

Revision No.	History	Draft Date	Remark
0.0	Initial issue.	April 10th 1999	Advanced Information

KM29U128AA16M x 8 Bit NAND Flash Memory

FEATURES

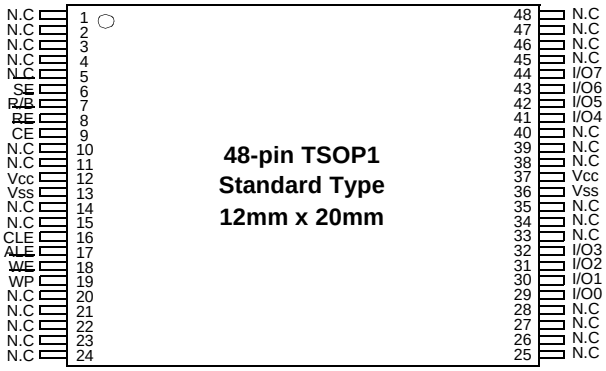
- Voltage supply : 2.7V~3.6V
- Organization
  - Memory Cell Array : (16M + 512K)bit x 8bit
  - Data Register : (512 + 16)bit x8bit
- Automatic Program and Erase
  - Page Program : (512 + 16)Byte
  - Block Erase : (16K + 512)Byte
- 528-Byte Page Read Operation
  - Random Access : 10µs(Max.)
  - Serial Page Access : 50ns(Min.)
- Fast Write Cycle Time
  - Program time : 200µs(typ.)
  - Block Erase time : 2ms(typ.)
- Command/Address/Data Multiplexed I/O port
- Hardware Data Protection
  - Program/Erase Lockout During Power Transitions
- Reliable CMOS Floating-Gate Technology
  - Endurance : 1M Program/Erase Cycles
  - Data Retention : 10 years
- Command Register Operation
- Package : 48 - pin TSOP Type1 - 12 x 20 / 0.5 mm pitch

GENERAL DESCRIPTION

The KM29U128A is a 16M(16,777,216)x8bit NAND Flash Memory with a spare 512K(524,288)x8bit. Its NAND cell provides the most cost-effective solution for the solid state mass storage market. A program operation programs the 528-byte page in typically 200µs and an erase operation can be performed in typically 2ms on a 16K-byte block. Data in the page can be read out at 50ns cycle time per byte. The I/O pins serve as the ports for address and data input/output as well as command inputs. The on-chip write controller automates all program and erase functions including pulse repetition, where required, and internal verify and margining of data. Even the write-intensive systems can take advantage of the KM29U128A′s extended reliability of 1,000,000 program/erase cycles by providing either ECC(Error Correcting Code) or real time mapping-out algorithm. These algorithms have been implemented in many mass storage applications and also the spare 16 bytes of a page combined with the other 512 bytes can be utilized by system-level ECC.

The KM29U128A is an optimum solution for large nonvolatile storage applications such as solid state file storage, digital voice recorder, digital still camera and other portable applications requiring non-volatility.

PIN CONFIGURATION



PIN DESCRIPTION

Pin Name	Pin Function
$I/O_0 \sim I/O_7$	Data Input/Outputs
CLE	Command Latch Enable
ALE	Address Latch Enable
$\overline{CE}$	Chip Enable
$\overline{RE}$	Read Enable
$\overline{WE}$	Write Enable
$\overline{WP}$	Write Protect
$\overline{SE}$	Spare area Enable
R/$\overline{B}$	Ready/Busy output
V_{CC}	Power(+2.7V~3.6V)
V_{SS}	Ground
N.C	No Connection

NOTE : Connect all V_{CC} and V_{SS} pins of each device to common power supply outputs.
Do not leave V_{CC} or V_{SS} disconnected.