

GENERAL DESCRIPTION

The XR16L2752¹ (2752) is a low voltage dual universal asynchronous receiver and transmitter (UART) with 5V tolerant inputs. The device operates from 2.5V to 5.5V supply range and is pin-to-pin compatible to Exar's ST16C2552 and XR16C2852. The 2752 register set is compatible to the ST16C2552 and the XR16C2852 enhanced features. It supports the Exar's enhanced features of 64 bytes of TX and RX FIFOs, programmable FIFO trigger level and FIFO level counters, automatic hardware (RTS/CTS) and software flow control, automatic RS-485 half duplex direction control output and a complete modem interface. Onboard registers provide the user with operational status and data error flags. An internal loopback capability allows system diagnostics. Independent programmable baud rate generators are provided in each channel to select data rates up to 3.125 Mbps at 5V. The 2752 is available in the 44-pin PLCC package.

NOTE: 1 Covered by U.S. Patent #5,649,122 and #5,832,205

APPLICATIONS

- Portable Appliances
- Telecommunication Network Routers
- Ethernet Network Routers
- Cellular Data Devices
- Factory Automation and Process Controls

FEATURES

- **2.5V, 3.3V and 5V Operation**
- **5V Tolerant Inputs**
- Pin-to-pin compatible to Exar's ST16C2552 and XR16C2852
- Improved version of PC16C552
- Two independent UART channels
 - Register set compatible to 16C550
 - Up to 6.25 Mbps at 5V, 4 Mbps at 3.3V and 3 Mbps at 2.5V with 8X sampling rate
 - Transmit and Receive FIFOs of 64 bytes
 - Programmable TX and RX FIFO Trigger Levels
 - Transmit and Receive FIFO Level Counters
 - Automatic Hardware (RTS/CTS) Flow Control
 - Selectable Auto RTS Flow Control Hysteresis
 - Automatic Software (Xon/Xoff) Flow Control
 - Automatic RS-485 Half-duplex Direction Control Output
- Wireless Infrared (IrDA 1.0) Encoder/Decoder
- Automatic sleep mode
- Full modem interface
- Alternate Function Register
- Device Identification and Revision
- Crystal oscillator or external clock input
- Industrial and commercial temperature ranges
- 44-PLCC package

FIGURE 1. XR16L2752 BLOCK DIAGRAM

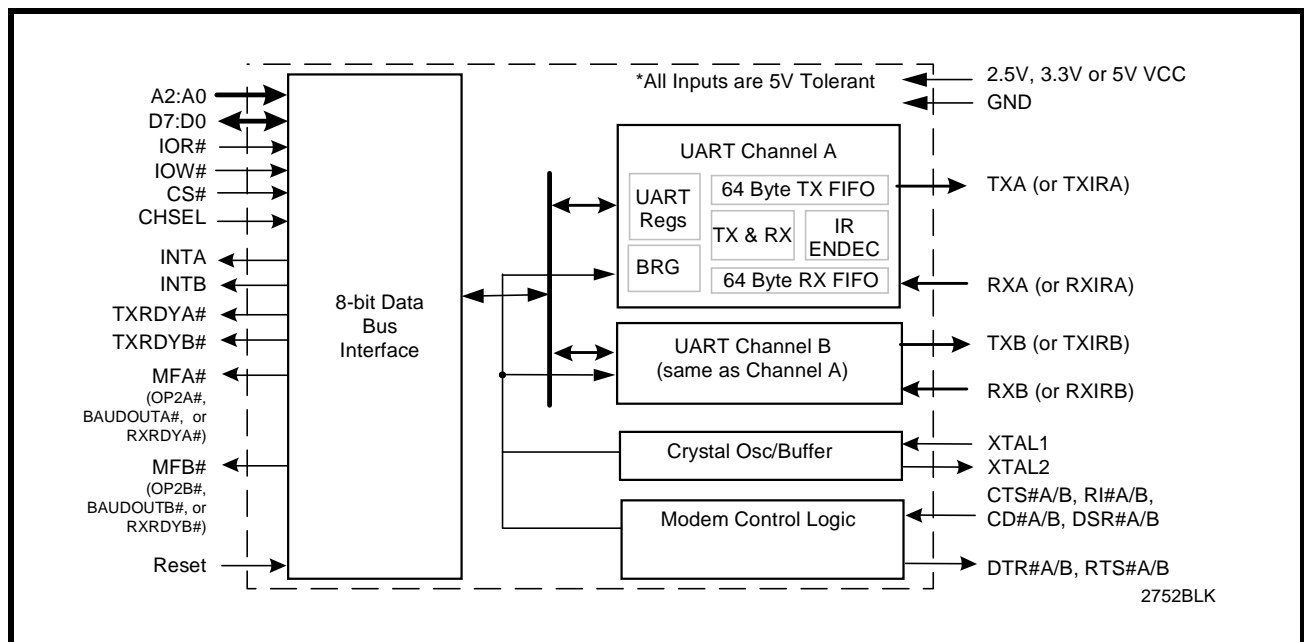
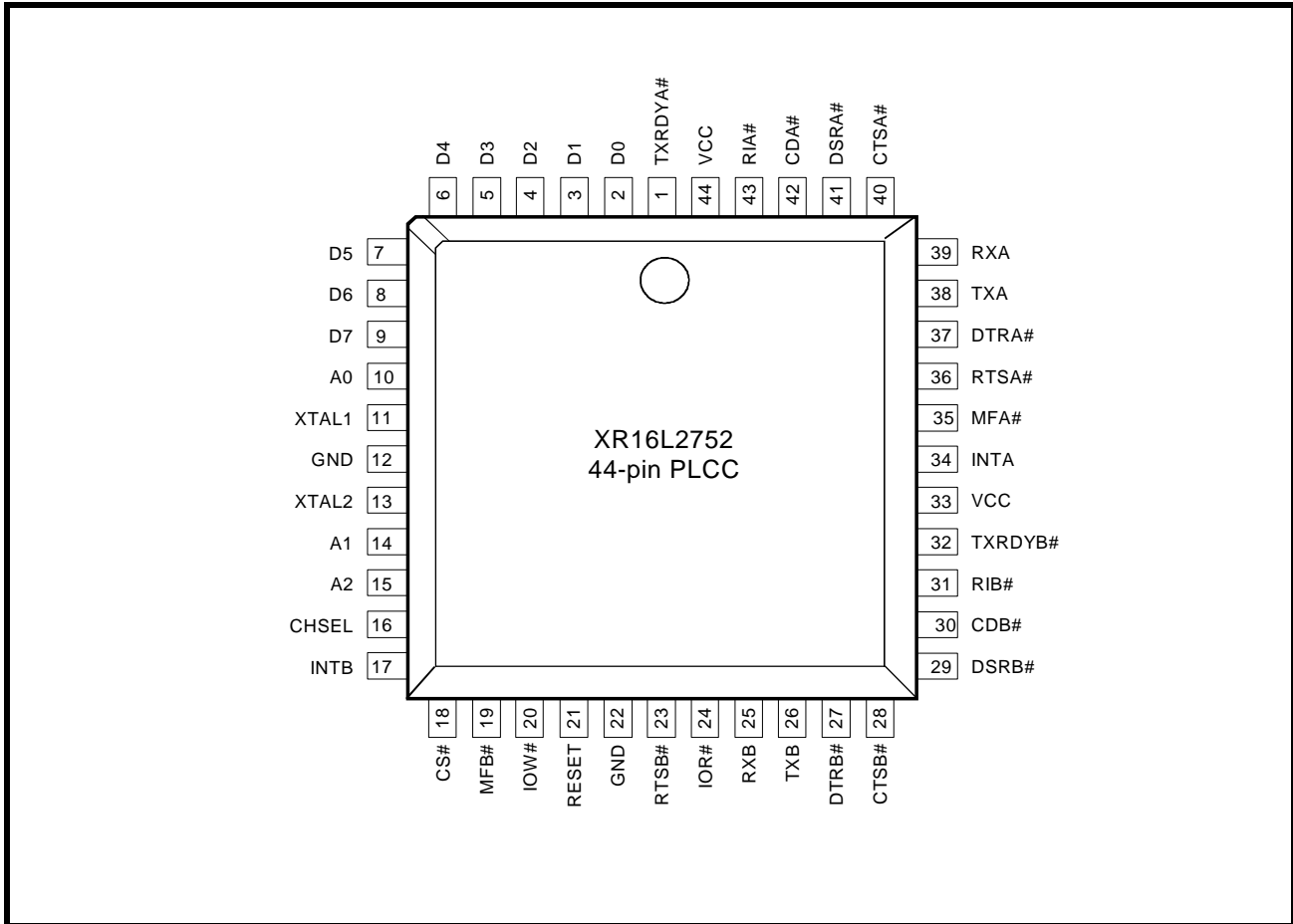


FIGURE 2. PIN OUT ASSIGNMENT



ORDERING INFORMATION

| PART NUMBER | PACKAGE | OPERATING TEMPERATURE RANGR |
|-------------|---------|-----------------------------|
| XR16L2752CJ | 44-PLCC | 0°C to +70°C |
| XR16L2752IJ | 44-PLCC | -40°C to +85°C |

PIN DESCRIPTIONS

Pin Description

| NAME | 44-PLCC PIN # | TYPE | DESCRIPTION |
|--------------------------------------|---------------------------|------|--|
| DATA BUS INTERFACE | | | |
| A2:A0 | 10, 14, 15 | I | Address data lines [2:0]. These 3 address lines select one of the internal registers in UART channel A/B during a data bus transaction. |
| D7:D0 | 9, 8, 7, 6, 5, 4, 3, 2 | I/O | Data bus lines [7:0] (bidirectional). |
| IOR# | 24 | I | Input/Output Read Strobe (active low). The falling edge instigates an internal read cycle and retrieves the data byte from an internal register pointed to by the address lines [A2:A0]. The data byte is placed on the data bus to allow the host processor to read it on the rising edge. |
| IOW# | 20 | I | Input/Output Write Strobe (active low). The falling edge instigates an internal write cycle and the rising edge transfers the data byte on the data bus to an internal register pointed to by the address lines. |
| CS# | 18 | I | UART chip select (active low). This function selects channel A or B in accordance with the logical state of the CHSEL pin. This allows data to be transferred between the user CPU and the 2752. |
| CHSEL | 16 | I | Channel Select - UART channel A or B is selected by the logical state of this pin when the CS# pin is a logic 0. A logic 0 on the CHSEL selects the UART channel B while a logic 1 selects UART channel A. Normally, CHSEL could just be an address line from the user CPU such as A4. Bit-0 of the Alternate Function Register (AFR) can temporarily override CHSEL function, allowing the user to write to both channel register simultaneously with one write cycle when CS# is low. It is especially useful during the initialization routine. |
| INTA | 34 | O | UART channel A Interrupt output (active high). A logic high indicates channel A is requesting for service. For more details, see Figures 17 - 22 . |
| INTB | 17 | O | UART channel B Interrupt output (active high). A logic high indicates channel B is requesting for service. For more details, see Figures 17 - 22 . |
| TXRDYA# | 1 | O | UART channel A Transmitter Ready (active low). The output provides the TX FIFO/THR status for transmit channel A. See Table 2 . |
| TXRDYB# | 32 | O | UART channel B Transmitter Ready (active low). The output provides the TX FIFO/THR status for transmit channel B. See Table 2 . |
| MODEM OR SERIAL I/O INTERFACE | | | |
| MFA# | 35 | O | Multi-Function Output Channel A. This output pin can function as the OP2A#, BAUD-OUTA#, or RXRDYA# pin. One of these output signal functions can be selected by the user programmable bits 1-2 of the Alternate Function Register (AFR). These signal functions are described as follows: 1) OP2A# - When OP2A# (active low) is selected, the MF# pin is a logic 0 when MCR bit-3 is set to a logic 1 (see MCR bit-3). MCR bit-3 defaults to a logic 1 condition after a reset or power-up. 2) BAUDOUTA# - When BAUDOUTA# function is selected, the 16X Baud rate clock output is available at this pin. 3) RXRDYA# - RXRDYA# (active low) is intended for monitoring DMA data transfers. See Table 2 for more details. |

Pin Description

| NAME | 44-PLCC PIN # | TYPE | DESCRIPTION |
|-------|---------------|------|---|
| MFB# | 19 | O | Multi-Function Output ChannelB. This output pin can function as the OP2B#, BAUD-OUTB#, or RXRDYB# pin. One of these output signal functions can be selected by the user programmable bits 1-2 of the Alternate Function Register (AFR). These signal functions are described as follows: 1) OP2B# - When OP2B# (active low) is selected, the MF# pin is a logic 0 when MCR bit-3 is set to a logic 1 (see MCR bit-3). MCR bit-3 defaults to a logic 1 condition after a reset or power-up. 2) BAUDOUTB# - When BAUDOUTB# function is selected, the 16X Baud rate clock output is available at this pin. 3) RXRDYB# - RXRDYB# (active low) is intended for monitoring DMA data transfers. See Table 2 for more details. |
| TXA | 38 | O | UART channel A Transmit Data or infrared encoder data. Standard transmit and receive interface is enabled when MCR[6] = 0. In this mode, the TX signal will be a logic 1 during reset or idle (no data). Infrared IrDA transmit and receive interface is enabled when MCR[6] = 1. In the Infrared mode, the inactive state (no data) for the Infrared encoder/decoder interface is a logic 0. If it is not used, leave it unconnected. |
| RXA | 39 | I | UART channel A Receive Data or infrared receive data. Normal receive data input must idle at logic 1 condition. The infrared receiver pulses typically idles at logic 0 but can be inverted by software control prior going in to the decoder, see MCR[6] and FCTR[2]. If this pin is not used, tie it to VCC or pull it high via a 100k ohm resistor. |
| RTSA# | 36 | O | UART channel A Request-to-Send (active low) or general purpose output. This output must be asserted prior to using auto RTS flow control, see EFR[6], MCR[1], FCTR[1:0], EMSR[5:4] and IER[6]. |
| CTSA# | 40 | I | UART channel A Clear-to-Send (active low) or general purpose input. It can be used for auto CTS flow control, see EFR[7], and IER[7]. This input should be connected to VCC when not used. |
| DTRA# | 37 | O | UART channel A Data-Terminal-Ready (active low) or general purpose output. If this pin is not used, leave it unconnected. |
| DSRA# | 41 | I | UART channel A Data-Set-Ready (active low) or general purpose input. This input should be connected to VCC when not used. This input has no effect on the UART. |
| CDA# | 42 | I | UART channel A Carrier-Detect (active low) or general purpose input. This input should be connected to VCC when not used. This input has no effect on the UART. |
| RIA# | 43 | I | UART channel A Ring-Indicator (active low) or general purpose input. This input should be connected to VCC when not used. This input has no effect on the UART. |
| TXB | 26 | O | UART channel B Transmit Data or infrared encoder data. Standard transmit and receive interface is enabled when MCR[6] = 0. In this mode, the TX signal will be a logic 1 during reset or idle (no data). Infrared IrDA transmit and receive interface is enabled when MCR[6] = 1. In the Infrared mode, the inactive state (no data) for the Infrared encoder/decoder interface is a logic 0. If it is not used, leave it unconnected. |
| RXB | 25 | I | UART channel B Receive Data or infrared receive data. Normal receive data input must idle at logic 1 condition. The infrared receiver pulses typically idles at logic 0 but can be inverted by software control prior going in to the decoder, see MCR[6] and FCTR[2]. If this pin is not used, tie it to VCC or pull it high via a 100k ohm resistor. |
| RTSB# | 23 | O | UART channel B Request-to-Send (active low) or general purpose output. This port must be asserted prior to using auto RTS flow control, see EFR[6], MCR[1], FCTR[1:0], EMSR[5:4] and IER[6]. |

Pin Description

| NAME | 44-PLCC PIN # | TYPE | DESCRIPTION |
|--------------------------|---------------|------|---|
| CTSB# | 28 | I | UART channel B Clear-to-Send (active low) or general purpose input. It can be used for auto CTS flow control, see EFR[7], and IER[7]. This input should be connected to VCC when not used. |
| DTRB# | 27 | O | UART channel B Data-Terminal-Ready (active low) or general purpose output. If this pin is not used, leave it unconnected. |
| DSRB# | 29 | I | UART channel B Data-Set-Ready (active low) or general purpose input. This input should be connected to VCC when not used. This input has no effect on the UART. |
| CDB# | 30 | I | UART channel B Carrier-Detect (active low) or general purpose input. This input should be connected to VCC when not used. This input has no effect on the UART. |
| RIB# | 31 | I | UART channel B Ring-Indicator (active low) or general purpose input. This input should be connected to VCC when not used. This input has no effect on the UART. |
| ANCILLARY SIGNALS | | | |
| XTAL1 | 11 | I | Crystal or external clock input. |
| XTAL2 | 13 | O | Crystal or buffered clock output. |
| RESET | 21 | I | Reset (active high) - A longer than 40 ns logic 1 pulse on this pin will reset the internal registers and all outputs. The UART transmitter output will be held at logic 1, the receiver input will be ignored and outputs are reset during reset period (see External Reset Conditions). |
| VCC | 44, 33 | Pwr | 2.5V to 5.5V power supply. All input pins are 5V tolerant. |
| GND | 22, 12 | Pwr | Power supply common, ground. |

Pin type: I=Input, O=Output, I/O= Input/output, OD=Output Open Drain.

1.0 PRODUCT DESCRIPTION

The XR16L2752 (2752) integrates the functions of 2 enhanced 16C550 Universal Asynchronous Receiver and Transmitter (UART). Each UART is independently controlled having its own set of device configuration registers. The configuration registers set is 16550 UART compatible for control, status and data transfer. Additionally, each UART channel has 64-bytes of transmit and receive FIFOs, automatic RTS/CTS hardware flow control with hysteresis control, automatic Xon/Xoff and special character software flow control, programmable transmit and receive FIFO trigger levels, FIFO level counters, infrared encoder and decoder (IrDA ver 1.0), programmable baud rate generator with a prescaler of divide by 1 or 4, and data rate up to 3.125Mbps. The XR16L2752 is a 5V, 3.3V and 2.5V device with 5 volt tolerant inputs. The 2752 is fabricated with an advanced CMOS process.

Enhanced Features

The 2752 DUART provides a solution that supports 64 bytes of transmit and receive FIFO memory, instead of 128 bytes provided in the XR16C2852 and 16 bytes in the ST16C2552. The 2752 is designed to work with low supply voltage and high performance data communication systems, that require fast data processing time. Increased performance is realized in the 2752 by the larger transmit and receive FIFOs, FIFO trigger level control, FIFO level counters and automatic flow control mechanism. This allows the external processor to handle more networking tasks within a given time. For example, the ST16C2552 with a 16 byte FIFO, unloads 16 bytes of receive data in 1.53 ms (This example uses a character length of 11 bits, including start/stop bits at 115.2Kbps). This means the external CPU will have to service the receive FIFO at 1.53 ms intervals. However with the 64 byte FIFO in the 2752, the data buffer will not require unloading/loading for 6.1 ms. This increases the service interval giving the external CPU additional time for other applications and reducing the overall

UART interrupt servicing time. In addition, the programmable FIFO level trigger interrupt and automatic hardware/software flow control is uniquely provided for maximum data throughput performance especially when operating in a multi-channel system. The combination of the above greatly reduces the CPU's bandwidth requirement, increases performance, and reduces power consumption.

The 2752 supports a half-duplex output direction control signaling pin, RTS# A/B, to enable and disable the external RS-485 transceiver operation. It automatically switches the logic state of the output pin to the receive state after the last stop-bit of the last character has been shifted out of the transmitter. After receiving, the logic state of the output pin switches back to the transmit state when a data byte is loaded in the transmitter. The auto RS-485 direction control pin is not activated after reset. To activate the direction control function, user has to set FCTR Bit-3 to "1". This pin is normally high for receive state, low for transmit state.

Data Rate

The 2752 is capable of operation up to 3.125Mbps at 5V with 16x internal sampling clock rate. The device can operate with an external 24 MHz crystal on pins XTAL1 and XTAL2, or external clock source of up to 50MHz on XTAL1 pin. With a typical crystal of 14.7464 MHz and through a software option, the user can set the prescaler bit for data rates of up to 921.6Kbps.

The rich feature set of the 2752 is available through the internal registers. Automatic hardware/software flow control, selectable transmit and receive FIFO trigger levels, selectable TX and RX baud rates, infrared encoder/decoder interface, modem interface controls, and a sleep mode are all standard features. Following a power on reset or an external reset, the 2752 is software compatible with previous generation of UARTs 16C2552 and 16C2852.

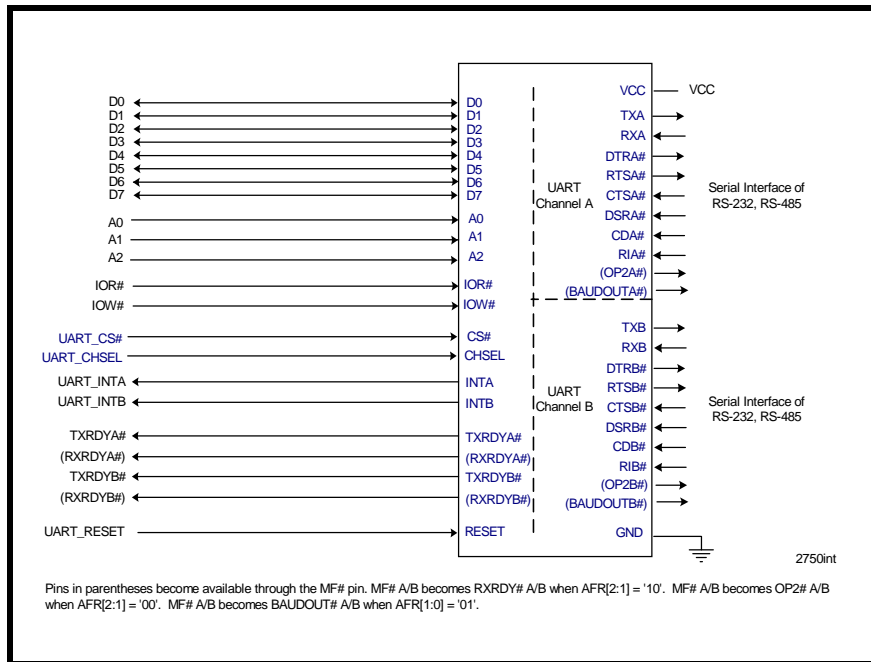
2.0 FUNCTIONAL DESCRIPTIONS

2.1 CPU INTERFACE

The CPU interface is 8 data bits wide with 3 address lines and control signals to execute data bus read and write transactions. The 2752 data interface supports the Intel compatible types of CPUs and it is compatible to the industry standard 16C550 UART. No clock

(oscillator nor external clock) is required to operate a data bus transaction. Each bus cycle is asynchronous using CS#, IOR# and IOW# signals. Both UART channels share the same data bus for host operations. The data bus interconnections are shown in Figure 3.

FIGURE 3. XR16L2752 DATA BUS INTERCONNECTIONS



2.2 5-VOLT TOLERANT INPUTS

The 2752 can accept up to 5V inputs even when operating at 3.3V or 2.5V. But note that if the 2752 is operating at 2.5V, its V_{OH} may not be high enough to meet the requirements of the V_{IH} of a CPU or a serial transceiver that is operating at 5V.

2.3 DEVICE RESET

The RESET input resets the internal registers and the serial interface outputs in both channels to their default state (see Table 16). An active high pulse of longer than 40 ns duration will be required to activate the reset function in the device.

2.4 DEVICE IDENTIFICATION AND REVISION

The XR16L2752 provides a Device Identification code and a Device Revision code to distinguish the part from other devices and revisions. To read the identification code from the part, it is required to set the baud rate generator registers DLL and DLM both to 0x00. Now reading the content of the DLM will provide 0x0A for the XR16L2752 and reading the content

of DLL will provide the revision of the part; for example, a reading of 0x01 means revision A.

2.5 CHANNEL A AND B SELECTION

The UART provides the user with the capability to bi-directionally transfer information between an external CPU and an external serial communication device. A logic 0 on chip select pin (CS#) allows the user to select the UART and then using the channel select (CHSEL) pin, the user can select channel A or B to configure, send transmit data and/or unload receive data to/from the UART. Individual channel select functions are shown in Table 1.

TABLE 1: CHANNEL A AND B SELECT

| CS# | CHSEL | FUNCTION |
|-----|-------|--------------------|
| 1 | X | UART de-selected |
| 0 | 1 | Channel A selected |
| 0 | 0 | Channel B selected |

2.6 CHANNEL A AND B INTERNAL REGISTERS

Each UART channel in the 2752 has a set of enhanced registers for control, monitoring and data loading and unloading. The configuration register set is compatible to those already available in the standard single 16C550 and dual ST16C2550. These registers function as data holding registers (THR/RHR), interrupt status and control registers (ISR/IER), a FIFO control register (FCR), receive line status and control registers (LSR/LCR), modem status and control registers (MSR/MCR), programmable data rate (clock) divisor registers (DLL/DLM), and a user accessible scratchpad register (SPR).

Beyond the general 16C2550 features and capabilities, the 2752 offers enhanced feature registers (AFR, EMSR, FLVL, EFR, Xon/Xoff 1, Xon/Xoff 2, FCTR, TRG, FC) that provide automatic RTS and CTS hardware flow control, Xon/Xoff software flow control, automatic RS-485 half-duplex direction output enable/disable, FIFO trigger level control, FIFO level counters, and simultaneous writes to both channels. All the register functions are discussed in full detail later in "UART INTERNAL REGISTERS" on page 18.

2.7 SIMULTANEOUS WRITE TO CHANNEL A AND B

During a write mode cycle, the setting of Alternate Function Register (AFR) bit-0 to a logic 1 will override the CHSEL selection and allows a simultaneous write to both UART channel sections. This functional capability allow the registers in both UART channels to be modified concurrently, saving individual channel ini-

tialization time. Caution should be considered, however, when using this capability. Any in-process serial data transfer may be disrupted by changing an active channel's mode.

2.8 DMA MODE

The device does not support direct memory access. The DMA Mode (a legacy term) in this document doesn't mean "direct memory access" but refers to data block transfer operation. The DMA mode affects the state of the RXRDY# A/B (MF# A/B becomes RXRDY# A/B output when AFR[2:1] = '10') and TXRDY# A/B output pins. The transmit and receive FIFO trigger levels provide additional flexibility to the user for block mode operation. The LSR bits 5-6 provide an indication when the transmitter is empty or has an empty location(s) for more data. The user can optionally operate the transmit and receive FIFO in the DMA mode (FCR bit-3=1). When the transmit and receive FIFO are enabled and the DMA mode is disabled (FCR bit-3 = 0), the 2752 is placed in single-character mode for data transmit or receive operation. When DMA mode is enabled (FCR bit-3 = 1), the user takes advantage of block mode operation by loading or unloading the FIFO in a block sequence determined by the programmed trigger level. In this mode, the 2752 sets the TXRDY# pin when the transmit FIFO becomes full, and sets the RXRDY# pin when the receive FIFO becomes empty. The following table shows their behavior. Also see Figures 17 through 22 .

TABLE 2: TXRDY# AND RXRDY# OUTPUTS IN FIFO AND DMA MODE

| PINS | FCR BIT-0=0 (FIFO DISABLED) | FCR BIT-0=1 (FIFO ENABLED) | |
|------------|------------------------------------|---|---|
| | | FCR Bit-3 = 0 (DMA Mode Disabled) | FCR Bit-3 = 1 (DMA Mode Enabled) |
| RXRDY# A/B | 0 = 1 byte. 1 = no data. | 0 = at least 1 byte in FIFO 1 = FIFO empty. | 1 to 0 transition when FIFO reaches the trigger level, or timeout occurs. 0 to 1 transition when FIFO empties. |
| TXRDY# A/B | 0 = THR empty. 1 = byte in THR. | 0 = FIFO empty. 1 = at least 1 byte in FIFO. | 0 = FIFO has at least 1 empty location. 1 = FIFO is full. |

2.9 INTA AND INTB OUPUTS

The INTA and INTB interrupt output changes according to the operating mode and enhanced features

setup. Table 3 and 4 summarize the operating behavior for the transmitter and receiver. Also see Figures 17 through 22 .

TABLE 3: INTA AND INTB PINS OPERATION FOR TRANSMITTER

| | Auto RS485 Mode | FCR BIT-0 = 0 (FIFO DISABLED) | FCR BIT-0 = 1 (FIFO ENABLED) |
|------------|-----------------|--|---|
| INTA/B Pin | NO | 0 = a byte in THR 1 = THR empty | 0 = FIFO above trigger level 1 = FIFO below trigger level or FIFO empty |
| INTA/B Pin | YES | 0 = a byte in THR 1 = transmitter empty | 0 = FIFO above trigger level 1 = FIFO below trigger level or transmitter empty |

TABLE 4: INTA AND INTB PIN OPERATION FOR RECEIVER

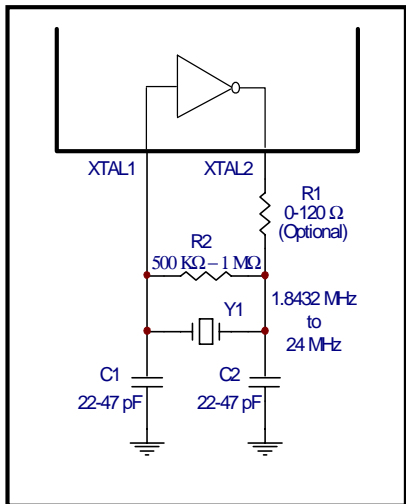
| | FCR BIT-0 = 0 (FIFO DISABLED) | FCR BIT-0 = 1 (FIFO ENABLED) |
|------------|-------------------------------|--|
| INTA/B Pin | 0 = no data 1 = 1 byte | 0 = FIFO below trigger level 1 = FIFO above trigger level |

2.10 CRYSTAL OSCILLATOR OR EXT. CLOCK INPUT

The 2752 includes an on-chip oscillator (XTAL1 and XTAL2) to produce a clock for both UART sections in the device. The CPU data bus does not require this clock for bus operation. The crystal oscillator provides a system clock to the Baud Rate Generators (BRG) section found in each of the UART. XTAL1 is the input to the oscillator or external clock buffer input with XTAL2 pin being the output. For programming details, see “Programmable Baud Rate Generator.”

The on-chip oscillator is designed to use an industry standard microprocessor crystal (parallel resonant, fundamental frequency with 10-22 pF capacitance load, ESR of 20-80 ohms and 100ppm frequency tolerance) connected externally between the XTAL1 and XTAL2 pins (see Figure 4). Alternatively, an external clock can be connected to the XTAL1 pin to clock the internal baud rate generator for standard or custom rates. Typical oscillator connections are shown in Figure 4. For further reading on oscillator circuit please see application note DAN108 on EXAR’s web site.

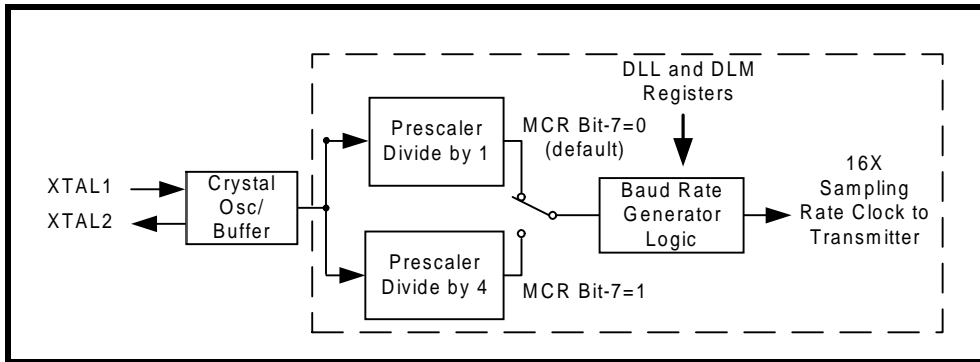
FIGURE 4. TYPICAL OSCILLATOR CONNECTIONS



2.11 PROGRAMMABLE BAUD RATE GENERATOR

Each UART has its own Baud Rate Generator (BRG) with a prescaler. The prescaler is controlled by a software bit in the MCR register. The MCR register bit-7 sets the prescaler to divide the input crystal or external clock by 1 or 4. The clock output of the prescaler goes to the BRG. The BRG further divides this clock by a programmable divisor between 1 and $(2^{16} - 1)$ to obtain a 16X sampling rate clock of the serial data rate. The sampling rate clock is used by the transmitter for data bit shifting and receiver for data sampling. The BRG divisor defaults to the maximum baud rate (DLL = 0x01 and DLM = 0x00) upon power up.

FIGURE 5. BAUD RATE GENERATOR AND PRESCALER



Programming the Baud Rate Generator Registers DLM and DLL provides the capability of selecting the operating data rate. Table 5 shows the standard data rates available with a 14.7456 MHz crystal or external

clock at 16X sampling rate clock rate. When using a non-standard data rate crystal or external clock, the divisor value can be calculated for DLL/DLM with the following equation.

$$\text{divisor (decimal)} = (\text{XTAL1 clock frequency} / \text{prescaler}) / (\text{serial data rate} \times 16)$$

TABLE 5: TYPICAL DATA RATES WITH A 14.7456 MHz CRYSTAL OR EXTERNAL CLOCK

| OUTPUT Data Rate MCR Bit-7=1 | OUTPUT Data Rate MCR Bit-7=0 (DEFAULT) | DIVISOR FOR 16x Clock (Decimal) | DIVISOR FOR 16x Clock (HEX) | DLM PROGRAM VALUE (HEX) | DLL PROGRAM VALUE (HEX) | DATA RATE ERROR (%) |
|---------------------------------|--|------------------------------------|--------------------------------|-------------------------------|-------------------------------|------------------------|
| 100 | 400 | 2304 | 900 | 09 | 00 | 0 |
| 600 | 2400 | 384 | 180 | 01 | 80 | 0 |
| 1200 | 4800 | 192 | C0 | 00 | C0 | 0 |
| 2400 | 9600 | 96 | 60 | 00 | 60 | 0 |
| 4800 | 19.2k | 48 | 30 | 00 | 30 | 0 |
| 9600 | 38.4k | 24 | 18 | 00 | 18 | 0 |
| 19.2k | 76.8k | 12 | 0C | 00 | 0C | 0 |
| 38.4k | 153.6k | 6 | 06 | 00 | 06 | 0 |
| 57.6k | 230.4k | 4 | 04 | 00 | 04 | 0 |
| 115.2k | 460.8k | 2 | 02 | 00 | 02 | 0 |
| 230.4k | 921.6k | 1 | 01 | 00 | 01 | 0 |

2.12 TRANSMITTER

The transmitter section comprises of an 8-bit Transmit Shift Register (TSR) and 64 bytes of FIFO which includes a byte-wide Transmit Holding Register (THR). TSR shifts out every data bit with the 16X internal clock. A bit time is 16 clock periods (see EMSR bit-7). The transmitter sends the start-bit followed by the number of data bits, inserts the proper parity-bit if enabled, and adds the stop-bit(s). The status of the FIFO and TSR are reported in the Line Status Register (LSR bit-5 and bit-6).

2.12.1 Transmit Holding Register (THR) - Write Only

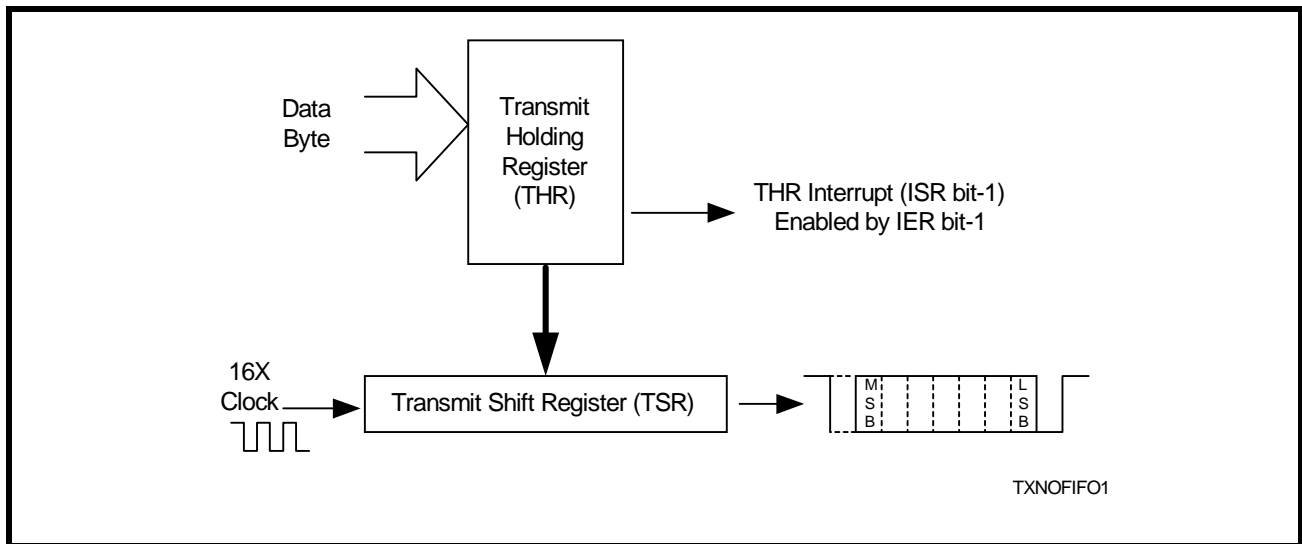
The transmit holding register is an 8-bit register providing a data interface to the host processor. The host writes transmit data byte to the THR to be converted

into a serial data stream including start-bit, data bits, parity-bit and stop-bit(s). The least-significant-bit (Bit-0) becomes first data bit to go out. The THR is the input register to the transmit FIFO of 64 bytes when FIFO operation is enabled by FCR bit-0. Every time a write operation is made to the THR, the FIFO data pointer is automatically bumped to the next sequential data location.

2.12.2 Transmitter Operation in non-FIFO Mode

The host loads transmit data to THR one character at a time. The THR empty flag (LSR bit-5) is set when the data byte is transferred to TSR. THR flag can generate a transmit empty interrupt (ISR bit-1) when it is enabled by IER bit-1. The TSR flag (LSR bit-6) is set when TSR becomes completely empty.

FIGURE 6. TRANSMITTER OPERATION IN NON-FIFO MODE

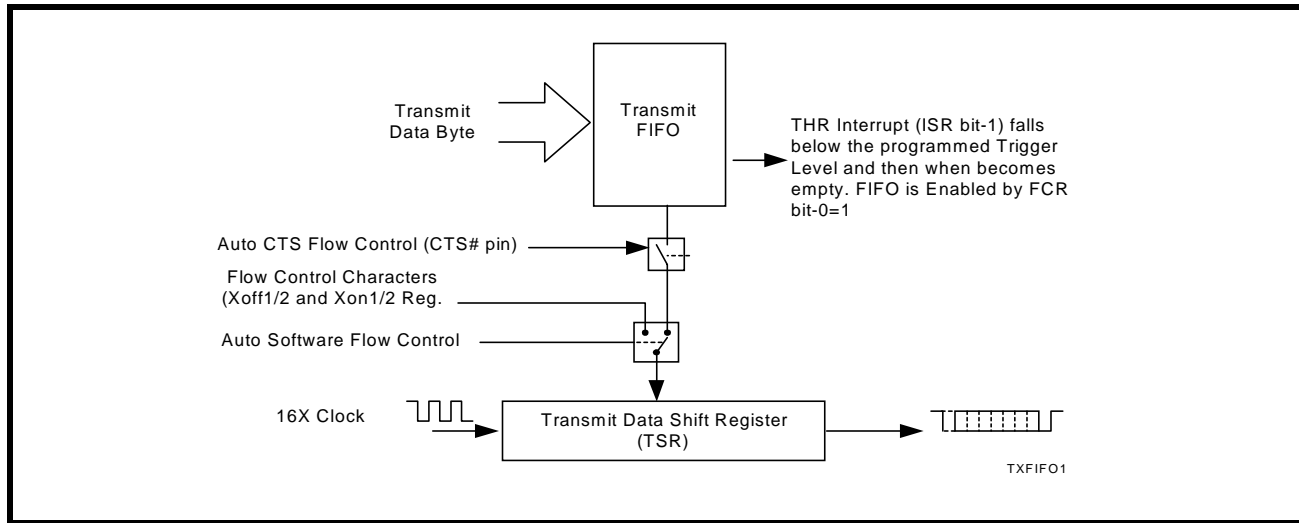


2.12.3 Transmitter Operation in FIFO Mode

The host may fill the transmit FIFO with up to 64 bytes of transmit data. The THR empty flag (LSR bit-5) is set whenever the FIFO is empty. The THR empty flag can generate a transmit empty interrupt (ISR bit-1)

when the amount of data in the FIFO falls below its programmed trigger level. The transmit empty interrupt is enabled by IER bit-1. The TSR flag (LSR bit-6) is set when TSR/FIFO becomes empty.

FIGURE 7. TRANSMITTER OPERATION IN FIFO AND FLOW CONTROL MODE



2.13 RECEIVER

The receiver section contains an 8-bit Receive Shift Register (RSR) and 64 bytes of FIFO which includes a byte-wide Receive Holding Register (RHR). The RSR uses the 16X for timing. It verifies and validates every bit on the incoming character in the middle of each data bit. On the falling edge of a start or false start bit, an internal receiver counter starts counting at the 16X. After 8 clocks the start bit period should be at the center of the start bit. At this time the start bit is sampled and if it is still a logic 0 it is validated. Evaluating the start bit in this manner prevents the receiver from assembling a false character. The rest of the data bits and stop bits are sampled and validated in this same manner to prevent false framing. If there were any error(s), they are reported in the LSR register bits 2-4. Upon unloading the receive data byte from RHR, the receive FIFO pointer is bumped and the error tags are immediately updated to reflect the status of the data byte in RHR register. RHR can generate a receive data ready interrupt upon receiving a character or delay until it reaches the FIFO trig-

ger level. Furthermore, data delivery to the host is guaranteed by a receive data ready time-out interrupt when data is not received for 4 word lengths as defined by LCR[1,0] plus 12 bits time. This is equivalent to 3.7-4.6 character times. The RHR interrupt is enabled by IER bit-0.

2.13.1 Receive Holding Register (RHR) - Read-Only

The Receive Holding Register is an 8-bit register that holds a receive data byte from the Receive Shift Register. It provides the receive data interface to the host processor. The RHR register is part of the receive FIFO of 64 bytes by 11-bits wide, the 3 extra bits are for the 3 error tags to be reported in LSR register. When the FIFO is enabled by FCR bit-0, the RHR contains the first data character received by the FIFO. After the RHR is read, the next character byte is loaded into the RHR and the errors associated with the current data byte are immediately updated in the LSR bits 2-4.

FIGURE 8. RECEIVER OPERATION IN NON-FIFO MODE

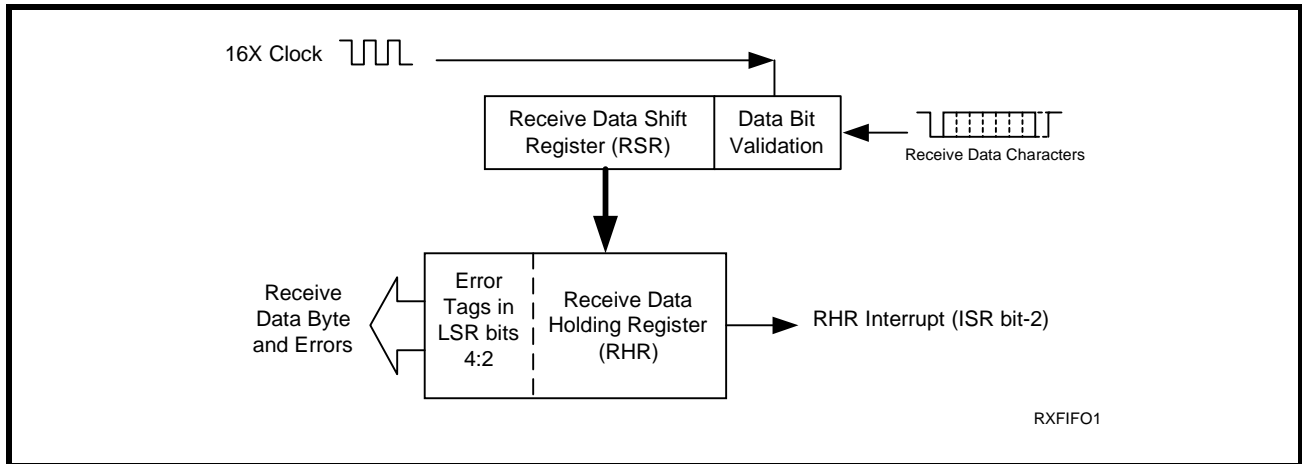
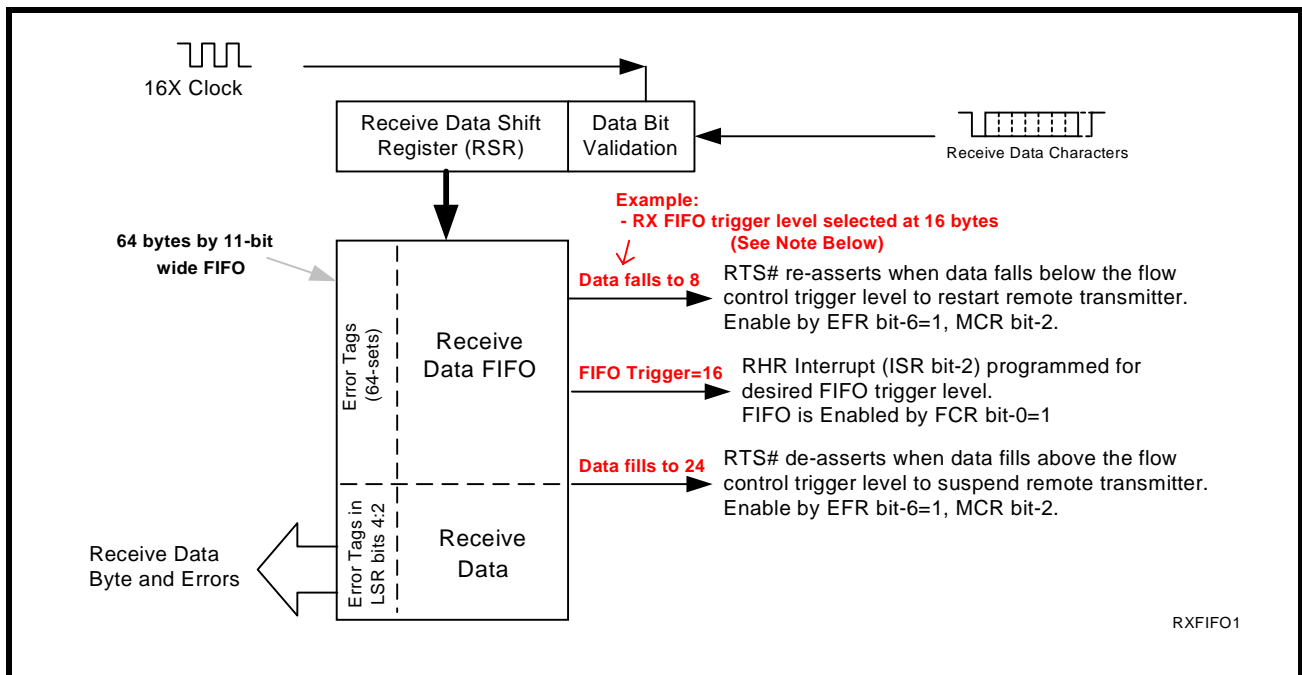


FIGURE 9. RECEIVER OPERATION IN FIFO AND AUTO RTS FLOW CONTROL MODE



NOTE: Table-B selected as Trigger Table for Figure 9 (Table 10).

2.14 AUTO RTS (HARDWARE) FLOW CONTROL

Automatic RTS hardware flow control is used to prevent data overrun to the local receiver FIFO. The RTS# output is used to request remote unit to suspend/resume data transmission. The auto RTS flow control features is enabled to fit specific application requirement (see Figure 10):

- Enable auto RTS flow control using EFR bit-6.
- The auto RTS function must be started by asserting RTS# output pin (MCR bit-1 to logic 1 after it is enabled).
- Enable RTS interrupt through IER bit-6 (after setting

EFR bit-4). The UART issues an interrupt when the RTS# pin makes a transition from low to high: ISR bit-5 will be set to logic 1.

2.15 AUTO RTS HYSTERESIS

The 2752 has a new feature that provides flow control trigger hysteresis while maintaining compatibility with the XR16C850, ST16C650A and ST16C550 family of UARTs. With the Auto RTS function enabled, an interrupt is generated when the receive FIFO reaches the programmed RX trigger level. The RTS# pin will not be forced to a logic 1 (RTS off), until the receive FIFO reaches the upper limit of the hysteresis level.

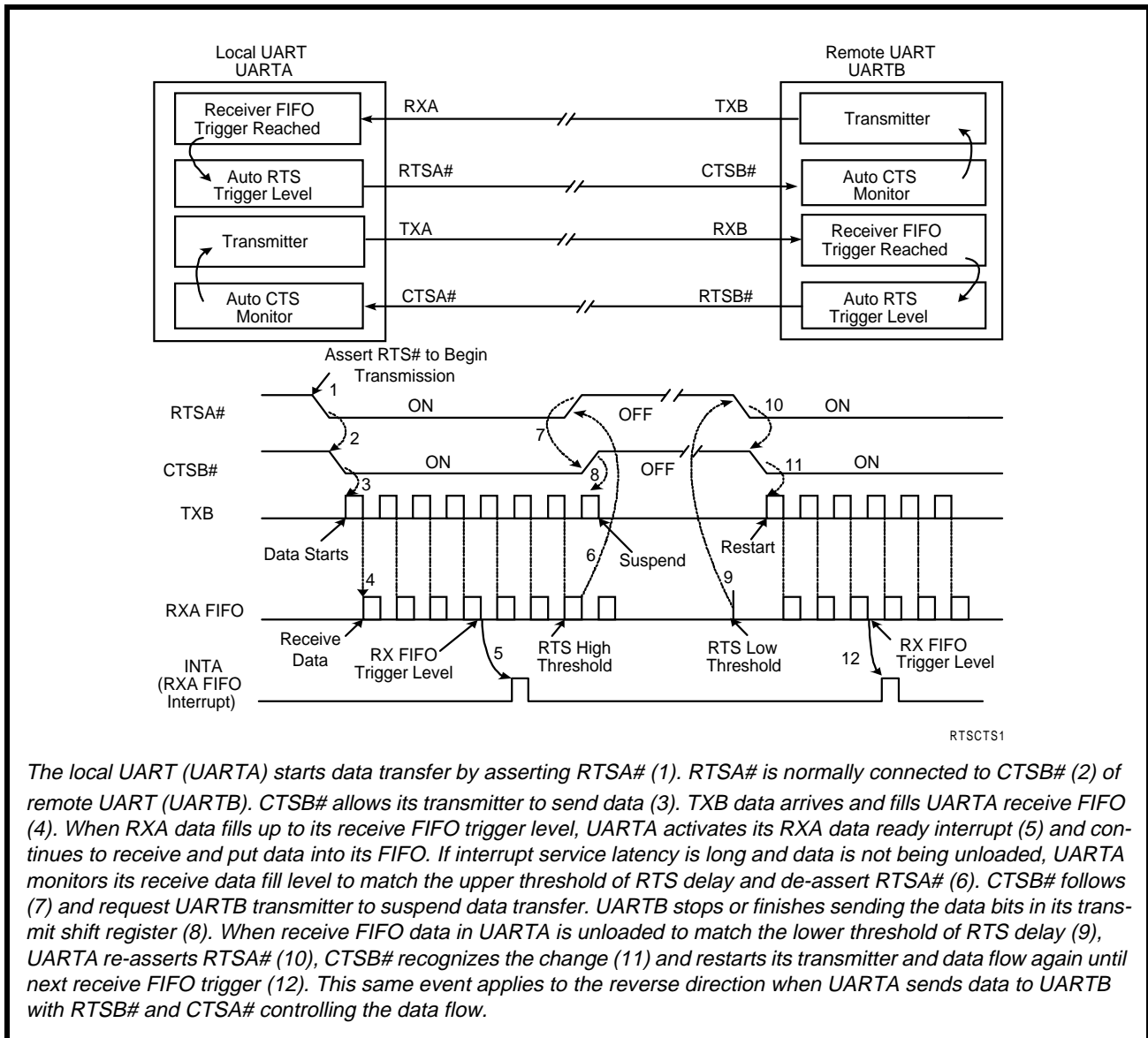
The RTS# pin will return to a logic 0 after the RX FIFO is unloaded to the lower limit of the hysteresis level. Under the above described conditions, the 2752 will continue to accept data until the receive FIFO gets full. The Auto RTS function is initiated when the RTS# output pin is asserted to a logic 0 (RTS On). Table 13 shows the complete details for the Auto RTS# Hysteresis levels. Please note that this table is for programmable trigger levels only (Table D). The hysteresis values for Tables A-C are the next higher and next lower trigger levels in Tables A-C.

2.16 AUTO CTS FLOW CONTROL

Automatic CTS flow control is used to prevent data overrun to the remote receiver FIFO. The CTS# input is monitored to suspend/restart the local transmitter. The auto CTS flow control feature is selected to fit specific application requirement (see Figure 10):

- Enable auto CTS flow control using EFR bit-7.
- Enable CTS interrupt through IER bit-7 (after setting EFR bit-4). The UART issues an interrupt when the CTS# pin is de-asserted (logic 1): ISR bit-5 will be set to 1, and UART will suspend transmission as soon as the stop bit of the character in process is shifted out. Transmission is resumed after the CTS# input is re-asserted (logic 0), indicating more data may be sent.

FIGURE 10. AUTO RTS AND CTS FLOW CONTROL OPERATION



2.17 AUTO XON/XOFF (SOFTWARE) FLOW CONTROL

When software flow control is enabled (See Table 15), the 2752 compares one or two sequential receive data characters with the programmed Xon or Xoff-1,2 character value(s). If receive character(s) (RX) match the programmed values, the 2752 will halt transmission (TX) as soon as the current character has completed transmission. When a match occurs, the Xoff (if enabled via IER bit-5) flag will be set and the interrupt output pin will be activated. Following a suspension due to a match of the Xoff character, the 2752 will monitor the receive data stream for a match to the Xon-1,2 character. If a match is found, the 2752 will resume operation and clear the flags (ISR bit-4). Reset initially sets the contents of the Xon/Xoff 8-bit flow control registers to a logic 0. Following reset the user can write any Xon/Xoff value desired for software flow control. Different conditions can be set to detect Xon/Xoff characters (See Table 15) and suspend/resume transmissions. When double 8-bit Xon/Xoff characters are selected, the 2752 compares two consecutive receive characters with two software flow

control 8-bit values (Xon1, Xon2, Xoff1, Xoff2) and controls TX transmissions accordingly. Under the above described flow control mechanisms, flow control characters are not placed (stacked) in the user accessible RX data buffer or FIFO.

In the event that the receive buffer is overfilling and flow control needs to be executed, the 2752 automatically sends an Xoff message (when enabled) via the serial TX output to the remote modem. The 2752 sends the Xoff-1,2 characters two-character-times (= time taken to send two characters at the programmed baud rate) after the receive FIFO crosses the programmed trigger level (for all trigger tables A-D). To clear this condition, the 2752 will transmit the programmed Xon-1,2 characters as soon as receive FIFO is less than one trigger level below the programmed trigger level (for Trigger Tables A, B, and C) or when receive FIFO is less than the trigger level minus the hysteresis value (for Trigger Table D). This hysteresis value is the same as the Auto RTS Hysteresis value in Table 13. Table 6 below explains this when Trigger Table-B (See Table 10) is selected.

TABLE 6: AUTO XON/XOFF (SOFTWARE) FLOW CONTROL

| RX TRIGGER LEVEL | INT PIN ACTIVATION | XOFF CHARACTER(S) SENT (CHARACTERS IN RX FIFO) | XON CHARACTER(S) SENT (CHARACTERS IN RX FIFO) |
|-------------------------|---------------------------|---|--|
| 8 | 8 | 8* | 0 |
| 16 | 16 | 16* | 8 |
| 24 | 24 | 24* | 16 |
| 28 | 28 | 28* | 24 |

* After the trigger level is reached, an xoff character is sent after a short span of time (= time required to send 2 characters); for example, after 2.083ms has elapsed for 9600 baud and 10-bit word length setting.

2.18 SPECIAL CHARACTER DETECT

A special character detect feature is provided to detect an 8-bit character when bit-5 is set in the Enhanced Feature Register (EFR). When this character (Xoff2) is detected, it will be placed in the FIFO along with normal incoming RX data.

The 2752 compares each incoming receive character with Xoff-2 data. If a match exists, the received data will be transferred to FIFO and ISR bit-4 will be set to indicate detection of special character. Although the Internal Register Table shows Xon, Xoff Registers with eight bits of character information, the actual number of bits is dependent on the programmed word length. Line Control Register (LCR) bits 0-1 defines the number of character bits, i.e., either 5 bits, 6 bits, 7 bits, or 8 bits. The word length selected by LCR bits 0-1 also determines the number of bits that will be used for the special character comparison. Bit-0 in the Xon, Xoff Registers corresponds with the LSB bit for the receive character.

2.19 AUTO RS485 HALF-DUPLEX CONTROL

The auto RS485 half-duplex direction control changes the behavior of the transmitter when enabled by FCTR bit-3. It de-asserts RTS# output following the last stop bit of the last character that has been transmitted. This helps in turning around the transceiver to receive the remote station's response. When the host is ready to transmit next polling data packet again, it only has to load data bytes to the transmit FIFO. The transmitter automatically re-asserts RTS# output prior sending the data.

2.20 INFRARED MODE

The 2752 UART includes the infrared encoder and decoder compatible to the IrDA (Infrared Data Association) version 1.0. The IrDA 1.0 standard that stipulates the infrared encoder sends out a 3/16 of a bit wide HIGH-pulse for each "0" bit in the transmit data stream. This signal encoding reduces the on-time of the infrared LED, hence reduces the power consump-

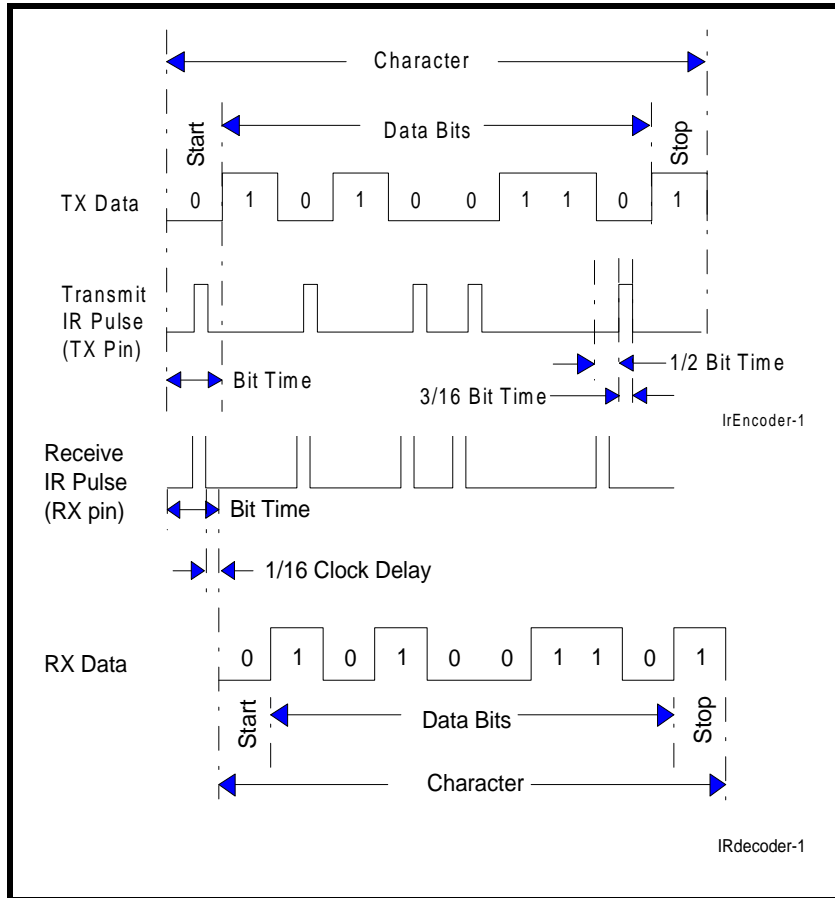
tion. See Figure 11 below.

The infrared encoder and decoder are enabled by setting MCR register bit-6 to a '1'. When the infrared feature is enabled, the transmit data output, TX, idles at logic zero level. Likewise, the RX input assumes an idle level of logic zero from a reset and power up, see Figure 11.

Typically, the wireless infrared decoder receives the

input pulse from the infrared sensing diode on the RX pin. Each time it senses a light pulse, it returns a logic 1 to the data bit stream. However, this is not true with some infrared modules on the market which indicate a logic 0 by a light pulse. So the 2752 has a provision to invert the input polarity to accommodate this. In this case user can enable FCTR bit-2 to invert the input signal.

FIGURE 11. INFRARED TRANSMIT DATA ENCODING AND RECEIVE DATA DECODING



2.21 SLEEP MODE WITH AUTO WAKE-UP

The 2752 supports low voltage system designs, hence, a sleep mode is included to reduce its power consumption when the chip is not actively used. With EFR bit-4 and IER bit-4 of both channels enabled (set to a logic 1), the 2752 DUART enters sleep mode when no interrupt is pending for both channels. The 2752 stops its crystal oscillator to further conserve power in the sleep mode. User can check the XTAL2 pin for no clock output as an indication that the device has entered the sleep mode. The 2752 resumes normal operation by any of the following: a receive data start bit transition (logic 1 to 0), a change of logic state on any of the modem or general purpose input pins: CTS#, DSR#, CD#, RI# or a transmit data byte is loaded to the THR/FIFO by the user. If the 2752 is

awakened by one of the above conditions, it will return to the sleep mode automatically after all interrupting condition have been serviced and cleared. In any case, the sleep mode will not be entered while an interrupt is pending from channel A or B. The 2752 will stay in the sleep mode of operation until it is disabled by setting IER bit-4 to a logic 0.

A word of caution: owing to the starting up delay of the crystal oscillator after waking up from sleep mode, the first few receive characters may be lost. Also, make sure the RX A/B inputs are idling at logic 1 or "marking" condition during sleep mode to avoid receiving a "break" condition upon the restart. This may occur when the external interface transceivers (RS-232, RS-485 or another type) are also put to sleep mode and can not maintain the "marking" con-

PRELIMINARY

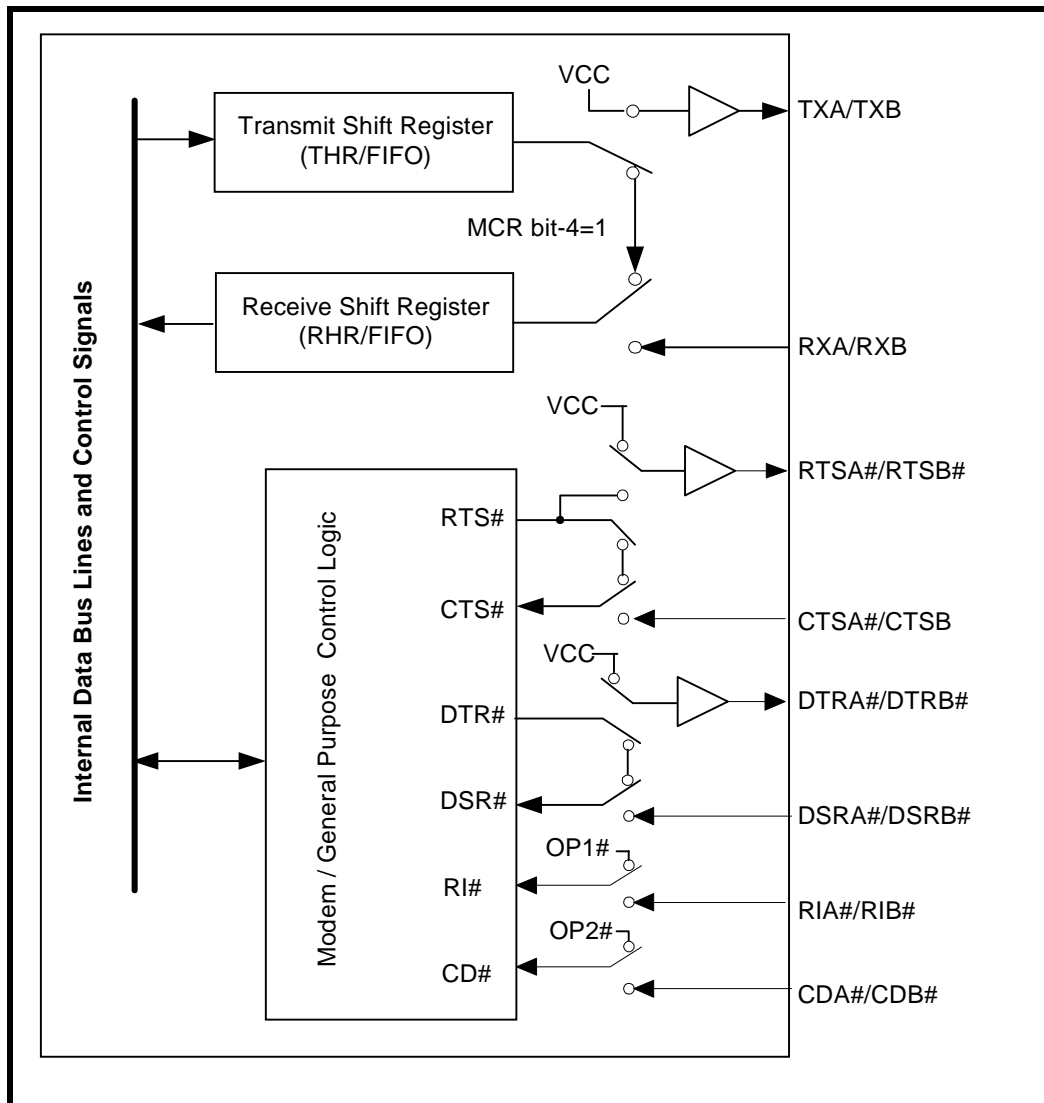
dition. To avoid this, the system design engineer can use a 47k ohm pull-up resistor on the RXA and RXB pins.

2.22 INTERNAL LOOPBACK

The 2752 UART provides an internal loopback capability for system diagnostic purposes. The internal loopback mode is enabled by setting MCR register bit-4 to logic 1. All regular UART functions operate normally. Figure 12 shows how the modem port signals are re-configured. Transmit data from the trans-

mit shift register output is internally routed to the receive shift register input allowing the system to receive the same data that it was sending. The TX pin is held at logic 1 or mark condition while RTS# and DTR# are de-asserted, and CTS#, DSR# CD# and RI# inputs are ignored. Caution: the RX input must be held to a logic 1 during loopback test else upon exiting the loopback test the UART may detect and report a false "break" signal.

FIGURE 12. INTERNAL LOOP BACK IN CHANNEL A AND B



3.0 UART INTERNAL REGISTERS
 Each of the UART channel in the 2752 has its own set of configuration registers selected by address lines

A0, A1 and A2 with CS# and CHSEL selecting the channel. The complete register set is shown in Table 7 and Table 8.

TABLE 7: UART CHANNEL A AND B UART INTERNAL REGISTERS

| A2,A1,A0 ADDRESSES | REGISTER | READ/WRITE | COMMENTS |
|------------------------------------|---|-------------------------|--|
| 16C550 COMPATIBLE REGISTERS | | | |
| 0 0 0 | RHR - Receive Holding Register THR - Transmit Holding Register | Read-only Write-only | LCR[7] = 0 |
| 0 0 0 | DLL - Div Latch Low Byte | Read/Write | LCR[7] = 1, LCR ≠ 0xBF |
| 0 0 1 | DLM - Div Latch High Byte | Read/Write | LCR[7] = 1, LCR ≠ 0xBF |
| 0 1 0 | AFR - Alternate Function Register | Read/Write | LCR[7] = 1, LCR ≠ 0xBF |
| 0 0 0 | DREV - Device Revision Code | Read-only | DLL, DLM = 0x00, LCR[7] = 1, LCR ≠ 0xBF |
| 0 0 1 | DVID - Device Identification Code | Read-only | |
| 0 0 1 | IER - Interrupt Enable Register | Read/Write | LCR[7] = 0 |
| 0 1 0 | ISR - Interrupt Status Register FCR - FIFO Control Register | Read-only Write-only | LCR[7] = 0 |
| 0 1 1 | LCR - Line Control Register | Read/Write | |
| 1 0 0 | MCR - Modem Control Register | Read/Write | LCR[7] = 0 |
| 1 0 1 | LSR - Line Status Register Reserved | Read-only Write-only | LCR[7] = 0 |
| 1 1 0 | MSR - Modem Status Register Reserved | Read-only Write-only | LCR[7] = 0 |
| 1 1 1 | SPR - Scratch Pad Register | Read/Write | LCR[7] = 0, FCTR[6] = 0 |
| 1 1 1 | FLVL - TX/RX FIFO Level Counter Register | Read-only | LCR[7] = 0, FCTR[6] = 1 |
| 1 1 1 | EMSR - Enhanced Mode Select Register | Write-only | |
| ENHANCED REGISTERS | | | |
| 0 0 0 | TRG - TX/RX FIFO Trigger Level Register FC - TX/RX FIFO Level Counter Register | Write-only Read-only | LCR = 0xBF |
| 0 0 1 | FCTR - Feature Control Reg | Read/Write | LCR = 0xBF |
| 0 1 0 | EFR - Enhanced Function Reg | Read/Write | LCR = 0xBF |
| 1 0 0 | Xon-1 - Xoff Character 1 | Read/Write | LCR = 0xBF |
| 1 0 1 | Xon-2 - Xoff Character 2 | Read/Write | LCR = 0xBF |
| 1 1 0 | Xoff-1 - Xon Character 1 | Read/Write | LCR = 0xBF |
| 1 1 1 | Xoff-2 - Xon Character 2 | Read/Write | LCR = 0xBF |

TABLE 8: INTERNAL REGISTERS DESCRIPTION. SHADED BITS ARE ENABLED WHEN EFR BIT-4=1

| ADDRESS A2-A0 | REG NAME | READ/ WRITE | BIT-7 | BIT-6 | BIT-5 | BIT-4 | BIT-3 | BIT-2 | BIT-1 | BIT-0 | COMMENT |
|------------------------------------|----------|-------------|-----------------------|-----------------------|------------------------|-------------------------|-------------------------|---------------------------|----------------------|---------------------|----------------------------|
| 16C550 Compatible Registers | | | | | | | | | | | |
| 0 0 0 | RHR | RD | Bit-7 | Bit-6 | Bit-5 | Bit-4 | Bit-3 | Bit-2 | Bit-1 | Bit-0 | LCR[7] = 0 |
| 0 0 0 | THR | WR | Bit-7 | Bit-6 | Bit-5 | Bit-4 | Bit-3 | Bit-2 | Bit-1 | Bit-0 | |
| 0 0 1 | IER | RD/WR | 0/ CTS Int. Enable | 0/ RTS Int. Enable | 0/ Xoff Int. Enable | 0/ Sleep Mode Enable | Modem Stat. Int. Enable | RX Line Stat. Int. Enable | TX Empty Int. Enable | RX Data Int. Enable | |
| 0 1 0 | ISR | RD | FIFOs Enabled | FIFOs Enabled | 0/ INT Source Bit-5 | 0/ INT Source Bit-4 | INT Source Bit-3 | INT Source Bit-2 | INT Source Bit-1 | INT Source Bit-0 | |
| 0 1 0 | FCR | WR | RXFIFO Trigger | RXFIFO Trigger | 0/ TXFIFO Trigger | 0/ TXFIFO Trigger | DMA Mode Enable | TX FIFO Reset | RX FIFO Reset | FIFOs Enable | |
| 0 1 1 | LCR | RD/WR | Divisor Enable | Set TX Break | Set Parity | Even Parity | Parity Enable | Stop Bits | Word Length Bit-1 | Word Length Bit-0 | |
| 1 0 0 | MCR | RD/WR | 0/ BRG Prescaler | 0/ IR Mode ENable | 0/ XonAny | Internal Lopback Enable | OP2# Output Control | Rsrvd (OP1#) | RTS# Output Control | DTR# Output Control | LCR[7] = 0 |
| 1 0 1 | LSR | RD | RX FIFO Global Error | THR & TSR Empty | THR Empty | RX Break | RX Framing Error | RX Parity Error | RX Over-run Error | RX Data Ready | |
| 1 1 0 | MSR | RD | CD# Input | RI# Input | DSR# Input | CTS# Input | Delta CD# | Delta RI# | Delta DSR# | Delta CTS# | |
| 1 1 1 | SPR | RD/WR | Bit-7 | Bit-6 | Bit-5 | Bit-4 | Bit-3 | Bit-2 | Bit-1 | Bit-0 | LCR[7] = 0 FCTR bit-6=0 |
| 1 1 1 | EMSR | WR | Rsvd | Rsvd | Auto RTS Hyst. bit-3 | Auto RTS Hyst. bit-2 | Rsvd | Rsvd | Rx/Tx FIFO Count | Rx/Tx FIFO Count | LCR[7] = 0 FCTR bit-6=1 |
| 1 1 1 | FLVL | RD | Bit-7 | Bit-6 | Bit-5 | Bit-4 | Bit-3 | Bit-2 | Bit-1 | Bit-0 | |

TABLE 8: INTERNAL REGISTERS DESCRIPTION. SHADED BITS ARE ENABLED WHEN EFR BIT-4=1

| ADDRESS A2-A0 | REG NAME | READ/ WRITE | BIT-7 | BIT-6 | BIT-5 | BIT-4 | BIT-3 | BIT-2 | BIT-1 | BIT-0 | COMMENT |
|------------------------------------|----------|-------------|-----------------|-----------------|---------------------|---|------------------------------|--------------------------|--------------------------|--------------------------|--|
| Baud Rate Generator Divisor | | | | | | | | | | | |
| 0 0 0 | DLL | RD/WR | Bit-7 | Bit-6 | Bit-5 | Bit-4 | Bit-3 | Bit-2 | Bit-1 | Bit-0 | LCR[7] = 1 LCR ≠ 0xBF |
| 0 0 1 | DLM | RD/WR | Bit-7 | Bit-6 | Bit-5 | Bit-4 | Bit-3 | Bit-2 | Bit-1 | Bit-0 | |
| 0 1 0 | AFR | RD/WR | Rsvd | Rsvd | Rsvd | Rsvd | Rsvd | RXRDY# Select | Baudout# Select | Concurrent Write | LCR[7] = 1 LCR ≠ 0xBF |
| 0 0 0 | DREV | RD | Bit-7 | Bit-6 | Bit-5 | Bit-4 | Bit-3 | Bit-2 | Bit-1 | Bit-0 | LCR[7] = 1 LCR ≠ 0xBF DLL=0x00 DLM=0x00 |
| 0 0 1 | DVID | RD | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | |
| Enhanced Registers | | | | | | | | | | | |
| 0 0 0 | TRG | WR | Bit-7 | Bit-6 | Bit-5 | Bit-4 | Bit-3 | Bit-2 | Bit-1 | Bit-0 | LCR=0xBF |
| 0 0 0 | FC | RD | Bit-7 | Bit-6 | Bit-5 | Bit-4 | Bit-3 | Bit-2 | Bit-1 | Bit-0 | |
| 0 0 1 | FCTR | RD/WR | RX/TX Mode | SCPAD Swap | Trig Table Bit-1 | Trig Table Bit-0 | Auto RS485 Direction Control | RX IR Input Inv. | Auto RTS Hyst Bit-1 | Auto RTS Hyst Bit-0 | |
| 0 1 0 | EFR | RD/WR | Auto CTS Enable | Auto RTS Enable | Special Char Select | Enable IER [7:4], ISR [5:4], FCR[5:4], MCR[7:5] | Software Flow Cntl Bit-3 | Software Flow Cntl Bit-2 | Software Flow Cntl Bit-1 | Software Flow Cntl Bit-0 | |
| 1 0 0 | XON1 | RD/WR | Bit-7 | Bit-6 | Bit-5 | Bit-4 | Bit-3 | Bit-2 | Bit-1 | Bit-0 | |
| 1 0 1 | XON2 | RD/WR | Bit-7 | Bit-6 | Bit-5 | Bit-4 | Bit-3 | Bit-2 | Bit-1 | Bit-0 | |
| 1 1 0 | XOFF1 | RD/WR | Bit-7 | Bit-6 | Bit-5 | Bit-4 | Bit-3 | Bit-2 | Bit-1 | Bit-0 | |
| 1 1 1 | XOFF2 | RD/WR | Bit-7 | Bit-6 | Bit-5 | Bit-4 | Bit-3 | Bit-2 | Bit-1 | Bit-0 | |

4.0 INTERNAL REGISTER DESCRIPTIONS

4.1 RECEIVE HOLDING REGISTER (RHR) - READ-ONLY

See “Receiver” on page 12..

4.2 TRANSMIT HOLDING REGISTER (THR) - WRITE-ONLY

See “Transmitter” on page 11..

4.3 BAUD RATE GENERATOR DIVISORS (DLL AND DLM) - READ/WRITE

The Baud Rate Generator (BRG) is a 16-bit counter that generates the data rate for the transmitter. The rate is programmed through registers DLL and DLM which are only accessible when LCR bit-7 is set to ‘1’. See “Programmable Baud Rate Generator” on page 9. for more details.

4.4 INTERRUPT ENABLE REGISTER (IER) - READ/WRITE

The Interrupt Enable Register (IER) masks the interrupts from receive data ready, transmit empty, line status and modem status registers. These interrupts are reported in the Interrupt Status Register (ISR).

4.4.1 IER versus Receive FIFO Interrupt Mode Operation

When the receive FIFO (FCR BIT-0 = 1) and receive interrupts (IER BIT-0 = 1) are enabled, the RHR interrupts (see ISR bits 2 and 3) status will reflect the following:

- A. The receive data available interrupts are issued to the host when the FIFO has reached the programmed trigger level. It will be cleared when the FIFO drops below the programmed trigger level.

- B. FIFO level will be reflected in the ISR register when the FIFO trigger level is reached. Both the ISR register status bit and the interrupt will be cleared when the FIFO drops below the trigger level.
- C. The receive data ready bit (LSR BIT-0) is set as soon as a character is transferred from the shift register to the receive FIFO. It is reset when the FIFO is empty.

4.4.2 IER versus Receive/Transmit FIFO Polled Mode Operation

When FCR BIT-0 equals a logic 1 for FIFO enable; resetting IER bits 0-3 enables the XR16L2752 in the FIFO polled mode of operation. Since the receiver and transmitter have separate bits in the LSR either or both can be used in the polled mode by selecting respective transmit or receive control bit(s).

- A. LSR BIT-0 indicates there is data in RHR or RX FIFO.
- B. LSR BIT-1 indicates an overrun error has occurred and that data in the FIFO may not be valid.
- C. LSR BIT 2-4 provides the type of receive data errors encountered for the data byte in RHR, if any.
- D. LSR BIT-5 indicates THR is empty.
- E. LSR BIT-6 indicates when both the transmit FIFO and TSR are empty.
- F. LSR BIT-7 indicates a data error in at least one character in the RX FIFO.

IER[0]: RHR Interrupt Enable

The receive data ready interrupt will be issued when RHR has a data character in the non-FIFO mode or when the receive FIFO has reached the programmed trigger level in the FIFO mode.

- Logic 0 = Disable the receive data ready interrupt (default).
- Logic 1 = Enable the receiver data ready interrupt.

IER[1]: THR Interrupt Enable

This bit enables the Transmit Ready interrupt which is issued whenever the THR becomes empty in the non-FIFO mode or when data in the FIFO falls below the programmed trigger level in the FIFO mode. If the THR is empty when this bit is enabled, an interrupt will be generated.

- Logic 0 = Disable Transmit Ready interrupt (default).
- Logic 1 = Enable Transmit Ready interrupt.

IER[2]: Receive Line Status Interrupt Enable

If any of the LSR register bits 1, 2, 3 or 4 is a logic 1, it will generate an interrupt to inform the host controller about the error status of the current data byte in FIFO. LSR bits 1-4 generate an interrupt immediately when the character has been received.

- Logic 0 = Disable the receiver line status interrupt (default).
- Logic 1 = Enable the receiver line status interrupt.

IER[3]: Modem Status Interrupt Enable

- Logic 0 = Disable the modem status register interrupt (default).
- Logic 1 = Enable the modem status register interrupt.

IER[4]: Sleep Mode Enable (requires EFR bit-4 = 1)

- Logic 0 = Disable Sleep Mode (default).
- Logic 1 = Enable Sleep Mode. See Sleep Mode section for further details.

IER[5]: Xoff Interrupt Enable (requires EFR bit-4=1)

- Logic 0 = Disable the software flow control, receive Xoff interrupt. (default)
- Logic 1 = Enable the software flow control, receive Xoff interrupt. See Software Flow Control section for details.

IER[6]: RTS# Output Interrupt Enable (requires EFR bit-4=1)

- Logic 0 = Disable the RTS# interrupt (default).
- Logic 1 = Enable the RTS# interrupt. The UART issues an interrupt when the RTS# pin makes a transition from low to high.

IER[7]: CTS# Input Interrupt Enable (requires EFR bit-4=1)

- Logic 0 = Disable the CTS# interrupt (default).
- Logic 1 = Enable the CTS# interrupt. The UART issues an interrupt when CTS# pin makes a transition from low to high.

4.5 INTERRUPT STATUS REGISTER (ISR) - READ-ONLY

The UART provides multiple levels of prioritized interrupts to minimize external software interaction. The Interrupt Status Register (ISR) provides the user with six interrupt status bits. Performing a read cycle on the ISR will give the user the current highest pending interrupt level to be serviced, others are queued up to be serviced next. No other interrupts are acknowledged until the pending interrupt is serviced. The Interrupt Source Table, Table 9, shows the data values (bit 0-5) for the interrupt priority levels and the interrupt sources associated with each of these interrupt levels.

4.5.1 Interrupt Generation:

- LSR is by any of the LSR bits 1, 2, 3 and 4.
- RXRDY is by RX trigger level.
- RXRDY Time-out is by a 4-char plus 12 bits delay timer.
- TXRDY is by TX trigger level or TX FIFO empty (or transmitter empty in auto RS-485 control).
- MSR is by any of the MSR bits 0, 1, 2 and 3.
- Receive Xoff/Special character is by detection of a Xoff or Special character.

- CTS# is when its transmitter toggles the input pin (from low to high) during auto CTS flow control enabled by EFR bit-7.
- RTS# is when its receiver toggles the output pin (from low to high) during auto RTS flow control enabled by EFR bit-6.

4.5.2 Interrupt Clearing:

- LSR interrupt is cleared by a read to the LSR register (but flags and tags not cleared until character(s) that generated the interrupt(s) has been emptied or cleared from FIFO).
- RXRDY interrupt is cleared by reading data until FIFO falls below the trigger level.
- RXRDY Time-out interrupt is cleared by reading RHR.
- TXRDY interrupt is cleared by a read to the ISR register or writing to THR.
- MSR interrupt is cleared by a read to the MSR register.
- Xoff or Special character interrupt is cleared by a read to ISR.
- RTS# and CTS# flow control interrupts are cleared by a read to the MSR register.

TABLE 9: INTERRUPT SOURCE AND PRIORITY LEVEL

| PRIORITY LEVEL | ISR REGISTER STATUS BITS | | | | | | SOURCE OF INTERRUPT |
|----------------|--------------------------|-------|-------|-------|-------|-------|--|
| | BIT-5 | BIT-4 | BIT-3 | BIT-2 | BIT-1 | BIT-0 | |
| 1 | 0 | 0 | 0 | 1 | 1 | 0 | LSR (Receiver Line Status Register) |
| 2 | 0 | 0 | 1 | 1 | 0 | 0 | RXRDY (Receive Data Time-out) |
| 3 | 0 | 0 | 0 | 1 | 0 | 0 | RXRDY (Received Data Ready) |
| 4 | 0 | 0 | 0 | 0 | 1 | 0 | TXRDY (Transmit Ready) |
| 5 | 0 | 0 | 0 | 0 | 0 | 0 | MSR (Modem Status Register) |
| 6 | 0 | 1 | 0 | 0 | 0 | 0 | RXRDY (Received Xoff or Special character) |
| 7 | 1 | 0 | 0 | 0 | 0 | 0 | CTS#, RTS# change of state |
| - | 0 | 0 | 0 | 0 | 0 | 1 | None (default) |

ISR[0]: Interrupt Status

- Logic 0 = An interrupt is pending and the ISR contents may be used as a pointer to the appropriate interrupt service routine.
- Logic 1 = No interrupt pending (default condition).

ISR[3:1]: Interrupt Status

These bits indicate the source for a pending interrupt at interrupt priority levels (See Interrupt Source

Table 9).

ISR[5:4]: Interrupt Status

These bits are enabled when EFR bit-4 is set to a logic 1. ISR bit-4 indicates that the receiver detected a data match of the Xoff character(s). Note that once set to a logic 1, the ISR bit-4 will stay a logic 1 until a Xon character is received. ISR bit-5 indicates that CTS# or RTS# has changed state.

ISR[7:6]: FIFO Enable Status

These bits are set to a logic 0 when the FIFOs are disabled. They are set to a logic 1 when the FIFOs are enabled.

4.6 FIFO CONTROL REGISTER (FCR) - WRITE-ONLY

This register is used to enable the FIFOs, clear the FIFOs, set the transmit/receive FIFO trigger levels, and select the DMA mode. The DMA, and FIFO modes are defined as follows:

FCR[0]: TX and RX FIFO Enable

- Logic 0 = Disable the transmit and receive FIFO (default).
- Logic 1 = Enable the transmit and receive FIFOs. This bit must be set to logic 1 when other FCR bits are written or they will not be programmed.

FCR[1]: RX FIFO Reset

This bit is only active when FCR bit-0 is a '1'.

- Logic 0 = No receive FIFO reset (default)
- Logic 1 = Reset the receive FIFO pointers and FIFO level counter logic (the receive shift register is not cleared or altered). This bit will return to a logic 0 after resetting the FIFO.

FCR[2]: TX FIFO Reset

This bit is only active when FCR bit-0 is a '1'.

- Logic 0 = No transmit FIFO reset (default).
- Logic 1 = Reset the transmit FIFO pointers and FIFO level counter logic (the transmit shift register is not cleared or altered). This bit will return to a logic 0 after resetting the FIFO.

FCR[3]: DMA Mode Select

Controls the behavior of the TXRDY# and RXRDY# pins. See DMA operation section for details.

- Logic 0 = Normal Operation (default).
- Logic 1 = DMA Mode.

FCR[5:4]: Transmit FIFO Trigger Select

(logic 0 = default, TX trigger level = one)

These 2 bits set the trigger level for the transmit FIFO. The UART will issue a transmit interrupt when the number of characters in the FIFO falls below the selected trigger level, or when it gets empty in case that the FIFO did not get filled over the trigger level on last re-load. Table 10 below shows the selections. EFR bit-4 must be set to '1' before these bits can be accessed. Note that the receiver and the transmitter cannot use different trigger tables. Whichever selection is made last applies to both the RX and TX side.

FCR[7:6]: Receive FIFO Trigger Select

(logic 0 = default, RX trigger level =1)

The FCTR Bits 5-4 are associated with these 2 bits. These 2 bits are used to set the trigger level for the receive FIFO. The UART will issue a receive interrupt when the number of the characters in the FIFO crosses the trigger level. Table 10 shows the complete selections. Note that the receiver and the transmitter cannot use different trigger tables. Whichever selection is made last applies to both the RX and TX side

TABLE 10: TRANSMIT AND RECEIVE FIFO TRIGGER LEVEL SELECTION

| FCTR BIT-5 | FCTR BIT-4 | FCR BIT-7 | FCR BIT-6 | FCR BIT-5 | FCR BIT-4 | RECEIVE TRIGGER LEVEL | TRANSMIT TRIGGER LEVEL | COMPATIBILITY |
|------------|------------|------------------|------------------|------------------|------------------|---|---|--|
| 0 | 0 | 0 0 1 1 | 0 1 0 1 | 0 | 0 | 1 (default) 4 8 14 | 1 (default) | Table-A. 16C550, 16C2550, 16C2552, 16C554, 16C580 compatible. |
| 0 | 1 | 0 0 1 1 | 0 1 0 1 | 0 0 1 1 | 0 1 0 1 | 8 16 24 28 | 16 8 24 30 | Table-B. 16C650A compatible. |
| 1 | 0 | 0 0 1 1 | 0 1 0 1 | 0 0 1 1 | 0 1 0 1 | 8 16 56 60 | 8 16 32 56 | Table-C. 16C654 compatible. |
| 1 | 1 | X | X | X | X | Programmable via TRG register. FCTR[7] = 0. | Programmable via TRG register. FCTR[7] = 1. | Table-D. 16C850, 16L2750, 16C2850, 16C2852, 16C854, 16C864, 16C872 compatible. |

4.7 LINE CONTROL REGISTER (LCR) - READ/WRITE

The Line Control Register is used to specify the asynchronous data communication format. The word or character length, the number of stop bits, and the parity are selected by writing the appropriate bits in this register.

LCR[1-0]: TX and RX Word Length Select

These two bits specify the word length to be transmitted or received.

| BIT-1 | BIT-0 | WORD LENGTH |
|-------|-------|-------------|
| 0 | 0 | 5 (default) |
| 0 | 1 | 6 |
| 1 | 0 | 7 |
| 1 | 1 | 8 |

LCR[2]: TX and RX Stop-bit Length Select

The length of stop bit is specified by this bit in conjunction with the programmed word length.

| BIT-2 | WORD LENGTH | STOP BIT LENGTH (BIT TIME(S)) |
|-------|-------------|-------------------------------|
| 0 | 5,6,7,8 | 1 (default) |
| 1 | 5 | 1-1/2 |
| 1 | 6,7,8 | 2 |

LCR[3]: TX and RX Parity Select

Parity or no parity can be selected via this bit. The parity bit is a simple way used in communications for data integrity check. See Table 11 for parity selection summary below.

- Logic 0 = No parity.
- Logic 1 = A parity bit is generated during the transmission while the receiver checks for parity error of the data character received.

LCR[4]: TX and RX Parity Select

If the parity bit is enabled with LCR bit-3 set to a logic 1, LCR BIT-4 selects the even or odd parity format.

- Logic 0 = ODD Parity is generated by forcing an odd number of logic 1's in the transmitted character. The receiver must be programmed to check the same format (default).
- Logic 1 = EVEN Parity is generated by forcing an even number of logic 1's in the transmitted character. The receiver must be programmed to check the same format.

LCR[5]: TX and RX Parity Select

If the parity bit is enabled, LCR BIT-5 selects the forced parity format.

- LCR BIT-5 = logic 0, parity is not forced (default).
- LCR BIT-5 = logic 1 and LCR BIT-4 = logic 0, parity bit is forced to a logical 1 for the transmit and receive data.

TABLE 11: PARITY SELECTION

| LCR BIT-5 | LCR BIT-4 | LCR BIT-3 | PARITY SELECTION |
|-----------|-----------|-----------|-----------------------------|
| X | X | 0 | No parity |
| 0 | 0 | 1 | Odd parity |
| 0 | 1 | 1 | Even parity |
| 1 | 0 | 1 | Force parity to mark, "1" |
| 1 | 1 | 1 | Forced parity to space, "0" |

LCR[6]: Transmit Break Enable

When enabled, the Break control bit causes a break condition to be transmitted (the TX output is forced to a "space", logic 0, state). This condition remains, until disabled by setting LCR bit-6 to a logic 0.

- Logic 0 = No TX break condition (default).
- Logic 1 = Forces the transmitter output (TX) to a "space", logic 0, for alerting the remote receiver of a line break condition.

LCR[7]: Baud Rate Divisors Enable

Baud rate generator divisor (DLL/DLM) enable.

- Logic 0 = Data registers are selected. (default)
- Logic 1 = Divisor latch registers are selected.

4.8 ALTERNATE FUNCTION REGISTER (AFR) - READ/WRITE

This register is used to select specific modes of MF# operation and to allow both UART register sets to be written concurrently.

AFR[0]: Concurrent Write Mode

When this bit is set, the CPU can write concurrently to the same register in both UARTs. This function is intended to reduce the dual UART initialization time. It can be used by the CPU when both channels are initialized to the same state. The external CPU can set or clear this bit by accessing either register set. When this bit is set, the channel select pin still selects the channel to be accessed during read operations. The user should ensure that LCR Bit-7 of both channels are in the same state before executing a concurrent write to the registers at address 0, 1, or 2.

- Logic 0 = No concurrent write (default).
- Logic 1 = Register set A and B are written concurrently with a single external CPU I/O write operation.

AFR[2:1]: MF# Output Select

These bits select a signal function for output on the MF# A/B pins. These signal function are described as: OP2#, BAUDOUT#, or RXRDY#. Only one signal function can be selected at a time.

| BIT-2 | BIT-1 | MF# FUNCTION |
|-------|-------|----------------|
| 0 | 0 | OP2# (default) |
| 0 | 1 | BAUDOUT# |
| 1 | 0 | RXRDY# |
| 1 | 1 | Reserved |

AFR[7:3]: Reserved

All are initialized to logic 0.

4.9 MODEM CONTROL REGISTER (MCR) OR GENERAL PURPOSE OUTPUTS CONTROL - READ/WRITE

The MCR register is used for controlling the serial/modem interface signals or general purpose inputs/outputs.

MCR[0]: DTR# Output

The DTR# pin is a modem control output. If the modem interface is not used, this output may be used as a general purpose output.

- Logic 0 = Force DTR# output to a logic 1 (default).
- Logic 1 = Force DTR# output to a logic 0.

MCR[1]: RTS# Output

The RTS# pin is a modem control output and may be used for automatic hardware flow control by enabled by EFR bit-6. If the modem interface is not used, this output may be used as a general purpose output.

- Logic 0 = Force RTS# output to a logic 1 (default).
- Logic 1 = Force RTS# output to a logic 0.

MCR[2]: Reserved

OP1# is not available as an output pin on the 2752. But it is available for use during Internal Loopback Mode. In the Loopback Mode, this bit is used to write the state of the modem RI# interface signal.

MCR[3]: OP2# Output / INT Output Enable

OP2# is available as an output pin on the 2752 when AFR[2:1] = '00'. In the Loopback Mode, MCR[3] is used to write the state of the modem CD# interface signal. Also see pin descriptions for MF# pins.

- Logic 0 = Forces OP2# output to a logic 1 (default).
- Logic 1 = Forces OP2# output to a logic 0.

MCR[4]: Internal Loopback Enable

- Logic 0 = Disable loopback mode (default).
- Logic 1 = Enable local loopback mode, see loopback section and Figure 12.

MCR[5]: Xon-Any Enable

- Logic 0 = Disable Xon-Any function (for 16C550 compatibility, default).
- Logic 1 = Enable Xon-Any function. In this mode, any RX character received will resume transmit operation. The RX character will be loaded into the RX FIFO, unless the RX character is an Xon or Xoff character and the 2752 is programmed to use the Xon/Xoff flow control.

MCR[6]: Infrared Encoder/Decoder Enable

- Logic 0 = Enable the standard modem receive and transmit input/output interface. (Default)
- Logic 1 = Enable infrared IrDA receive and transmit inputs/outputs. The TX/RX output/input are routed to the infrared encoder/decoder. The data input and output levels conform to the IrDA infrared interface requirement. While in this mode, the infrared TX output will be a logic 0 during idle data conditions.

MCR[7]: Clock Prescaler Select

- Logic 0 = Divide by one. The input clock from the crystal or external clock is fed directly to the Programmable Baud Rate Generator without further modification, i.e., divide by one (default).
- Logic 1 = Divide by four. The prescaler divides the input clock from the crystal or external clock by four and feeds it to the Programmable Baud Rate Generator, hence, data rates become one fourth.

4.10 LINE STATUS REGISTER (LSR) - READ ONLY

This register provides the status of data transfers between the UART and the host.

LSR[0]: Receive Data Ready Indicator

- Logic 0 = No data in receive holding register or FIFO (default).
- Logic 1 = Data has been received and is saved in the receive holding register or FIFO.

LSR[1]: Receiver Overrun Flag

- Logic 0 = No overrun error. (default)
- Logic 1 = Overrun error. A data overrun error condition occurred in the receive shift register. This happens when additional data arrives while the FIFO is full. In this case the previous data in the receive shift register is overwritten. Note that under this condition the data byte in the receive shift register is not transferred into the FIFO, therefore the data in the FIFO is not corrupted by the error.

LSR[2]: Receive Data Parity Error Flag

- Logic 0 = No parity error (default).
- Logic 1 = Parity error. The receive character in RHR does not have correct parity information and is suspect. This error is associated with the character available for reading in RHR.

LSR[3]: Receive Data Framing Error Flag

- Logic 0 = No framing error (default).
- Logic 1 = Framing error. The receive character did not have a valid stop bit(s). This error is associated with the character available for reading in RHR.

LSR[4]: Receive Break Flag

- Logic 0 = No break condition (default).
- Logic 1 = The receiver received a break signal (RX was a logic 0 for at least one character frame time). In the FIFO mode, only one break character is loaded into the FIFO. The break indication remains until the RX input returns to the idle condition, "mark" or logic 1.

LSR[5]: Transmit Holding Register Empty Flag

This bit is the Transmit Holding Register Empty indicator. The THR bit is set to a logic 1 when the last data byte is transferred from the transmit holding register to the transmit shift register. The bit is reset to logic 0 concurrently with the data loading to the transmit holding register by the host. In the FIFO mode this bit is set when the transmit FIFO is empty, it is cleared when the transmit FIFO contains at least 1 byte.

LSR[6]: THR and TSR Empty Flag

This bit is set to a logic 1 whenever the transmitter goes idle. It is set to logic 0 whenever either the THR or TSR contains a data character. In the FIFO mode this bit is set to a logic 1 whenever the transmit FIFO and transmit shift register are both empty.

LSR[7]: Receive FIFO Data Error Flag

- Logic 0 = No FIFO error (default).
- Logic 1 = A global indicator for the sum of all error bits in the RX FIFO. At least one parity error, framing error or break indication is in the FIFO data. This bit clears when there is no more error(s) in any of the bytes in the RX FIFO.

4.11 MODEM STATUS REGISTER (MSR) - READ ONLY

This register provides the current state of the modem interface input signals. Lower four bits of this register are used to indicate the changed information. These bits are set to a logic 1 whenever a signal from the modem changes state. These bits may be used as general purpose inputs when they are not used with modem signals.

MSR[0]: Delta CTS# Input Flag

- Logic 0 = No change on CTS# input (default).
- Logic 1 = The CTS# input has changed state since the last time it was monitored. A modem status interrupt will be generated if MSR interrupt is enabled (IER bit-3).

MSR[1]: Delta DSR# Input Flag

- Logic 0 = No change on DSR# input (default).
- Logic 1 = The DSR# input has changed state since the last time it was monitored. A modem status interrupt will be generated if MSR interrupt is enabled (IER bit-3).

MSR[2]: Delta RI# Input Flag

- Logic 0 = No change on RI# input (default).
- Logic 1 = The RI# input has changed from a logic 0 to a logic 1, ending of the ringing signal. A modem status interrupt will be generated if MSR interrupt is enabled (IER bit-3).

MSR[3]: Delta CD# Input Flag

- Logic 0 = No change on CD# input (default).
- Logic 1 = Indicates that the CD# input has changed state since the last time it was monitored. A modem status interrupt will be generated if MSR interrupt is enabled (IER bit-3).

MSR[4]: CTS Input Status

CTS# pin may function as automatic hardware flow control signal input if it is enabled and selected by Auto CTS (EFR bit-7). Auto CTS flow control allows starting and stopping of local data transmissions based on the modem CTS# signal. A logic 1 on the CTS# pin will stop UART transmitter as soon as the current character has finished transmission, and a logic 0 will resume data transmission. Normally MSR bit-4 bit is the compliment of the CTS# input. However in the loopback mode, this bit is equivalent to the

RTS# bit in the MCR register. The CTS# input may be used as a general purpose input when the modem interface is not used.

MSR[5]: DSR Input Status

DSR# (active high, logical 1). Normally this bit is the compliment of the DSR# input. In the loopback mode, this bit is equivalent to the DTR# bit in the MCR register. The DSR# input may be used as a general purpose input when the modem interface is not used.

MSR[6]: RI Input Status

RI# (active high, logical 1). Normally this bit is the compliment of the RI# input. In the loopback mode this bit is equivalent to bit-2 in the MCR register. The RI# input may be used as a general purpose input when the modem interface is not used.

MSR[7]: CD Input Status

CD# (active high, logical 1). Normally this bit is the compliment of the CD# input. In the loopback mode this bit is equivalent to bit-3 in the MCR register. The CD# input may be used as a general purpose input when the modem interface is not used.

4.12 SCRATCH PAD REGISTER (SPR) - READ/WRITE

This is a 8-bit general purpose register for the user to store temporary data. The content of this register is preserved during sleep mode but becomes 0xFF (default) after a reset or a power off-on cycle.

4.13 ENHANCED MODE SELECT REGISTER (EMSR)

This register replaces SPR (during a Write) and is accessible only when FCTR[6] = 1.

EMSR[1:0]: Receive/Transmit FIFO Count (Write-Only)

When Scratchpad Swap (FCTR[6]) is asserted, EMSR bits 1-0 controls what mode the FIFO Level Counter is operating in.

TABLE 12: SCRATCHPAD SWAP SELECTION

| FCTR[6] | EMSR[1] | EMSR[0] | Scratchpad is |
|---------|---------|---------|-----------------------------------|
| 0 | X | X | Scratchpad |
| 1 | 0 | 0 | RX FIFO Counter Mode |
| 1 | 0 | 1 | TX FIFO Counter Mode |
| 1 | 1 | 0 | RX FIFO Counter Mode |
| 1 | 1 | 1 | Alternate RX/TX FIFO Counter Mode |

During Alternate RX/TX FIFO Counter Mode, the first value read after EMSR bits 1-0 have been asserted will always be the RX FIFO Counter. The second value read will correspond with the TX FIFO Counter. The next value will be the RX FIFO Counter again, then the TX FIFO Counter and so on and so forth.

EMSR[3:2]: Reserved

EMSR[5:4]: Extended RTS Hysteresis

TABLE 13: AUTO RTS HYSTERESIS

| EMSR BIT-5 | EMSR BIT-4 | FCTR BIT-1 | FCTR BIT-0 | RTS# HYSTERESIS (CHARACTERS) |
|------------|------------|------------|------------|------------------------------|
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | ±4 |
| 0 | 0 | 1 | 0 | ±6 |
| 0 | 0 | 1 | 1 | ±8 |
| 0 | 1 | 0 | 0 | ±8 |
| 0 | 1 | 0 | 1 | ±16 |
| 0 | 1 | 1 | 0 | ±24 |
| 0 | 1 | 1 | 1 | ±32 |
| 1 | 0 | 0 | 0 | ±40 |
| 1 | 0 | 0 | 1 | ±44 |
| 1 | 0 | 1 | 0 | ±48 |
| 1 | 0 | 1 | 1 | ±52 |
| 1 | 1 | 0 | 0 | ±12 |
| 1 | 1 | 0 | 1 | ±20 |
| 1 | 1 | 1 | 0 | ±28 |
| 1 | 1 | 1 | 1 | ±36 |

EMSR[7:6]: Reserved

4.14 FIFO LEVEL REGISTER (FLVL) - READ-ONLY

The FIFO Level Register replaces the Scratchpad Register (during a Read) when FCTR[6] = 1. Note that this is not identical to the FIFO Data Count Register which can be accessed when LCR = 0xBF.

FLVL[7:0]: FIFO Level Register

This register provides the FIFO counter level for the RX FIFO or the TX FIFO or both depending on EMSR[1:0]. See Table 12 for details.

4.15 BAUD RATE GENERATOR REGISTERS (DLL AND DLM) - READ/WRITE

The concatenation of the contents of DLM and DLL gives the 16-bit divisor value which is used to calculate the baud rate:

- Baud Rate = (Clock Frequency / 16) / Divisor

See MCR bit-7 and the baud rate table also.

4.16 DEVICE IDENTIFICATION REGISTER (DVID) - READ ONLY

This register contains the device ID (0x0A for XR16C2752). Prior to reading this register, DLL and DLM should be set to 0x00.

4.17 DEVICE REVISION REGISTER (DREV) - READ ONLY

This register contains the device revision information. For example, 0x01 means revision A. Prior to reading this register, DLL and DLM should be set to 0x00.

4.18 TRIGGER LEVEL / FIFO DATA COUNT REGISTER (TRG) - WRITE-ONLY

User Programmable Transmit/Receive Trigger Level Register.

TRG[7:0]: Trigger Level Register

These bits are used to program desired trigger levels when trigger Table-D is selected. FCTR bit-7 selects between programming the RX Trigger Level (a logic 0) and the TX Trigger Level (a logic 1).

4.19 FIFO DATA COUNT REGISTER (FC) - READ-ONLY

This register is accessible when LCR = 0xBF. Note that this register is not identical to the FIFO Level Register which is located in the general register set when FCTR bit-6 = 1.

FC[7:0]: FIFO Data Count Register

Transmit/Receive FIFO Count. Number of characters in Transmit (FCTR[7] = 1) or Receive FIFO (FCTR[7] = 0) can be read via this register.

4.20 FEATURE CONTROL REGISTER (FCTR) - READ/WRITE

This register controls the XR16L2752 new functions.

FCTR[1:0]: RTS Hysteresis

User selectable RTS# hysteresis levels for hardware flow control application. After reset, these bits are set to "0" to select the next trigger level for hardware flow control. See Table 13 for more details.

FCTR[2]: IrDa RX Inversion

- Logic 0 = Select RX input as encoded IrDa data.
- Logic 1 = Select RX input as active high encoded IrDa data.

FCTR[3]: Auto RS-485 Direction Control

- Logic 0 = Standard ST16C550 mode. Transmitter generates an interrupt when transmit holding register becomes empty and transmit shift register is shifting data out.
- Logic 1 = Enable Auto RS485 Direction Control function. The direction control signal, RTS# pin, changes its output logic state from low to high one bit time after the last stop bit of the last character is shifted out. Also, the Transmit interrupt generation is delayed until the transmitter shift register becomes empty. The RTS# output pin will automatically return to a logic low when a data byte is loaded into the TX FIFO.

FCTR[5:4]: Transmit/Receive Trigger Table Select

See Table 10 .

TABLE 14: TRIGGER TABLE SELECT

| FCTR BIT-5 | FCTR BIT-4 | TABLE |
|-------------------|-------------------|-----------------|
| 0 | 0 | Table-A (TX/RX) |
| 0 | 1 | Table-B (TX/RX) |
| 1 | 0 | Table-C (TX/RX) |
| 1 | 1 | Table-D (TX/RX) |

FCTR[6]: Scratchpad Swap

- Logic 0 = Scratch Pad register is selected as general read and write register. ST16C550 compatible mode.
- Logic 1 = FIFO Count register (Read-Only), Enhanced Mode Select Register (Write-Only). Number of characters in transmit or receive FIFO can be read via scratch pad register when this bit is set. Enhanced Mode Select Register is selected when it is written into.

FCTR[7]: Programmable Trigger Register Select

- Logic 0 = Registers TRG and FC selected for RX.
- Logic 1 = Registers TRG and FC selected for TX.

4.21 ENHANCED FEATURE REGISTER (EFR)

Enhanced features are enabled or disabled using this register. Bit 0-3 provide single or dual consecutive character software flow control selection (see Table 15). When the Xon1 and Xon2 and Xoff1 and Xoff2 modes are selected, the double 8-bit words are concatenated into two sequential characters. Caution: note that whenever changing the TX or RX flow control bits, always reset all bits back to logic 0 (disable) before programming a new setting.

EFR[3:0]: Software Flow Control Select

Single character and dual sequential characters software flow control is supported. Combinations of software flow control can be selected by programming these bits.

TABLE 15: SOFTWARE FLOW CONTROL FUNCTIONS

| EFR BIT-3 CONT-3 | EFR BIT-2 CONT-2 | EFR BIT-1 CONT-1 | EFR BIT-0 CONT-0 | TRANSMIT AND RECEIVE SOFTWARE FLOW CONTROL |
|---------------------|---------------------|---------------------|---------------------|--|
| 0 | 0 | 0 | 0 | No TX and RX flow control (default and reset) |
| 0 | 0 | X | X | No transmit flow control |
| 1 | 0 | X | X | Transmit Xon1, Xoff1 |
| 0 | 1 | X | X | Transmit Xon2, Xoff2 |
| 1 | 1 | X | X | Transmit Xon1 and Xon2, Xoff1 and Xoff2 |
| X | X | 0 | 0 | No receive flow control |
| X | X | 1 | 0 | Receiver compares Xon1, Xoff1 |
| X | X | 0 | 1 | Receiver compares Xon2, Xoff2 |
| 1 | 0 | 1 | 1 | Transmit Xon1, Xoff1 Receiver compares Xon1 or Xon2, Xoff1 or Xoff2 |
| 0 | 1 | 1 | 1 | Transmit Xon2, Xoff2 Receiver compares Xon1 or Xon2, Xoff1 or Xoff2 |
| 1 | 1 | 1 | 1 | Transmit Xon1 and Xon2, Xoff1 and Xoff2, Receiver compares Xon1 and Xon2, Xoff1 and Xoff2 |
| 0 | 0 | 1 | 1 | No transmit flow control, Receiver compares Xon1 and Xon2, Xoff1 and Xoff2 |

EFR[4]: Enhanced Function Bits Enable

Enhanced function control bit. This bit enables IER bits 4-7, ISR bits 4-5, FCR bits 4-5, and MCR bits 5-7 to be modified. After modifying any enhanced bits, EFR bit-4 can be set to a logic 0 to latch the new values. This feature prevents legacy software from altering or overwriting the enhanced functions once set. Normally, it is recommended to leave it enabled, logic 1.

- Logic 0 = modification disable/latch enhanced features. IER bits 4-7, ISR bits 4-5, FCR bits 4-5, and MCR bits 5-7 are saved to retain the user settings. After a reset, the IER bits 4-7, ISR bits 4-5, FCR bits 4-5, and MCR bits 5-7 are set to a logic 0 to be compatible with ST16C550 mode (default).
- Logic 1 = Enables the above-mentioned register bits to be modified by the user.

EFR[5]: Special Character Detect Enable

- Logic 0 = Special Character Detect Disabled (default).
- Logic 1 = Special Character Detect Enabled. The UART compares each incoming receive character with data in Xoff-2 register. If a match exists, the receive data will be transferred to FIFO and ISR bit-4 will be set to indicate detection of the special

character. Bit-0 corresponds with the LSB bit of the receive character. If flow control is set for comparing Xon1, Xoff1 (EFR [1:0]= '10') then flow control and special character work normally. However, if flow control is set for comparing Xon2, Xoff2 (EFR[1:0]= '01') then flow control works normally, but Xoff2 will not go to the FIFO, and will generate an Xoff interrupt and a special character interrupt, if enabled via IER bit-5.

EFR[6]: Auto RTS Flow Control Enable

RTS# output may be used for hardware flow control by setting EFR bit-6 to logic 1. When Auto RTS is selected, an interrupt will be generated when the receive FIFO is filled to the programmed trigger level and RTS de-asserts to a logic 1 at the next upper trigger level. RTS# will return to a logic 0 when FIFO data falls below the next lower trigger level. The RTS# output must be asserted (logic 0) before the auto RTS can take effect. RTS# pin will function as a general purpose output when hardware flow control is disabled.

- Logic 0 = Automatic RTS flow control is disabled (default).
- Logic 1 = Enable Automatic RTS flow control.

EFR[7]: Auto CTS Flow Control Enable

Automatic CTS Flow Control.

- Logic 0 = Automatic CTS flow control is disabled (default).
- Logic 1 = Enable Automatic CTS flow control. Data transmission stops when CTS# input de-asserts to logic 1. Data transmission resumes when CTS# returns to a logic 0.

4.22 SOFTWARE FLOW CONTROL REGISTERS (XOFF1, XOFF2, XON1, XON2) - READ/WRITE

These registers are used as the programmable software flow control characters xoff1, xoff2, xon1, and xon2. For more details, see Table 6 .

TABLE 16: UART RESET CONDITIONS FOR CHANNEL A AND B

| REGISTERS | RESET STATE |
|-------------|---|
| DLM and DLL | DLM = 0x00 and DLL = 0x01. Only resets to these values during a power up. They do not reset when the Reset Pin is asserted. |
| AFR | Bits 7-0 = 0x00 |
| RHR | Bits 7-0 = 0xFF |
| THR | Bits 7-0 = 0xFF |
| IER | Bits 7-0 = 0x00 |
| FCR | Bits 7-0 = 0x00 |
| ISR | Bits 7-0 = 0x01 |
| LCR | Bits 7-0 = 0x00 |
| MCR | Bits 7-0 = 0x00 |
| LSR | Bits 7-0 = 0x60 |
| MSR | Bits 3-0 = Logic 0 Bits 7-4 = Logic levels of the inputs inverted |
| SPR | Bits 7-0 = 0xFF |
| EMSR | Bits 7-0 = 0x80 |
| FLVL | Bits 7-0 = 0x00 |
| EFR | Bits 7-0 = 0x00 |
| XON1 | Bits 7-0 = 0x00 |
| XON2 | Bits 7-0 = 0x00 |
| XOFF1 | Bits 7-0 = 0x00 |
| XOFF2 | Bits 7-0 = 0x00 |
| FC | Bits 7-0 = 0x00 |
| I/O SIGNALS | RESET STATE |
| TX | Logic 1 |
| OP1# | Logic 1 |
| MF# | Logic 1 |
| RTS# | Logic 1 |
| DTR# | Logic 1 |
| TXRDY# | Logic 0 |
| INT | Logic 0 |

ABSOLUTE MAXIMUM RATINGS

| | |
|-----------------------|------------------|
| Power Supply Range | 7 Volts |
| Voltage at Any Pin | GND-0.3 V to 7 V |
| Operating Temperature | -40° to +85°C |
| Storage Temperature | -65° to +150°C |
| Package Dissipation | 500 mW |

TYPICAL PACKAGE THERMAL RESISTANCE DATA (MARGIN OF ERROR: ± 15%)

| | |
|------------------------------|--------------------------------------|
| Thermal Resistance (44-PLCC) | theta-ja = 50°C/W, theta-jc = 21°C/W |
|------------------------------|--------------------------------------|

ELECTRICAL CHARACTERISTICS

DC ELECTRICAL CHARACTERISTICS

UNLESS OTHERWISE NOTED: TA=0° TO 70°C (-40° TO +85°C FOR INDUSTRIAL GRADE PACKAGE), VCC IS 2.5V, 3.3V, 5.0V ±10%

| SYMBOL | PARAMETER | LIMITS 2.5V | | LIMITS 3.3V | | LIMITS 5.0V | | UNITS | CONDITIONS |
|--------------------|----------------------------|----------------|-----|----------------|-----|----------------|-----|-------|-------------------------|
| | | MIN | MAX | MIN | MAX | MIN | MAX | | |
| V _{ILCK} | Clock Input Low Level | -0.3 | 0.6 | -0.3 | 0.6 | -0.5 | 0.6 | V | |
| V _{IHCK} | Clock Input High Level | 2.0 | VCC | 2.4 | VCC | 3.0 | VCC | V | |
| V _{IL} | Input Low Voltage | -0.3 | 0.8 | -0.3 | 0.8 | -0.5 | 0.8 | V | |
| V _{IH} | Input High Voltage | 2.0 | VCC | 2.0 | VCC | 2.2 | VCC | V | |
| V _{OL} | Output Low Voltage | | | | | | 0.4 | V | I _{OL} = 6 mA |
| V _{OL} | Output Low Voltage | | 0.4 | | 0.4 | | | V | I _{OL} = 4 mA |
| V _{OH} | Output High Voltage | | | | | 2.4 | | V | I _{OH} = -6 mA |
| V _{OH} | Output High Voltage | 2.0 | | 2.0 | | | | V | I _{OH} = -1 mA |
| I _{IL} | Input Low Leakage Current | | ±10 | | ±10 | | ±10 | uA | |
| I _{IH} | Input High Leakage Current | | ±10 | | ±10 | | ±10 | uA | |
| C _{IN} | Input Pin Capacitance | | 5 | | 5 | | 5 | pF | |
| I _{CC} | Power Supply Current | | 2.7 | | 2.7 | | 4 | mA | |
| I _{SLEEP} | Sleep Current | | 30 | | 30 | | 50 | uA | See Test 1 |

Test 1: The following inputs should remain steady at VCC or GND state to minimize Sleep current: A0-A2, D0-D7, IOR#, IOW#, CSA# and CSB#. Also, RXA and RXB inputs must idle at logic 1 state while asleep.

AC ELECTRICAL CHARACTERISTICS
TA=0° TO 70°C (-40° TO +85°C FOR INDUSTRIAL GRADE PACKAGE), VCC IS 2.5- 5.0V ±10%

| SYMBOL | PARAMETER | LIMITS 2.5 | | LIMITS 3.3 | | LIMITS 5.0 | | UNIT | CONDITIONS |
|------------------|--|---------------|-----|---------------|-----|---------------|-----|------|-------------|
| | | MIN | MAX | MIN | MAX | MIN | MAX | | |
| CLK | Clock Pulse Duration | 50 | | 50 | | 17 | | ns | |
| OSC | Oscillator Frequency | | 16 | | 20 | | 24 | MHz | |
| OSC | External Clock Frequency | | 24 | | 33 | | 50 | MHz | |
| T _{AS} | Address Setup Time | 15 | | 10 | | 5 | | ns | |
| T _{AH} | Address Hold Time | 15 | | 10 | | 5 | | ns | |
| T _{CS} | Chip Select Width | 66 | | 66 | | 50 | | ns | |
| T _{RD} | IOR# Strobe Width | 50 | | 35 | | 25 | | ns | |
| T _{DY} | Read Cycle Delay | 50 | | 40 | | 30 | | ns | |
| T _{RDV} | Data Access Time | | 50 | | 50 | | 35 | ns | |
| T _{DD} | Data Disable Time | 0 | 35 | 0 | 35 | 0 | 25 | ns | |
| T _{WR} | IOW# Strobe Width | 40 | | 40 | | 25 | | ns | |
| T _{DY} | Write Cycle Delay | 50 | | 40 | | 30 | | ns | |
| T _{DS} | Data Setup Time | 15 | | 10 | | 5 | | ns | |
| T _{DH} | Data Hold Time | 15 | | 10 | | 5 | | ns | |
| T _{WDO} | Delay From IOW# To Output | | 50 | | 50 | | 40 | ns | 100 pF load |
| T _{MOD} | Delay To Set Interrupt From MODEM Input | | 50 | | 40 | | 35 | ns | 100 pF load |
| T _{RSI} | Delay To Reset Interrupt From IOR# | | 50 | | 40 | | 35 | ns | 100 pF load |
| T _{SSI} | Delay From Stop To Set Interrupt | | 1 | | 1 | | 1 | Bclk | |
| T _{RRI} | Delay From IOR# To Reset Interrupt | | 50 | | 45 | | 40 | ns | 100 pF load |
| T _{SI} | Delay From Stop To Interrupt | | 50 | | 45 | | 40 | ns | |
| T _{INT} | Delay From Initial INT Reset To Transmit Start | 8 | 24 | 8 | 24 | 8 | 24 | Bclk | |
| T _{WRI} | Delay From IOW# To Reset Interrupt | | 50 | | 45 | | 40 | ns | |
| T _{SSR} | Delay From Stop To Set RXRDY# | | 1 | | 1 | | 1 | Bclk | |
| T _{RR} | Delay From IOR# To Reset RXRDY# | | 50 | | 45 | | 40 | ns | |

AC ELECTRICAL CHARACTERISTICS

TA=0° to 70°C (-40° to +85°C for INDUSTRIAL GRADE PACKAGE), VCC IS 2.5- 5.0V ±10%

| SYMBOL | PARAMETER | LIMITS 2.5 | | LIMITS 3.3 | | LIMITS 5.0 | | UNIT | CONDITIONS |
|------------------|--|------------------|--------------------|---------------|--------------------|---------------|--------------------|------|------------|
| | | MIN | MAX | MIN | MAX | MIN | MAX | | |
| T _{WT} | Delay From IOW# To Set TXRDY# | | 50 | | 45 | | 40 | ns | |
| T _{SRT} | Delay From Center of Start To Reset TXRDY# | | 8 | | 8 | | 8 | Bclk | |
| T _{RST} | Reset Pulse Width | 40 | | 40 | | 40 | | ns | |
| N | Baud Rate Divisor | 1 | 2 ¹⁶ -1 | 1 | 2 ¹⁶ -1 | 1 | 2 ¹⁶ -1 | - | |
| Bclk | Baud Clock | 16X of data rate | | | | | | bps | |

FIGURE 13. CLOCK TIMING

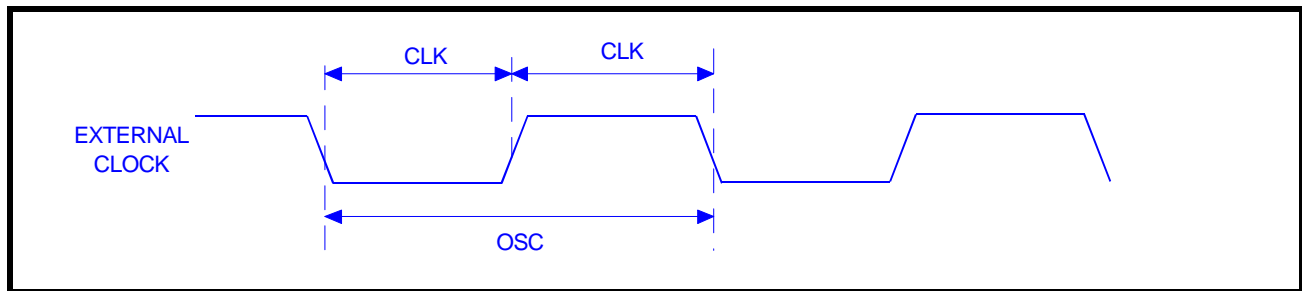


FIGURE 14. MODEM INPUT/OUTPUT TIMING FOR CHANNELS A & B

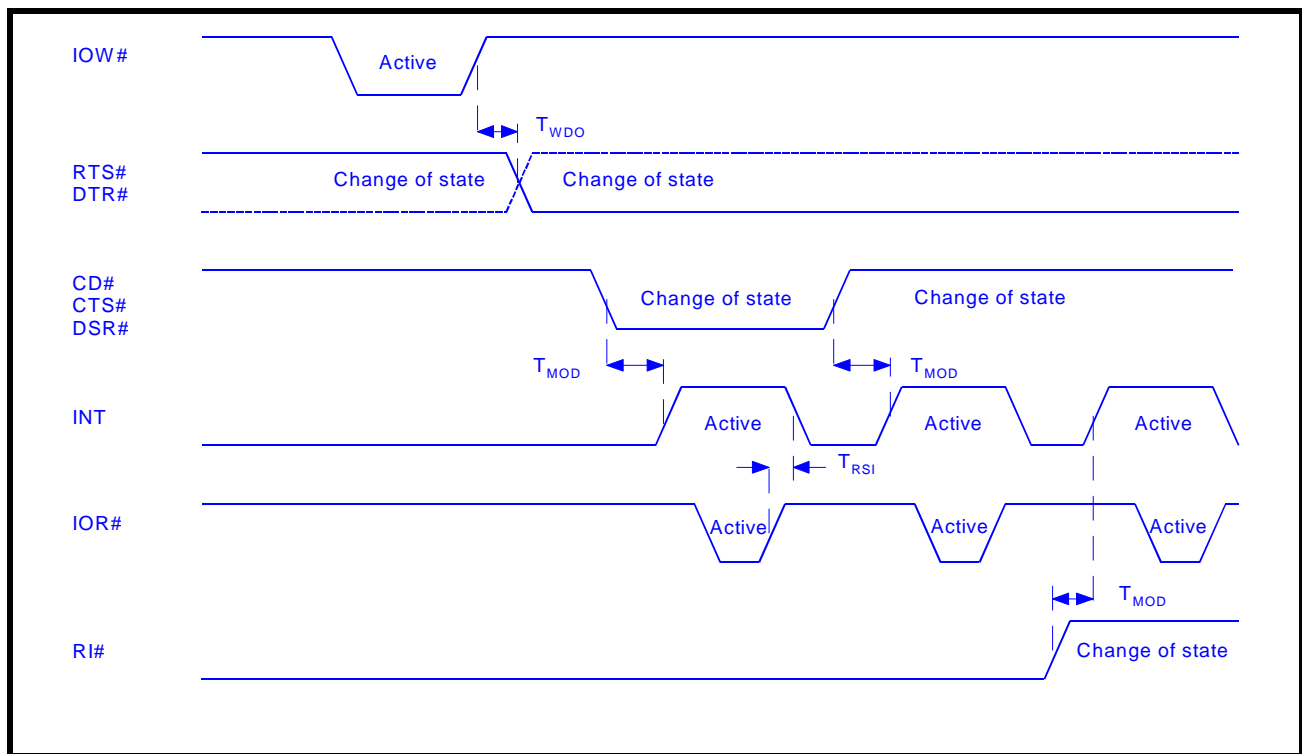


FIGURE 15. DATA BUS READ TIMING

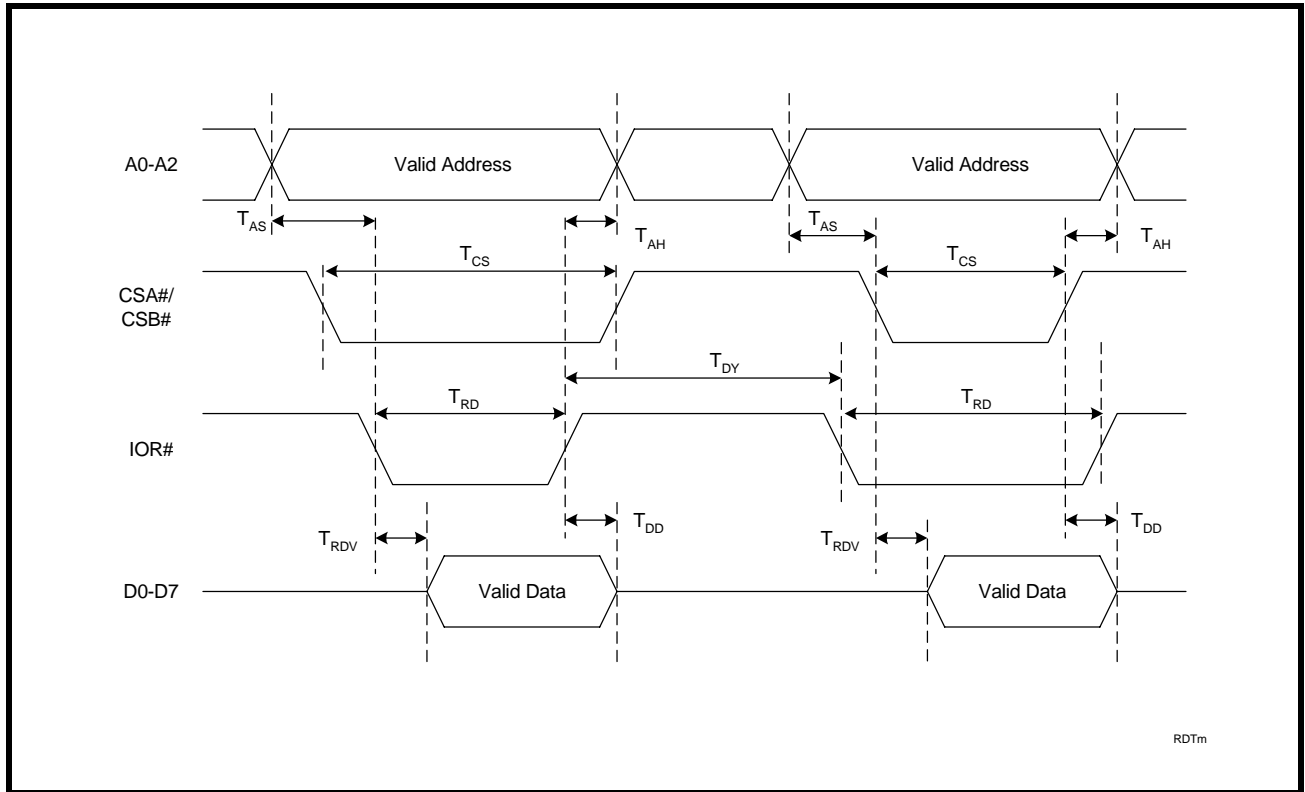


FIGURE 16. DATA BUS WRITE TIMING

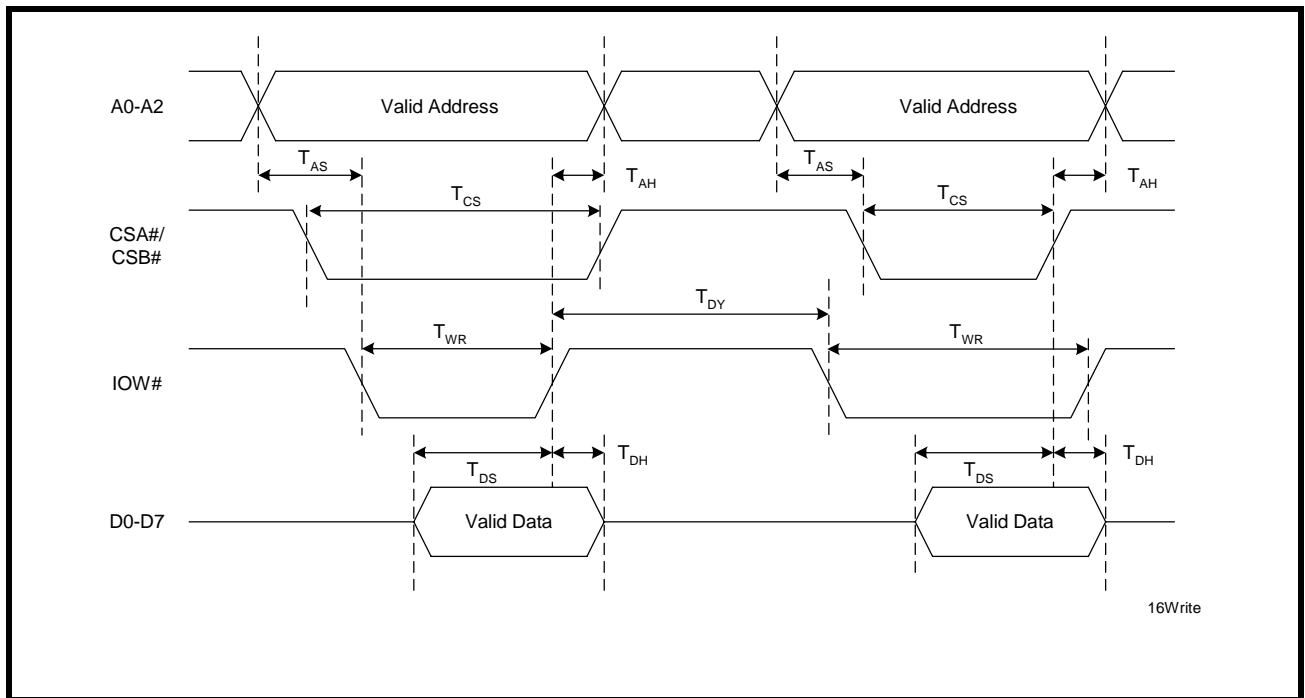


FIGURE 17. RECEIVE READY & INTERRUPT TIMING [NON-FIFO MODE] FOR CHANNELS A & B

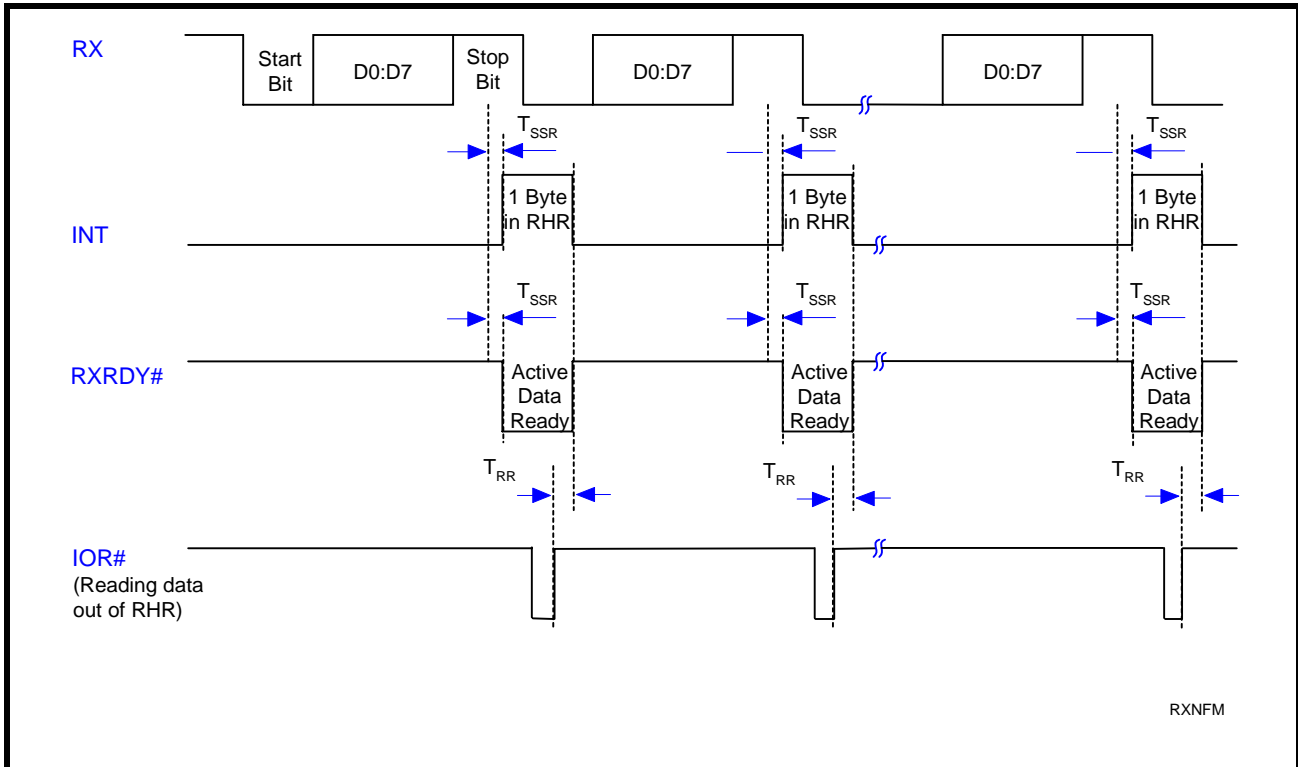


FIGURE 18. TRANSMIT READY & INTERRUPT TIMING [NON-FIFO MODE] FOR CHANNELS A & B

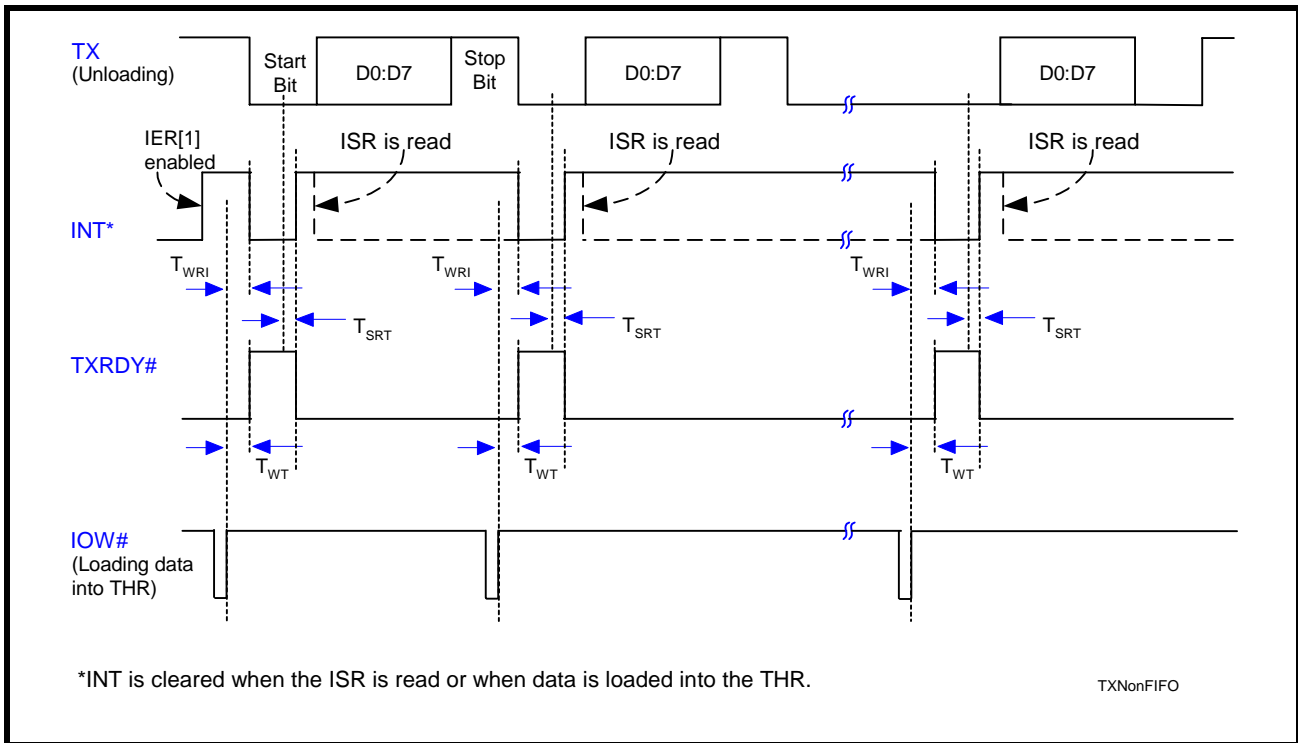


FIGURE 19. RECEIVE READY & INTERRUPT TIMING [FIFO MODE, DMA DISABLED] FOR CHANNELS A & B

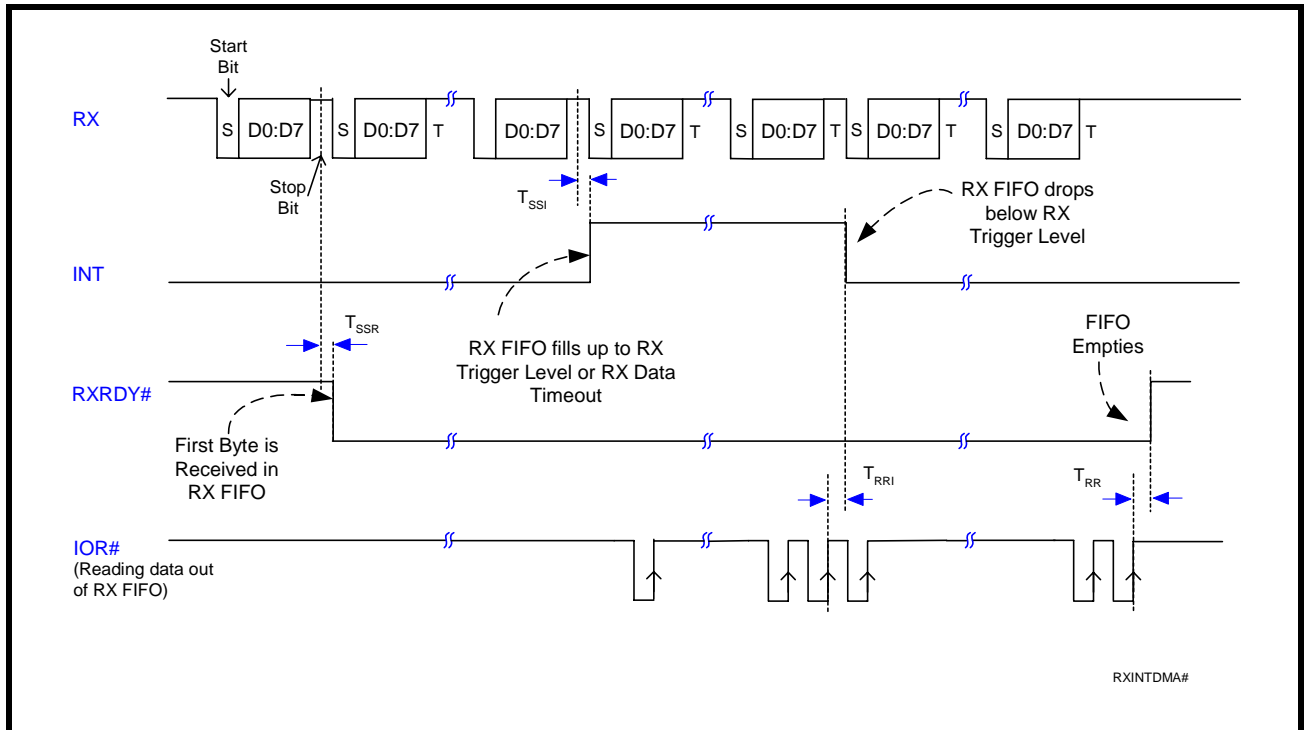


FIGURE 20. RECEIVE READY & INTERRUPT TIMING [FIFO MODE, DMA ENABLED] FOR CHANNELS A & B

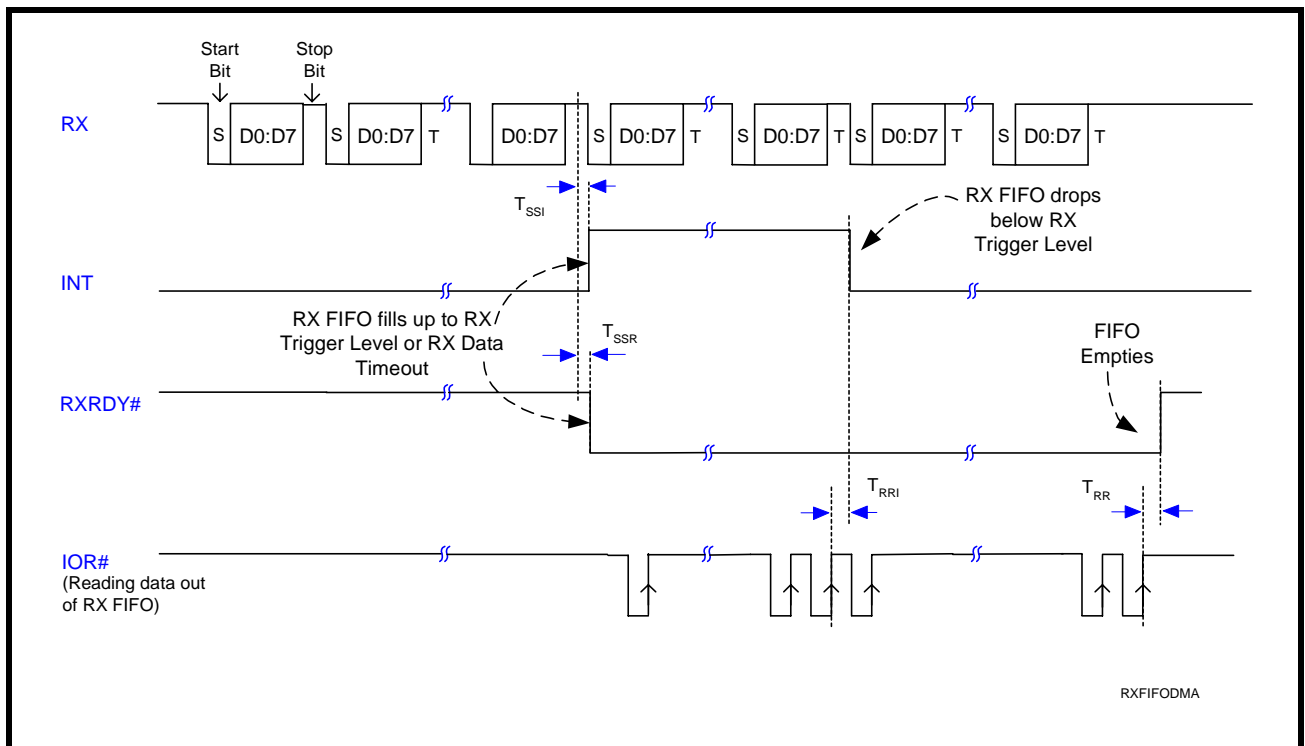


FIGURE 21. TRANSMIT READY & INTERRUPT TIMING [FIFO MODE, DMA MODE DISABLED] FOR CHANNELS A & B

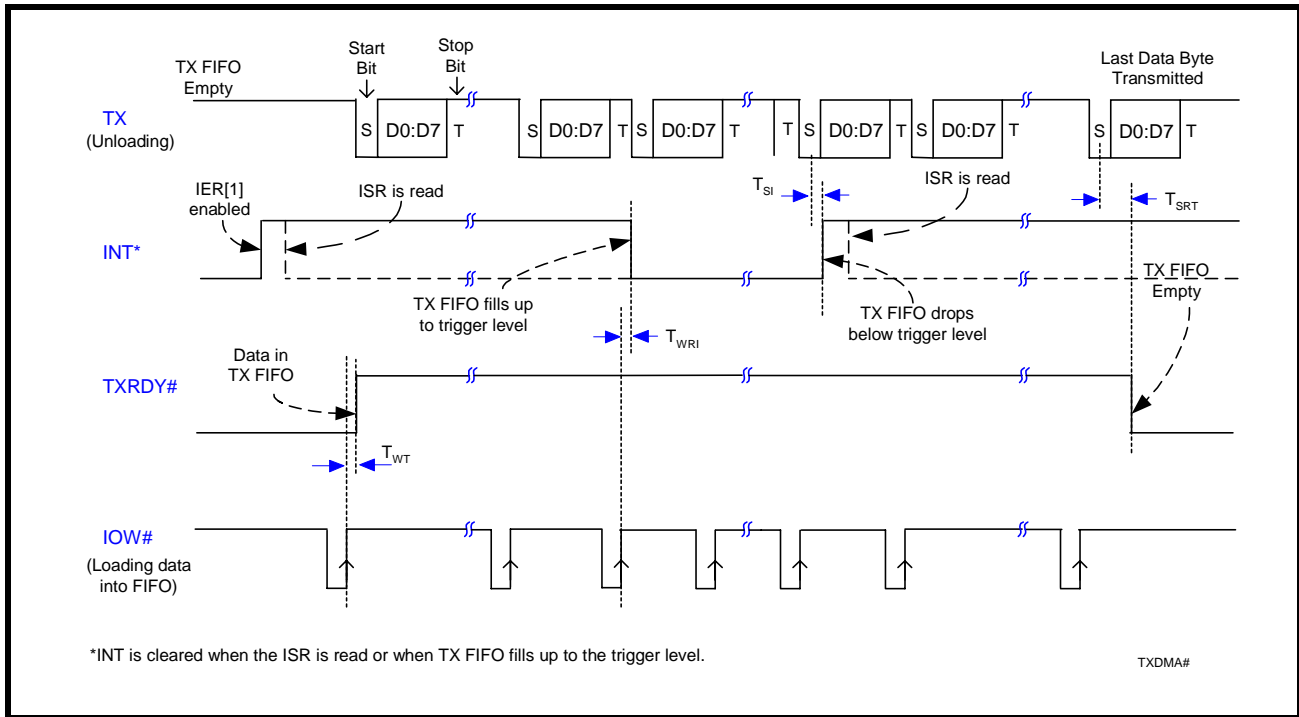
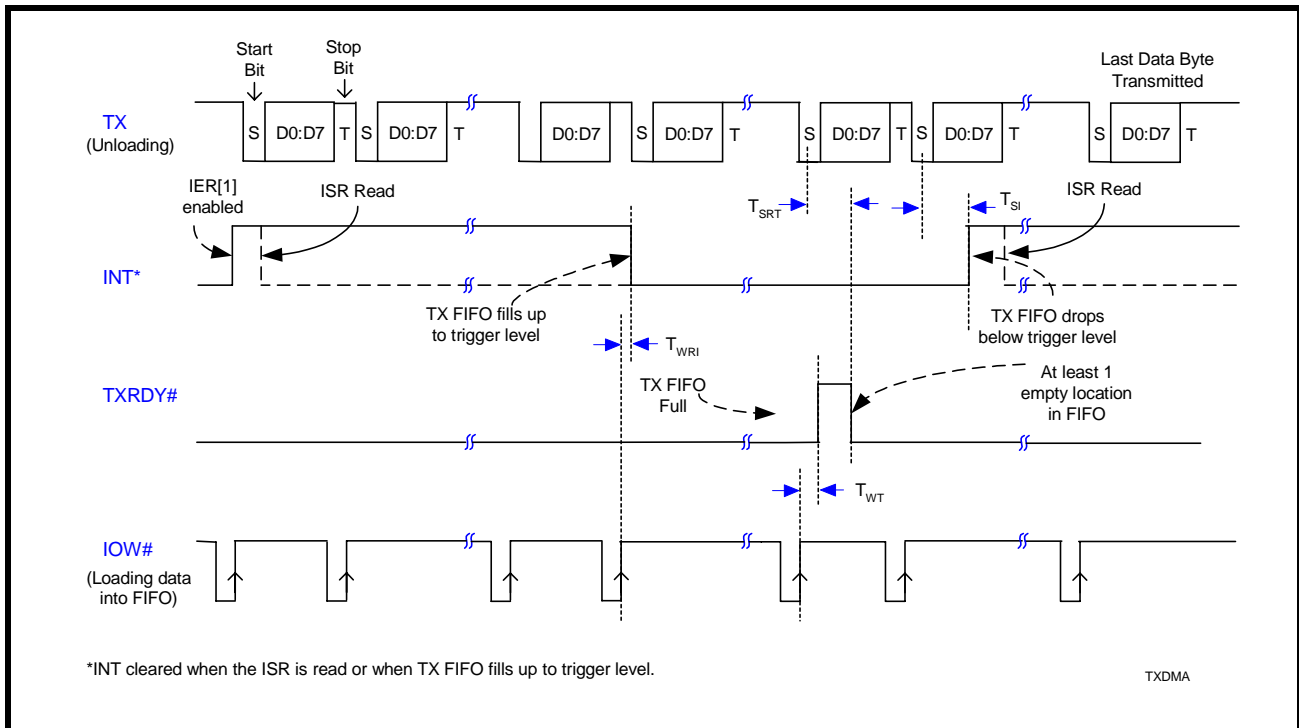
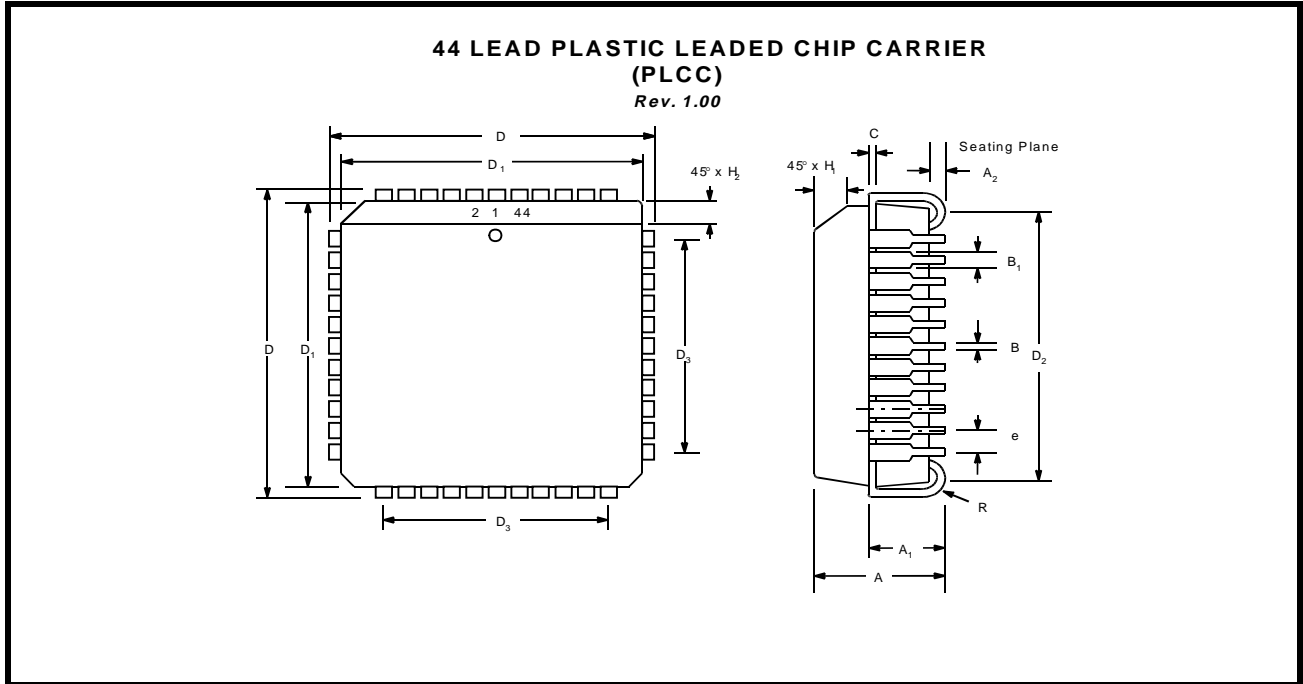


FIGURE 22. TRANSMIT READY & INTERRUPT TIMING [FIFO MODE, DMA MODE ENABLED] FOR CHANNELS A & B



PACKAGE DIMENSIONS (44 PIN PLCC)



Note: The control dimension is the millimeter column

| SYMBOL | INCHES | | MILLIMETERS | |
|----------------|------------|-------|-------------|-------|
| | MIN | MAX | MIN | MAX |
| A | 0.165 | 0.180 | 4.19 | 4.57 |
| A ₁ | 0.090 | 0.120 | 2.29 | 3.05 |
| A ₂ | 0.020 | --- | 0.51 | --- |
| B | 0.013 | 0.021 | 0.33 | 0.53 |
| B ₁ | 0.026 | 0.032 | 0.66 | 0.81 |
| C | 0.008 | 0.013 | 0.19 | 0.32 |
| D | 0.685 | 0.695 | 17.40 | 17.65 |
| D ₁ | 0.650 | 0.656 | 16.51 | 16.66 |
| D ₂ | 0.590 | 0.630 | 14.99 | 16.00 |
| D ₃ | 0.500 typ. | | 12.70 typ. | |
| e | 0.050 BSC | | 1.27 BSC | |
| H ₁ | 0.042 | 0.056 | 1.07 | 1.42 |
| H ₂ | 0.042 | 0.048 | 1.07 | 1.22 |
| R | 0.025 | 0.045 | 0.64 | 1.14 |

REVISION HISTORY

| <u>Date</u> | <u>Revision</u> | <u>Description</u> |
|---------------|-----------------|---|
| November 2001 | Rev P1.0.0 | Prelim datasheet. |
| March 2002 | Rev P1.1.0 | Corrected INTA/B pin descriptions and reset state. Renamed Sclk to Bclk. Changed A0-A7 in Figures 15 and 16 to A0-A2. |

NOTICE

EXAR Corporation reserves the right to make changes to the products contained in this publication in order to improve design, performance or reliability. EXAR Corporation assumes no responsibility for the use of any circuits described herein, conveys no license under any patent or other right, and makes no representation that the circuits are free of patent infringement. Charts and schedules contained here in are only for illustration purposes and may vary depending upon a user's specific application. While the information in this publication has been carefully checked; no responsibility, however, is assumed for inaccuracies.

EXAR Corporation does not recommend the use of any of its products in life support applications where the failure or malfunction of the product can reasonably be expected to cause failure of the life support system or to significantly affect its safety or effectiveness. Products are not authorized for use in such applications unless EXAR Corporation receives, in writing, assurances to its satisfaction that: (a) the risk of injury or damage has been minimized; (b) the user assumes all such risks; (c) potential liability of EXAR Corporation is adequately protected under the circumstances.

Copyright 2002 EXAR Corporation

Datasheet March 2002.

Send your UART technical inquiry with technical details to hotline: uarttechsupport@exar.com

Reproduction, in part or whole, without the prior written consent of EXAR Corporation is prohibited.

TABLE OF CONTENTS

GENERAL DESCRIPTION..... 1

APPLICATIONS..... 1

FEATURES 1

FIGURE 1. XR16L2752 BLOCK DIAGRAM..... 1

FIGURE 2. PIN OUT ASSIGNMENT..... 2

ORDERING INFORMATION 2

PIN DESCRIPTIONS 3

1.0 Product DESCRIPTION 6

2.0 FUNCTIONAL DESCRIPTIONS 7

 2.1 CPU INTERFACE 7

FIGURE 3. XR16L2752 DATA BUS INTERCONNECTIONS 7

 2.2 5-VOLT TOLERANT INPUTS 7

 2.3 DEVICE RESET 7

 2.4 DEVICE IDENTIFICATION AND REVISION 7

 2.5 CHANNEL A AND B SELECTION 7

TABLE 1: CHANNEL A AND B SELECT..... 7

 2.6 CHANNEL A AND B INTERNAL REGISTERS 8

 2.7 SIMULTANEOUS WRITE TO CHANNEL A AND B 8

 2.8 DMA MODE 8

TABLE 2: TXRDY# AND RXRDY# OUTPUTS IN FIFO AND DMA MODE 8

 2.9 INTA AND INTB OUPUTS 8

TABLE 3: INTA AND INTB PINS OPERATION FOR TRANSMITTER..... 9

TABLE 4: INTA AND INTB PIN OPERATION FOR RECEIVER..... 9

 2.10 CRYSTAL OSCILLATOR OR EXT. CLOCK INPUT 9

FIGURE 4. TYPICAL OSCILLATOR CONNECTIONS..... 9

 2.11 PROGRAMMABLE BAUD RATE GENERATOR 9

FIGURE 5. BAUD RATE GENERATOR AND PRESCALER 10

TABLE 5: TYPICAL DATA RATES WITH A 14.7456 MHZ CRYSTAL OR EXTERNAL CLOCK..... 10

 2.12 TRANSMITTER 11

 2.12.1 Transmit Holding Register (THR) - Write Only 11

 2.12.2 Transmitter Operation in non-FIFO Mode 11

FIGURE 6. TRANSMITTER OPERATION IN NON-FIFO MODE..... 11

 2.12.3 Transmitter Operation in FIFO Mode 11

FIGURE 7. TRANSMITTER OPERATION IN FIFO AND FLOW CONTROL MODE..... 12

 2.13 RECEIVER 12

 2.13.1 Receive Holding Register (RHR) - Read-Only 12

FIGURE 8. RECEIVER OPERATION IN NON-FIFO MODE 13

FIGURE 9. RECEIVER OPERATION IN FIFO AND AUTO RTS FLOW CONTROL MODE..... 13

 2.14 AUTO RTS (HARDWARE) FLOW CONTROL 13

 2.15 AUTO RTS HYSTERESIS 13

 2.16 AUTO CTS FLOW CONTROL 14

FIGURE 10. AUTO RTS AND CTS FLOW CONTROL OPERATION..... 14

 2.17 AUTO XON/XOFF (SOFTWARE) FLOW CONTROL 15

TABLE 6: AUTO XON/XOFF (SOFTWARE) FLOW CONTROL..... 15

 2.18 SPECIAL CHARACTER DETECT 15

 2.19 AUTO RS485 HALF-DUPLEX CONTROL 15

 2.20 INFRARED MODE 15

FIGURE 11. INFRARED TRANSMIT DATA ENCODING AND RECEIVE DATA DECODING 16

 2.21 SLEEP MODE WITH AUTO WAKE-UP 16

 2.22 INTERNAL LOOPBACK 17

FIGURE 12. INTERNAL LOOP BACK IN CHANNEL A AND B..... 17

3.0 UART INTERNAL REGISTERS 18

TABLE 7: UART CHANNEL A AND B UART INTERNAL REGISTERS..... 18

TABLE 8: INTERNAL REGISTERS DESCRIPTION. SHADED BITS ARE ENABLED WHEN EFR BIT-4=1 19

4.0 INTERNAL Register descriptions 20

| | |
|---|-----------|
| 4.1 RECEIVE HOLDING REGISTER (RHR) - READ- ONLY | 20 |
| 4.2 TRANSMIT HOLDING REGISTER (THR) - WRITE-ONLY | 20 |
| 4.3 BAUD RATE GENERATOR DIVISORS (DLL AND DLM) - READ/WRITE | 20 |
| 4.4 INTERRUPT ENABLE REGISTER (IER) - READ/WRITE | 20 |
| 4.4.1 IER versus Receive FIFO Interrupt Mode Operation..... | 20 |
| 4.4.2 IER versus Receive/Transmit FIFO Polled Mode Operation..... | 21 |
| 4.5 INTERRUPT STATUS REGISTER (ISR) - READ-ONLY | 22 |
| 4.5.1 Interrupt Generation: | 22 |
| 4.5.2 Interrupt Clearing:..... | 22 |
| TABLE 9: INTERRUPT SOURCE AND PRIORITY LEVEL..... | 22 |
| 4.6 FIFO CONTROL REGISTER (FCR) - WRITE-ONLY | 23 |
| TABLE 10: TRANSMIT AND RECEIVE FIFO TRIGGER LEVEL SELECTION..... | 24 |
| 4.7 LINE CONTROL REGISTER (LCR) - READ/WRITE | 24 |
| 4.8 ALTERNATE FUNCTION REGISTER (AFR) - READ/WRITE | 25 |
| TABLE 11: PARITY SELECTION..... | 25 |
| 4.9 MODEM CONTROL REGISTER (MCR) OR GENERAL PURPOSE OUTPUTS CONTROL - READ/WRITE | 25 |
| 4.10 LINE STATUS REGISTER (LSR) - READ ONLY | 26 |
| 4.11 MODEM STATUS REGISTER (MSR) - READ ONLY | 27 |
| 4.12 SCRATCH PAD REGISTER (SPR) - READ/WRITE | 27 |
| 4.13 ENHANCED MODE SELECT REGISTER (EMSR) | 27 |
| TABLE 12: SCRATCHPAD SWAP SELECTION..... | 27 |
| 4.14 FIFO LEVEL REGISTER (FLVL) - READ-ONLY | 28 |
| TABLE 13: AUTO RTS HYSTERESIS | 28 |
| 4.15 BAUD RATE GENERATOR REGISTERS (DLL AND DLM) - READ/WRITE | 28 |
| 4.16 DEVICE IDENTIFICATION REGISTER (DVID) - READ ONLY | 28 |
| 4.17 DEVICE REVISION REGISTER (DREV) - READ ONLY | 28 |
| 4.18 TRIGGER LEVEL / FIFO DATA COUNT REGISTER (TRG) - WRITE-ONLY | 28 |
| 4.19 FIFO DATA COUNT REGISTER (FC) - READ-ONLY | 28 |
| 4.20 FEATURE CONTROL REGISTER (FCTR) - READ/WRITE | 28 |
| TABLE 14: TRIGGER TABLE SELECT..... | 29 |
| 4.21 ENHANCED FEATURE REGISTER (EFR) | 29 |
| TABLE 15: SOFTWARE FLOW CONTROL FUNCTIONS | 30 |
| 4.22 SOFTWARE FLOW CONTROL REGISTERS (XOFF1, XOFF2, XON1, XON2) - READ/WRITE | 31 |
| TABLE 16: UART RESET CONDITIONS FOR CHANNEL A AND B | 31 |
| ABSOLUTE MAXIMUM RATINGS..... | 32 |
| TYPICAL PACKAGE THERMAL RESISTANCE DATA (MARGIN OF ERROR: ± 15%) | 32 |
| ELECTRICAL CHARACTERISTICS | 32 |
| DC ELECTRICAL CHARACTERISTICS | 32 |
| AC ELECTRICAL CHARACTERISTICS..... | 33 |
| TA=00 TO 70oC (-40o TO +85oC FOR INDUSTRIAL GRADE PACKAGE), VCC IS 2.5- 5.0V ±10%..... | 33 |
| FIGURE 13. CLOCK TIMING..... | 34 |
| FIGURE 14. MODEM INPUT/OUTPUT TIMING FOR CHANNELS A & B..... | 34 |
| FIGURE 15. DATA BUS READ TIMING | 35 |
| FIGURE 16. DATA BUS WRITE TIMING..... | 35 |
| FIGURE 17. RECEIVE READY & INTERRUPT TIMING [NON-FIFO MODE] FOR CHANNELS A & B..... | 36 |
| FIGURE 18. TRANSMIT READY & INTERRUPT TIMING [NON-FIFO MODE] FOR CHANNELS A & B..... | 36 |
| FIGURE 19. RECEIVE READY & INTERRUPT TIMING [FIFO MODE, DMA DISABLED] FOR CHANNELS A & B..... | 37 |
| FIGURE 20. RECEIVE READY & INTERRUPT TIMING [FIFO MODE, DMA ENABLED] FOR CHANNELS A & B..... | 37 |
| FIGURE 21. TRANSMIT READY & INTERRUPT TIMING [FIFO MODE, DMA MODE DISABLED] FOR CHANNELS A & B..... | 38 |
| FIGURE 22. TRANSMIT READY & INTERRUPT TIMING [FIFO MODE, DMA MODE ENABLED] FOR CHANNELS A & B..... | 38 |
| PACKAGE DIMENSIONS (44 PIN PLCC) | 39 |
| REVISION HISTORY..... | 40 |
| TABLE OF CONTENTS | I |