10k ECL Delay Lines

ECLDL
16-pin DIP

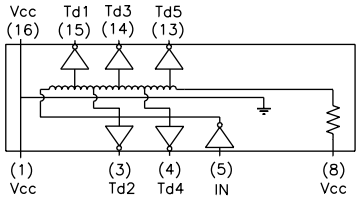
- **10k ECL buffered input and output in 16-pin transfer-molded DIP.**
- **5-tap line provides delays from 5 ns to 500 ns.**
- **Temperature range -30 to +85°C.**
- **Transfer molded—reliable.**
- **Fanout: 83 ECL loads.**
- **Military models with temperature range -55 to +125°C and ceramic package IC. Add suffix "M" to part number.**
- **Military models as above, but with ceramic package IC screened to MIL- STD-883C. Add suffix "MX" to part number.**
- **Military models as "MS" above, but with in-house burn-in and thermal shock, add suffix "MY".**

MODEL ECLDL ACTIVE DELAY LINES

TECHNITROL PART NO.	TAP DELAYS (ns)					Output Rise Time (ns)
	T_O1	T_O2	T_O3	T_O4	T_O5	
ECLDL025	5	10	15	20	25	4
ECLDL050	10	20	30	40	50	4
ECLDL075	15	30	45	60	75	5
ECLDL100	20	40	60	80	100	6
ECLDL125	25	50	75	100	125	7
ECLDL150	30	60	90	120	150	7
ECLDL200	40	80	120	160	200	8
ECLDL250	50	100	150	200	250	10
ECLDL300	60	120	180	240	300	15
ECLDL350	70	140	210	280	350	15
ECLDL400	80	160	240	320	400	15
ECLDL450	90	180	270	350	450	20
ECLDL500	100	200	300	400	500	20

Delay Characteristics measured at V_{CC} = -5.2V ± .01 Vdc. T_a = 25° C.
Delay Tolerance ±1.5 ns or 5%, whichever is greater.
Delay time measured @ -1.3V.
500 linear FPM airflow and output terminated with 50 ohm to -2.0 Vdc.
Rise time measured @ 20 to 80% of output pulse.
For minimum input pulse width -- contact factory.

SCHEMATIC



ECLDL
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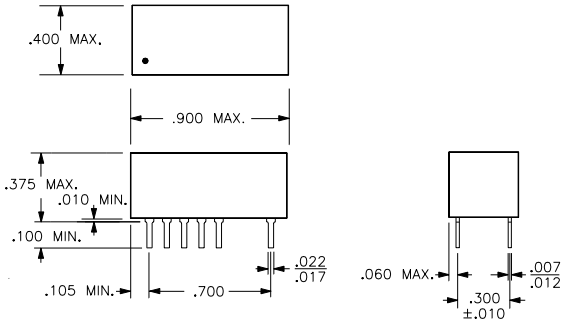
MECHANICAL OUTLINE



Notes

- Only the pins specified in the schematics are provided with each package.
- Pin numbers shown are for reference only and are not necessarily marked on unit.
- Lead material is electro tin plated (alloy 42) or solder dipped.
- All specifications are subject to change without notice.

TWO PEARL BUCK COURT ● BRISTOL, PA 19007-6812 ● TEL 215-781-6400 ● FAX 215-781-6403 ● www.pulsespecialty.com