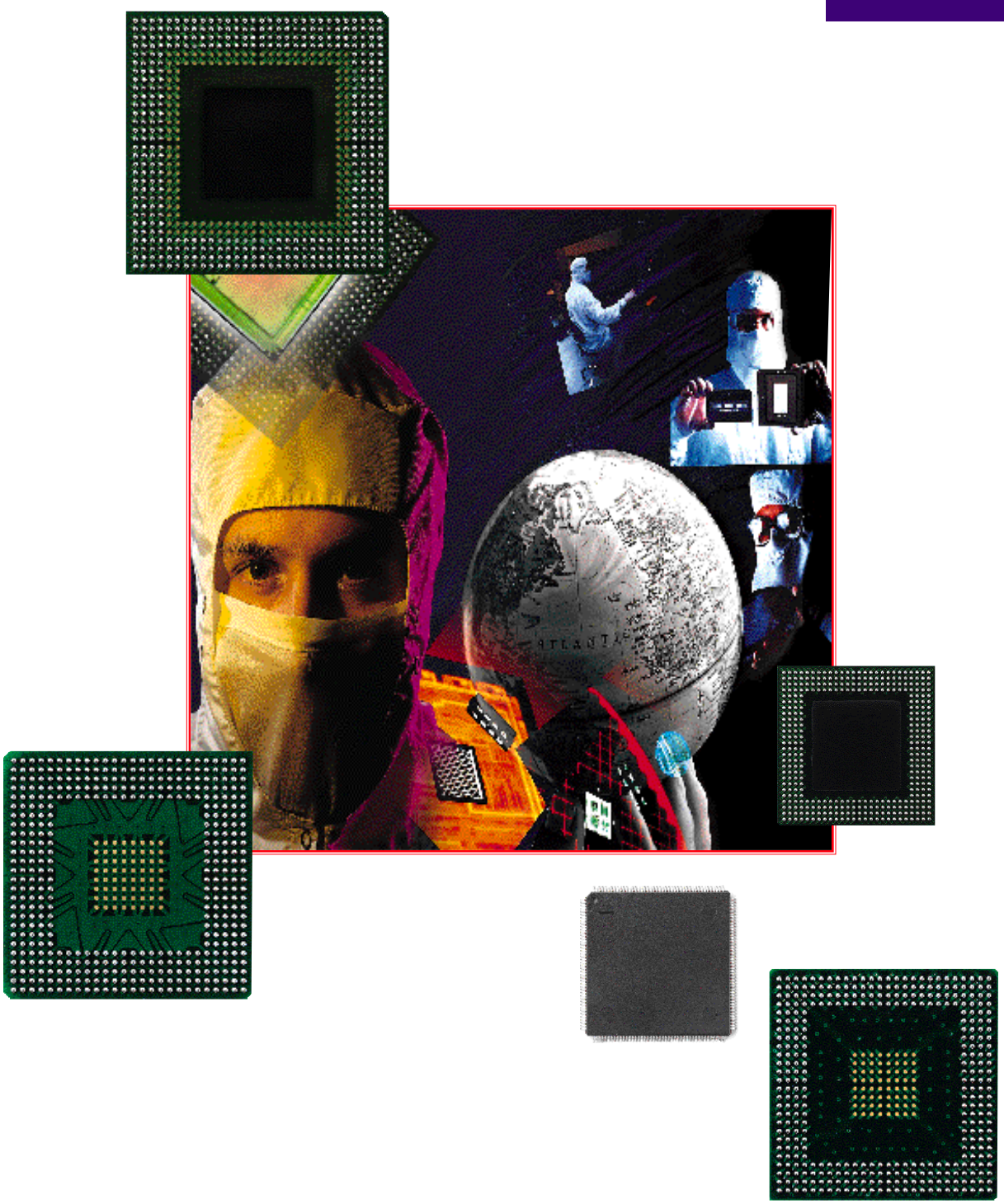
HIGH-DENSITY

KZ300GH
KZ300EH

CMOS GATE ARRAYS



KAWASAKI LSI

Overview

With the KZ300GH/KZ300EH CMOS Series, Kawasaki LSI offers an advanced, 0.5micron generation of gate arrays and embedded arrays. These leading-edge devices provide optimal solutions to meet your cost and performance needs for low-voltage, high-speed applications, combined with quick turnaround. The technology is ideal for high-volume applications in the computing and communications markets that require up to a 100MHz system clock.

To achieve integration densities up to 1 million gates, these gate arrays use Kawasaki LSI's 0.37µm effective channel length (0.5µm drawn gate length), DLM (Double Layer Metal) or TLM (Triple Layer Metal) process technology. Using Kawasaki LSI's tight metal gridsize and unique cell architecture, you can now achieve very high-density, high-performance, and very low-power dissipation–comparable to standard-cell products. This Series also makes available I/O buffers such as LVTTL, 5V-tolerant LVTTL, and 3.3V-PCI Bus, and supports standards such as GTL+, USB, and PECL.

The KZ300GH/KZ300EH Series offers a wide selection of compilable memories, so you can optimize your design by choosing the best solution to satisfy your requirements. For high-performance, design convenience and fast time-to-market, the Series offers value-added analog functions (PLL, A/D Converter, D/A Converter, etc.), CPU (and its peripheral) cores, JPEG core, and CAM (Content-Addressable Memory) core. You can also maximize chip-level and system-level performance for complex chips using the Kawasaki LSI design methodology, which includes a large library of accurately characterized cells, timing-driven synthesis, clock distribution schemes, test insertion, and physical layouts driven from a floor planner on industry-standard tools.

Quality and Reliability

Kawasaki LSI is committed to supplying high-quality products with reliability levels meeting or exceeding semiconductor industry standards. Quality is designed in from the earliest stages of product development and is an integral part of productization and manufacturing in volume production. The benefit of this focus to the customer is that Kawasaki LSI delivers modeling libraries on multiple tools that provide excellent correlation to the actual silicon performance and result in designs that physically work according to the simulations.

Also, rigid qualification tests are performed on each product introduced to ensure that exacting industry standards of reliability are met.

In production, Kawasaki LSI continually strives to improve quality, lower costs and speed delivery–by process automation, operator education, and statistical process control.

Kawasaki LSI has been ISO9001 qualified on semiconductor manufacturing and design since 1994.

Key Features

- 0.5µm (drawn) double/triple layer metal 3.3V-optimized CMOS process
- Gate Array Architecture (18 masterslices) for fastest time-to-market
- Embedded Arrays offered for fast complex designs with Megafunctions
- Unique cell architecture for high-density and high-performance designs competing with Std. Cell solutions
- Power dissipation of 0.9µW/MHz/gate (average gate, standard condition)
- Customized array options available for high volume applications
- Wide selection of I/O functionality (LVTTL, PCI, GTL, GTL+, USB, PECL)
- Design system with open interface to a variety of front-end platforms
- Large macrocell library for effective logic synthesis
- Clock skew management; PLL and clock distribution methodologies
- Testability tools such as SCAN TEST, IDDQ, and JTAG
- Six types of metal-programmable SRAM compilers
- High-density all-layer memory compilers; up to 15K bits/mm^2 for RAM
- I/O drive: 2~24mA, including slew rate
- 5V-tolerant I/O interface capability
- Plastic flat packs (QFP), Ball Grid Array (BGA) and Pin Grid Array (PGA) packages available

Core Library

The KZ300GH/KZ300EH Series library offers more than 300 robust macrocells, providing a variety of high-performance synthesizing options. The macrocells are composed of different sized transistors, enabling you to optimize for speed, power and density. The macrocells have input slew-rate-dependent loading and off-set delay, and non-linear output load dependent delay parameters to produce accurate characterized timings, resulting in the maximum performance achievable from the process technology. The core library is supplied for many industry-standard tools, including Verilog HDL, VHDL, Synopsys, Mentor, ViewLogic and others.

I/O LIBRARY

The I/Os in this Series are powered from a 3.3V supply, and input and output signals are tuned to this voltage. Kawasaki LSI also provides 5V-tolerant I/Os, which can receive signals from a 5V-powered device, but can output 3.3V. Kawasaki LSI's 5V-tolerant I/Os are realized by its unique, proprietary circuit technology. Options such as slew-rate controlled buffers, input with pull-up, pull-down resistors, and open drain outputs are available.

The KZ300GH/KZ300EH Series also supports low-voltage swing I/Os. Kawasaki LSI's 3.3V PCI Bus I/O buffer uses only one I/O slot, and is an optimal solution for interfacing to industry-standard PCI Buses. Standards such as Pseudo-ECL (PECL), GTL and GTL+, and Universal Serial Bus (USB), are also supported.

Kawasaki LSI is developing a new library of compact I/Os with simplified functions for cost reduction of pad-limited designs.

MEMORIES

Metal-Programmable Memory

The KZ300GH/KZ300EH Series has two types of metal-programmable memory compilers: High-Density (HD) RAM compiler and Low-Power (LP) RAM compiler. HD RAMs feature very high-performance, including more than 100MHz operation, offering high-density up to 6K bits/mm^2. HD RAMs are suitable for applications that need high-performance, high-density memories. The total capacity of a HD RAM is up to 36K bits per block.

LP RAMs feature high-performance and very low-power. The total capacity of an LP RAM is 16K bits. LP RAMs are suitable, for example, to the needs of register files. Table 1 shows the performance and specification of HD and LP RAMs.

Table 1 KZ300GH Metal-Programmable Memories

		Total Bits	Word	Bit	Density	Access Time
High-Density	1-p Async.	64~36K	64~4K	1~36	~5,985 bits/mm^2	4.4 ns*
	2-p Async.	64~36K	64~4K	1~36	~2,901 bits/mm^2	5.2 ns*
	1-p Sync.	64~36K	64~4K	1~36	~5,788 bits/mm^2	4.9 ns*
	2-p Sync.	64~36K	64~4K	1~36	~2,858 bits/mm^2	5.4 ns*
Low-Power	1-p Async.	1~16K	1~128	1~128	~2,830 bits/mm^2	4.0 ns**
	2-p Async.	1~16K	1~128	1~128	~2,830 bits/mm^2	4.0 ns**

*Access time is for 512-word x 8-bit configuration in typical condition.
**Access time is for 32-word x 8-bit configuration in typical condition.

All-Layer Memory

In the KZ300EH Series, higher density embedded memories are provided by all-layer memory compilers. All-layer memories feature extremely high-density, large-capacity, and high-performance, while offering low-power dissipation. The largest compilable RAM is 256K bits, and 1M bit for ROM. The bit density of 15K bits/mm^2 for the single-port RAM is high for an ASIC memory.

These Kawasaki LSI all-layer memories are tuned for high-performance, memory-intensive applications such as image processing, ATM switches, etc. If lower power is required, an Address Transition Detection (ATD) circuit can be optionally added. ATD detects the address transition, then starts accessing the memory. After a certain period of time, it turns off the entire memory operation to cut off the DC current and prepare for the next address transition automatically. This option is very effective for power reduction when the operating frequency is less than 66MHz in RAMs, and less than 30MHz in ROM.

Kawasaki LSI is now developing ASIC-DRAM as one of the all-layer memories offered; the size of a 256K-bit block is targeted to be 60% of that of the all-layer single-port RAM, with a density of about 26K bits/mm^2. A 50MHz (worst case condition) high-speed page mode operation would be achieved. Table 2 shows the performance specifications of all-layer memories.

Table 2 KZ300EH All-Layer Memories

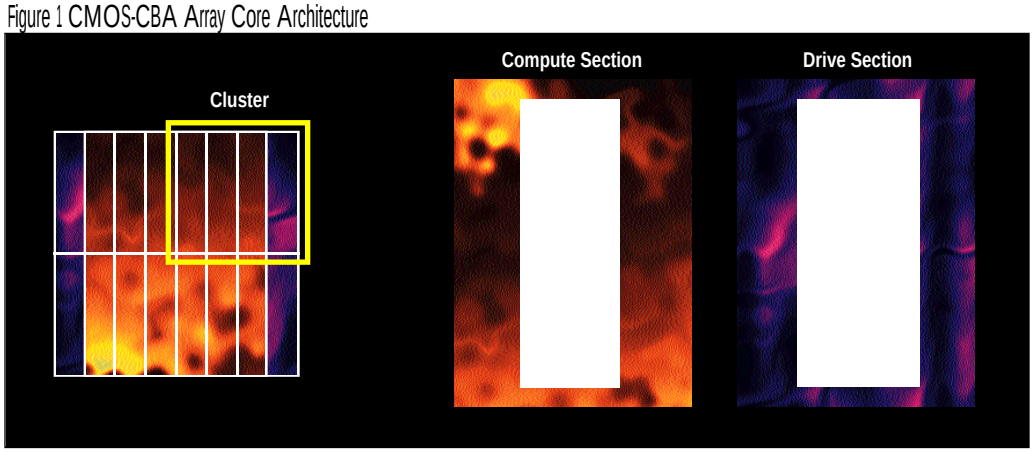
		Total Bits	Word	Bit	Density	Access Time
SRAM	1-p Async.	16~256K	16~8K	1~64	~15,457 bits/mm^2	4.9 ns*
	2-p Async.	16~256K	16~8K	1~64	~8,244 bits/mm^2	5.4 ns*
ROM	1-p Async.	64~1M	64~128K	1~128	~98,274 bits/mm^2	5.9 ns*
DRAM**	1-p Sync.	256K	8K	16 x 2 bank	–	–

*The numbers are for 512-word x 8-bit configuration in typical condition.
**Under development

Array Architecture

The core cell of the KZ300GH/KZ300EH Series, shown in Figure 1, is based on the CMOS-CBA® architecture licensed by Synopsys, Inc. It consists of two different unit cells, a compute cell and a drive cell. A compute cell contains four small PMOS and four small NMOS transistors that are optimized for building logic and memory. A drive cell contains two large PMOS and two large NMOS transistors that provide sufficient drive for global nets or large fanout. Macrocells are built mixing these two unit cells. Three compute cells and one drive cell in a cluster have been determined by statistical analysis to provide an optimal density capability for many design styles. Four clusters are indicated in Figure 1. Since a compute cell has low input capacitance and consumes less power, the performance of the KZ300GH/KZ300EH Series is very similar to that achieved with standard cell technologies. With this optimized cell architecture, KZ300GH/KZ300EH arrays achieve a gate density of up to 5,300 usable gates/mm^2.

Figure 1 CMOS-CBA Array Core Architecture



Array Family

Table 3 shows the 18 base arrays in the KZ300GH/KZ300EH Series. Array utilization depends on design, and typically varies from 28 to 40% in DLM (Double Layer Metal) technology, and from 45 to 60% in TLM (Triple Layer Metal) technology. A compute cell or a drive cell is counted as a gate. This unique cell architecture results in a higher integration density compared to conventional gate array technology composed of four transistor cells. Kawasaki LSI offers an option to compile and fabricate a custom sized array for a specific high-volume design.

Table 3 KZ300GH Masterslice Selection

Array Index	Pad Count (by Pad Pitch)			Raw Gates	Usable Gates	
	Very Fine	Fine	Standard		DLM	TLM
005	132	112	108	48,400	19,400	29,000
007	136	136	128	71,800	28,700	43,100
011	184	160	152	105,000	40,200	60,400
013	204	180	168	129,600	48,300	72,400
016	224	196	184	156,800	56,800	85,200
022	264	232	216	219,000	75,300	113,000
025	284	252	232	254,000	85,200	127,800
030	304	268	248	296,000	96,900	145,400
034	324	284	264	336,400	107,700	161,500
038	344	304	280	379,500	118,700	178,100
041	360	316	292	414,700	127,600	191,500
047	384	340	312	473,300	141,800	213,000
053	404	356	328	530,000	155,500	238,500
057	420	372	340	565,500	163,400	254,500
064	444	392	360	640,000	180,300	288,000
090	524	464	424	898,700	251,600	404,400
120	604	536	488	1,192,500	333,900	536,600
173	724	640	584	1,731,900	484,900	779,300

*Typical design both for DLM and TLM
**A compute cell or a drive cell is counted as a gate.

MEGAFUNCTIONS AND ANALOG FUNCTIONS

Kawasaki LSI does offer a number of Megafunctions other than the compiled memories, which can be supported in the KZ300GH/KZ300EH Series to minimize design time and maximize performance of complex system chips. The KC80 is a very high-performance CPU core that is binary-compatible with the Zilog Z80. A JPEG core is also available for imaging and data compression applications. Kawasaki LSI also offers an Address Processor Core or Content Addressable Memory (CAM) for high-performance broadband network and internetworking applications.

There are a number of analog functions that are under development for video signal processing applications, system clock management and frequency synthesis. These functions include 8- to 10-bit A/D converters, 8-bit D/A converters, Operational Amplifiers, Comparators, Phase Locked Loops (PLL) and Voltage Controlled Oscillators (VCO).

PHASE LOCKED LOOP (PLL)

As system clock frequencies increase, clock skew must be minimized between different chips in a system to maximize system performance. Kawasaki LSI's KZ300GH/KZ300EH Series offers the PLL function, which synchronizes the ASIC's internal clock to the external system clock to minimize the skew between chips on a board. The frequency of the internal clock can be a multiple of the external clock. The specification and range of the PLL in KZ300GH/KZ300EH technology is indicated in Table 4.

Table 4 KZ300GH/KZ300EH PLL Specifications

CHARACTERISTICS	SPECIFICATIONS
Operating Frequency	20MHz~162MHz
Maximum Input Phase Tolerance	+/- 50ppm
Maximum Jitter	-150ps~150ps
Maximum Phase Error	-300ps~300ps
Duty Cycle	45%~55%

CLOCK DISTRIBUTION

It is important to minimize not only chip-to-chip level system clock skew, but also chip-level clock skew on a die for maximum system performance. Kawasaki LSI provides several clocking methodologies to minimize on-chip clock skew. You can choose from these implementations, and also combine them to satisfy your design requirements. The recommended maximum loading and specification for each are indicated in Table 5.

Clock Buffer

This method is most popular and is well utilized in older technologies. This is simple and effective in cases where the number of clocked elements are less than a few hundred, or the clock skew requirement is not severe. In the KZ300GH/KZ300EH Series, up to 200 flip-flops (depends on frequency) can be driven in a single stage with special buffers for clocking.

Clock Tree Synthesis (CTS)

Clock Tree Synthesis is an automatic way to build a clock tree by balancing the far end delay with local buffers at the most appropriate physical location. The clock tree is synthesized with low driving inverters or buffers. Clock Tree Synthesis (CTS) is efficient when the number of clocked instances is very large or the clock skew requirement is strict.

Clock Trunk with CTS

The clock trunk is a wide metal line which is connected to a special clock driver. It provides lower skew and a shorter delay than a clock buffer or CTS. In the KZ300GH/KZ300EH Series, a strong clock driver can be built with multiple special buffers for clocking, or can be configured with an I/O clock driver, which typically uses 2 to 3 I/O pads.

Table 5 Recommended Maximum Loading and Specification for Clock Distribution Methodology

	NUMBEROF CLOCKED INSTANCES	TARGETED CLOCK SKEW	TARGETED CLOCK INSERTION DELAY
CLOCK BUFFER	≤200	≤500ps~1000ps	≤2~3ns (typical)
CLOCK TREE SYNTHESIS (CTS)	≤3000	≤300ps~500ps	≤2~4ns (typical)
CLOCK TRUNKWITH CTS	≤5000	≤300ps~500ps	≤1~2ns (typical)

Packages

Kawasaki LSI has internal ceramic packaging capabilities that can offer accelerated prototype deliveries. External subcontractors are used for the most popular cost effective plastic packaging that high-volume designs demand and Kawasaki LSI has some close developmental relationships with key vendors to ensure that the next generation of industry standard Ball Grid Arrays (BGA) will be offered to customers with designs exceeding about 300 pins. The extent of the packaging solutions are shown in Table 6.

Table 6 KZ300GH/KZ300EH Package Offerings

Package	Pin Count										
Skinny Dip	42	64									
PQFP	44	64	80	100	120*	144*	160*	176*	208*	240*	304*
TQFP (1.4 mm thick body)	64	80	100	144							
PBGA	256	304	352	420	480	576					
TBGA	256	304	352	420	480	576	672				
PGA	144	180	208	256	280						

*Drop-in heat spreader available for high power dissipation

Test Methodology

To ensure a high-quality device, it is important to implement a test with high-fault coverage. Kawasaki LSI's test methodology for the KZ300GH/KZ300EH Series includes the following test solutions.

Internal Full Scan Testing

Internal Full Scan Testing is one of the most powerful test methodologies for automatically developing test vectors, achieving more than 95% stuck-at fault coverage for large synchronous designs. This methodology is supported using Synopsys' Test Compiler, which automatically performs testability rule checking, scan chain insertion and ATPG (Automatic Test Pattern Generation).

IDDQ Testing

IDDQ Testing is an effective methodology which detects various types of silicon defects without area or performance overhead. This methodology is supported by measuring the device's quiescent power-supply current on functional vectors selected by CM-iTest from CrossCheck, Inc. This test provides an easy way to improve the fault coverage of an ad-hoc test strategy.

JTAG (IEEE 1149.1 Boundary Scan Testing)

JTAG is supported by inserting the boundary scan circuits into the system logic and providing test vectors and BSDL for the boundary scan logic. The TAP controller and associated logic is transparently inserted into the customer's netlist.

Process Monitoring

Process monitoring is performed by adding an AC measurement circuit into the device and measuring the AC delay. This AC measurement verifies that the device can operate at a required frequency.

Fault Simulation

Fault simulation is supported using the Cadence Verifault-XL simulator, which allows you to rapidly obtain fault coverage information for the applied test vectors.

Table 7 Kawasaki LSI's Test Solutions

Capability	LSI Availability Status	Customer Development Time	LSI Service Development Time	ATPG Availability	Target Fault Coverage	Performance Penalty	Silicon Overhead
Internal Scan	Now	<1 week	<1 week	Now	>95%	5-15%	5-12%
IDDQ	Now	Design Development	1-4 weeks	Not Yet	>90% Low Speed	None	None
JTAG	Now	<1 day	<1 day	Now	>95%	0.4-1.0 ns	400 + BSR* Gates
Process Monitoring	Now	<1 day	2-3 days	Not Required	N/A	None	<200 Gates
Fault Simulation	Now	Design Development	Design Development	Not Required	>95%	None	None

*BSR = 21 x input pin + 21 x output pin (2state) + 42 x output pin (3state) + 46 x bi-directional pin

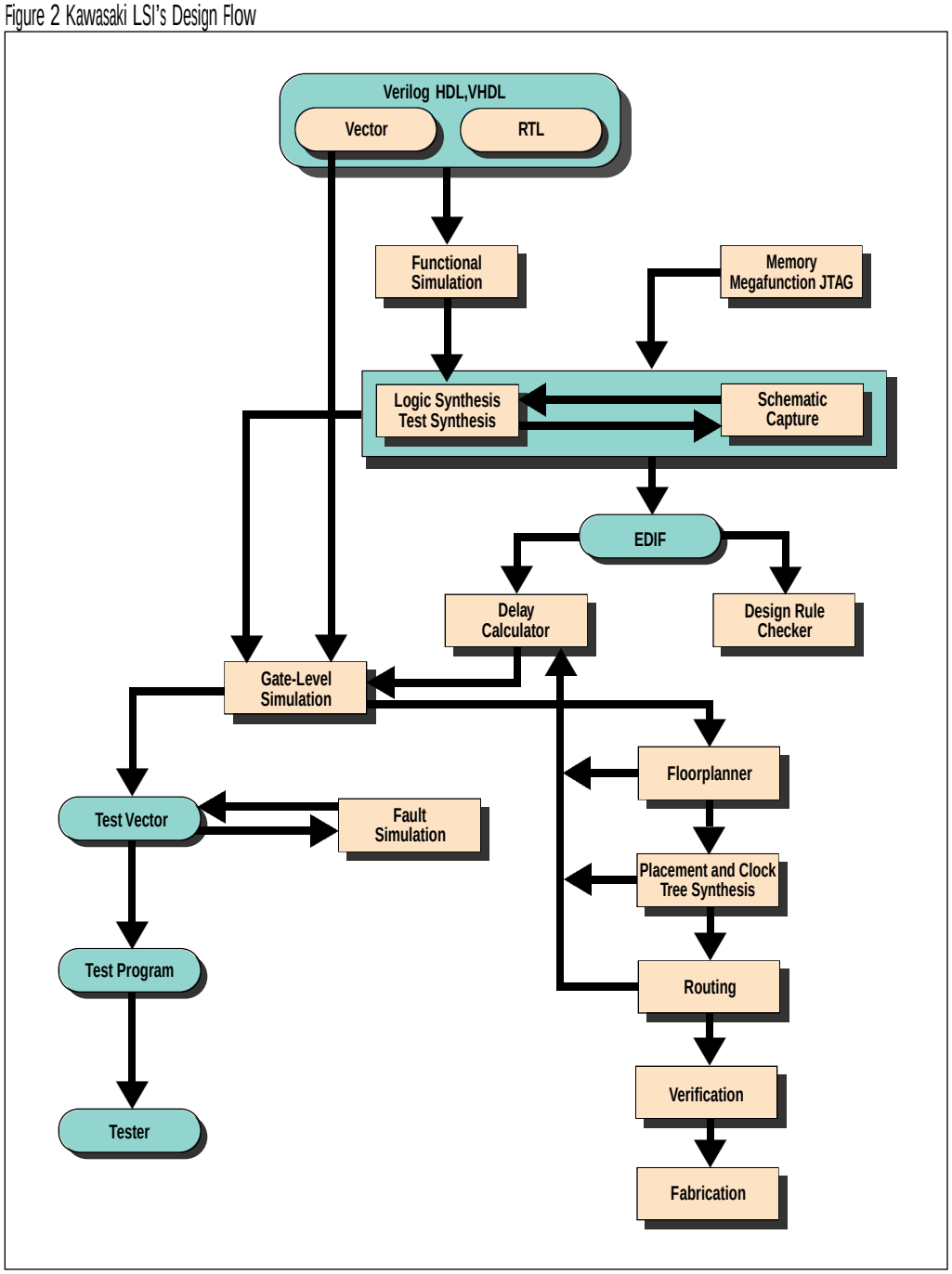
DESIGN SYSTEM

Kawasaki LSI's integrated topdown design flow is shown in Figure 2. It allows you to start either with VHDL or Verilog-HDL, or from the gate level, and choose from a wide assortment of schematic capture programs within Kawasaki LSI's design environment. Kawasaki LSI supports popular EDA tools, from companies such as Synopsys, Cadence, Mentor Graphics and ViewLogic.

Kawasaki LSI's Design Rule Checker and Delay Calculator can read EDIF netlists. Thus you have a choice of either VSS with an FTGS library, Verilog, QuickSim II, ViewSim, or another VHDL simulator with VITAL libraries, to read the delay files generated by the Delay Calculator for gate-level simulation. An accurate delay calculation method is provided, accounting for not only output-load-dependent delay, but also input-slew-rate-dependent off-set delay, input-slew-rate-dependent loading delay and interconnect delay due to the wire resistance. This advanced calculation methodology, coupled with control of the physical layout, results in the implementation of the highest performance designs in 0.5 micron technology.

The interfaces to these tools are industry-standard formats such as VHDL, EDIF, SDF, PDEF and WGL, making it very easy for designers to migrate their designs to Kawasaki LSI's technologies. The design sign-off golden simulator is Verilog, and verification is done using Dracula tools.

Figure 2 Kawasaki LSI's Design Flow



Electrical Characteristics

Tables 8 through 10 show the electrical characteristics of the KZ300GH/KZ300EH Series.

Table 8 Recommended Operating Conditions

Parameter	Symbol	Rating	Units
Power Supply Voltage	VDD	3.0~3.6	V
Ambient Temperature	Ta	-40~+85	°C

Table 9 Absolute Maximum Ratings

Parameter	Symbol	Rating	Units
Power Supply Voltage	VDD	-0.3~+4.0	V
Input Voltage	VIN	-0.3~VDD+0.3	V
	VIN (5V-tolerant)	-0.3~7.3	V
Output Current	IOUT	30	mA
Storage Temperature	TSTG	-55~+125	°C

Table 10 DC Electrical Characteristics

Symbol	Parameter	Conditions	Limits Min.	Limits Typ.	Limits Max.	Units
Vih	High Input Voltage	LVTTL	2.0	–	–	V
		5V-tolerant LVTTL	2.0	–	–	V
		3.3V PCI	0.5 x VDD	–	–	V
Vil	Low Input Voltage	LVTTL	–	–	0.8	V
		5V-tolerant LVTTL	–	–	0.8	V
		3.3V PCI	–	–	0.3xVDD	V
V+	High Input Voltage	LVTTL-Schmitt	–	2.1	2.6	V
V-	Low Input Voltage	LVTTL-Schmitt	0.5	0.9	–	V
Vh	Hysterisis Voltage	LVTTL-Schmitt	0.6	–	–	V
Iih	High Input Current	VIN=VDD	-10	–	+10	µA
Iil	Low Input Current	VIN=VSS	-10	–	+10	µA
Voh	High Output Voltage	Ioh=-2~-24mA	2.4	–	–	V
Vol	Low Output Voltage	Iol=2~24mA	–	–	0.4	V
Ioz	3-State Leak Current	Voh=VSS	-10	–	+10	µA
		Vol=VDD	-10	–	+10	µA
Ipu	Active Pull-Up Current	VIN=VSS	-25	-66	-160	µA
Ipd	Active Pull-Down Current	VIN=VDD	25	66	160	µA
Idds	Static Stand-By Current	–	–	–	450*	µA

*The number is design dependent.
ESD protection:>2000V using MIL STD-883D 3015.6 and EIAJ:ED4701 C-111, B standards
Latch-up immunity:300mA Injection Current (Room Temp) using JEDEC No. 17 Standard

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