SYNCHRONOUS DUAL-PORT BURST SRAM

64K/32K/16K x 16/18
128K/64K/32K x 8/9

+3.3V SUPPLY, BURST COUNTER

FEATURES

- True Dual-Ported memory cells which allow simultaneous access of the same memory location.
- Fast access times: 4.5ns, 5.0ns, and 6.0ns
- Fast clock speed: 125, 100, 83, and 66MHz
- Fast OE# access times: 4.5ns, 5.0ns, and 6.0ns
- Address, data and control registers
- 3.3V ± 0.3V power supply
- 5V tolerant inputs except I/O's
- Address burst counters enable and reset capabilities
- Dual Chip Enables for easy depth expansion
- Fully synchronous interface on both ports
- 3 operating modes: Flow-Through, Pipelined, and Burst
- Dual chip enables for depth expansion
- BYTE ENABLE controls for x16 and x18 devices
- Internally self-timed WRITE CYCLE
- Automatic power-down
- Commercial and Industrial temperature ranges
- Available in 100-pin TQFP package

MARKING

- Clock Cycle Timing

8ns (125MHz)	-8
10ns (100MHz)	-10
12ns (83MHz)	-12
15ns (67MHz)	-15

Configurations

16K x 16	GVT8116C16
16K x 18	GVT8116C18
32K x 16	GVT8132C16
32K x 18	GVT8132C18
64K x 16	GVT8164C16
64K x 18	GVT8164C18
32K x 8	GVT8132C8
32K x 9	GVT8132C9
64K x 8	GVT8164C8
64K x 9	GVT8164C9
128K x 8	GVT81128C8
128K x 9	GVT81128C9

Package Versions

100-pin TQFP	T

GNERAL DESCRIPTION

The GVT8116C16/18, GVT8132C16/18, and GVT8164C16/18 are high speed synchronous 16K, 32K and 64K x 16/18 dual-port static RAMs; the GVT8132C8/9, GVT8164C8/9, and GVT81128C8/9 are high speed synchronous 32K, 64K, and 128K x 8/9 dual-port static RAMs. Dual-port memory cells are provided, permitting independent, simultaneous access for reads and writes to any address location in these devices. Registers on address, data, and control inputs allow for minimal set-up and hold times. All synchronous inputs are gated by registers controlled by a positive-edge-triggered clock input (CLK).

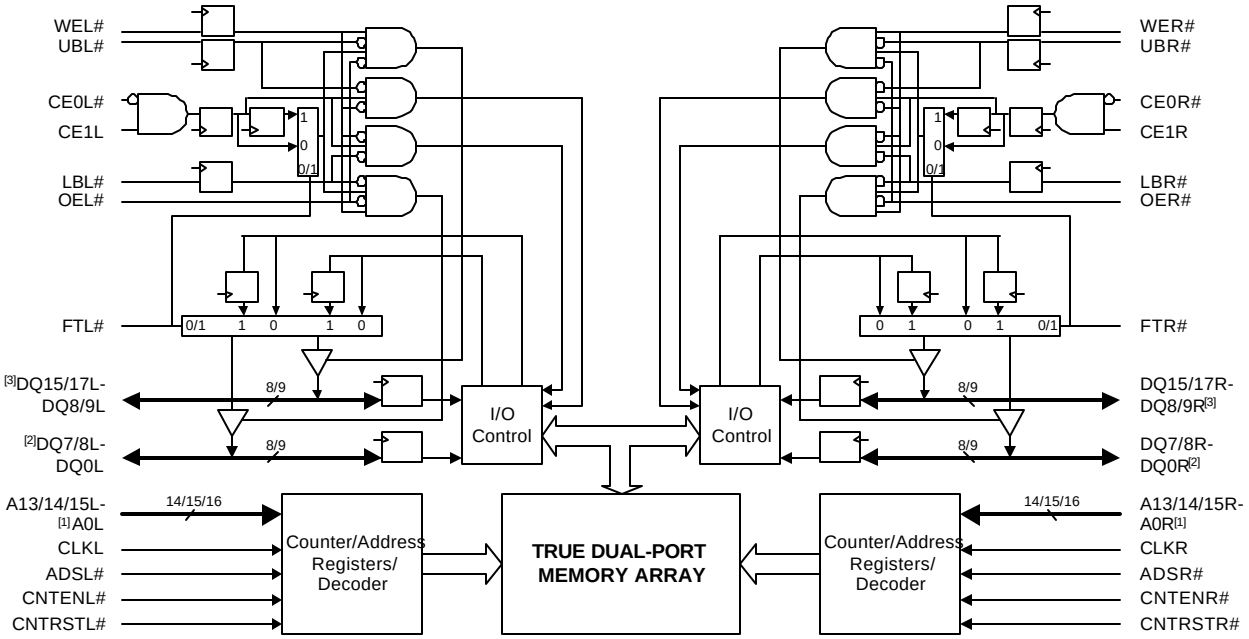
Each port contains a burst counter on the input address register for internal burst operation. The address burst counter can be incremented, suspended or reset to zero, depending upon the CNTEN# and CNTRST# pins.

In the pipelined mode, output data will be valid after one cycle delay. Flow-through mode can be used to bypass the pipelined output register to eliminate one cycle latency. Pipelined or flow-through mode is selected by the FT# pin.

The port of the device is activated by asserting LOW on CE0# and HIGH on CE1 at the rising edge of CLK. By asserting HIGH on CE0# or LOW on CE1 at the rising edge of CLK signal will power down the internal circuitry to reduce the static power consumption. The use of multiple Chip Enables allows easier banking of multiple chips for depth expansion configurations.

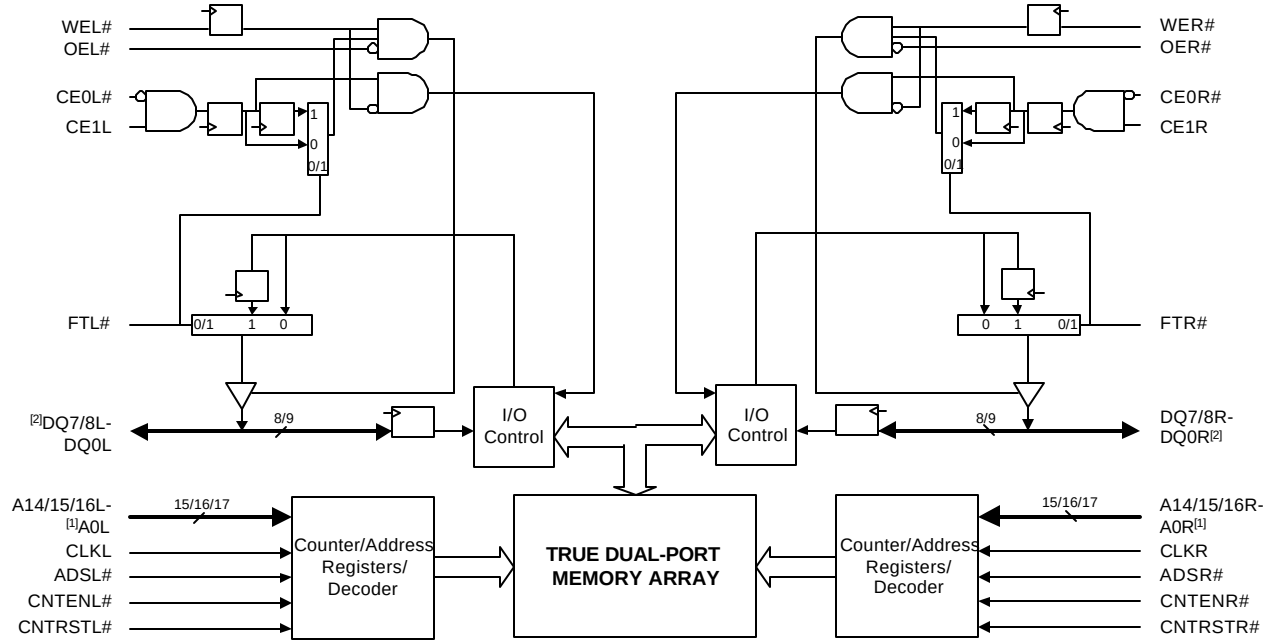
Counter enable inputs are provided to utilize the internal address generated by the internal counter for fast memory applications. A port's address burst conter is loaded with the port's address strobe (ADS#). When the port's count enable (CNTEN#) is asserted, the address burst counter will increment on each LOW-to-HIGH transition of the port's clock signal. This will read/write one word from/into each successive address location until CNTEN is deasserted. The address burst counter can address the entire memory array and will loop back to the start. Counter reset (CNTRST#) is used to reset the address burst counter.

16K/32K/64K X 16/18 FUNCTIONAL BLOCK DIAGRAM



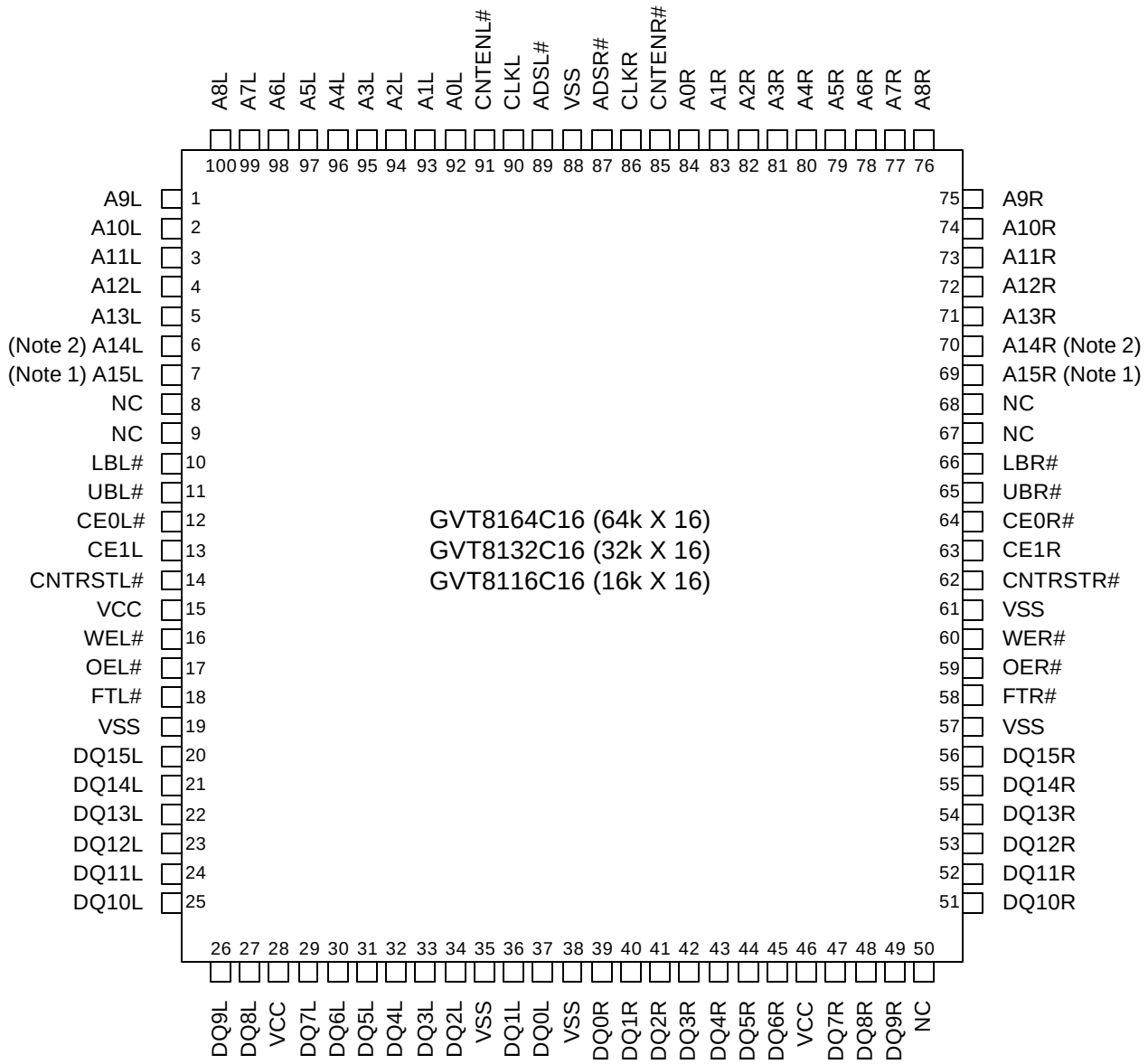
Notes:
1. A13-A0 for 16K devices; A14-A0 for 32K devices; A15-A0 for 64K devices.
2. DQ7-DQ0 for x16 devices; DQ8-DQ0 for x18 devices.
3. DQ15-DQ8 for x16 devices; DQ17-DQ9 for x18 devices.

32K/64K/128K X 8/9 FUNCTIONAL BLOCK DIAGRAM



Notes:
1. A14-A0 for 32K devices; A15-A0 for 64K devices; A16-A0 for 128K devices.
2. DQ7-DQ0 for x8 devices; DQ8-DQ0 for x9 devices.

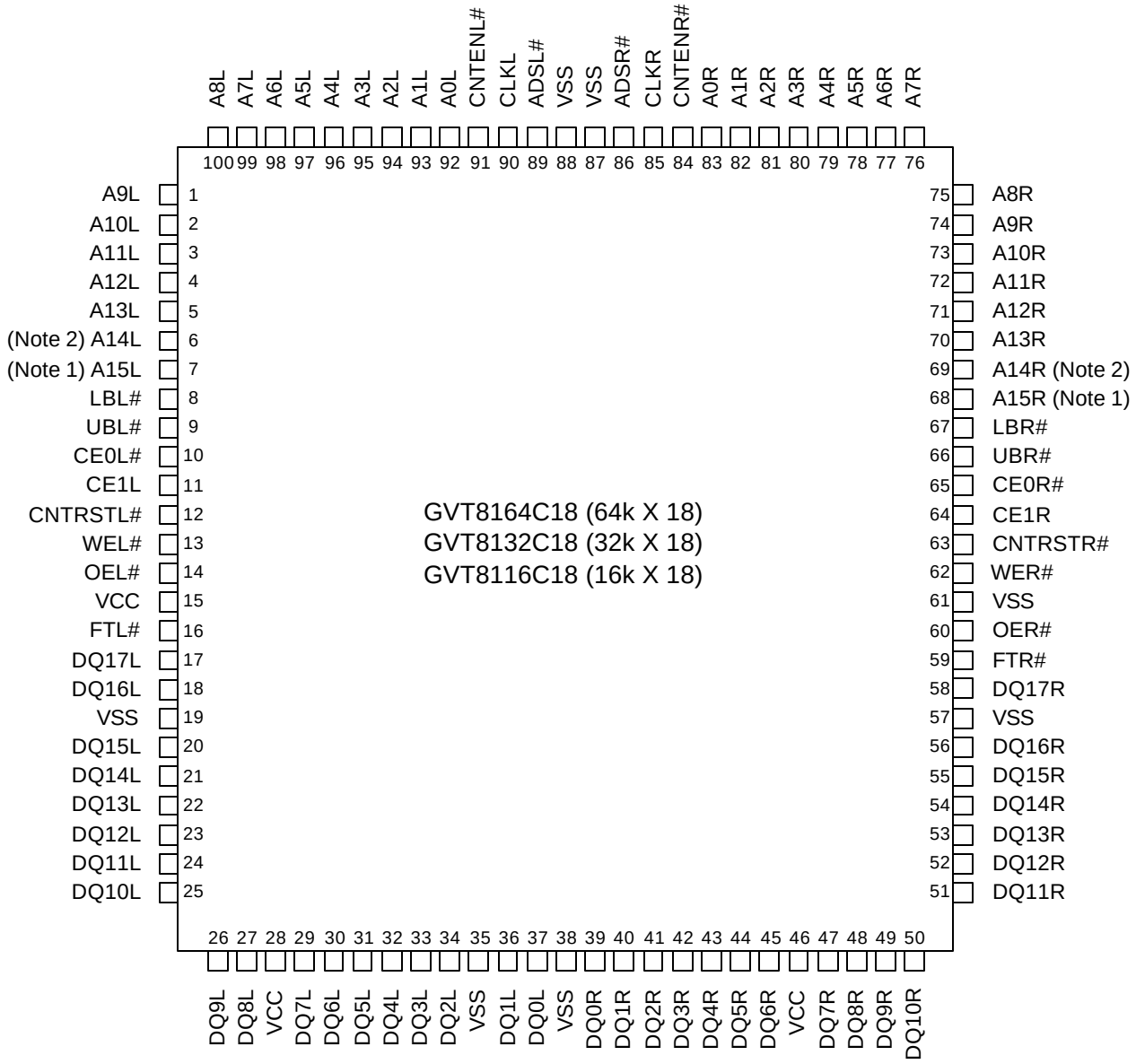
16K/32K/64K X 16, 100-PIN TQFP (Top View)



Notes:

1. These pins are NC for 32K x 16 and 16K x 16 devices.
2. These pins are NC for 16K x 16 devices.

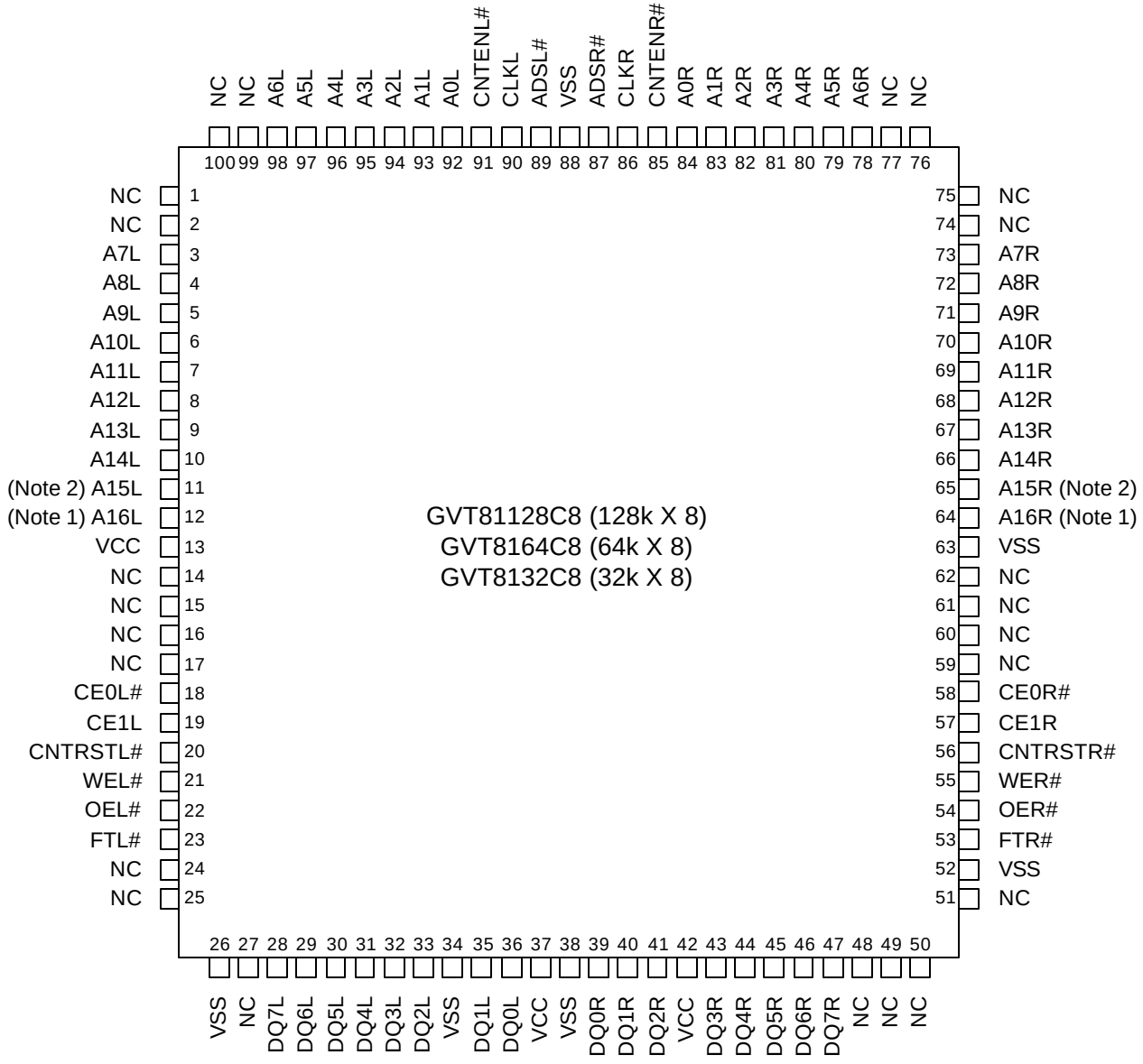
16K/32K/64K X 18, 100-PIN TQFP (Top View)



Notes:

1. These pins are NC for 32K x 18 and 16K x 18 devices.
2. These pins are NC for 16K x 18 devices.

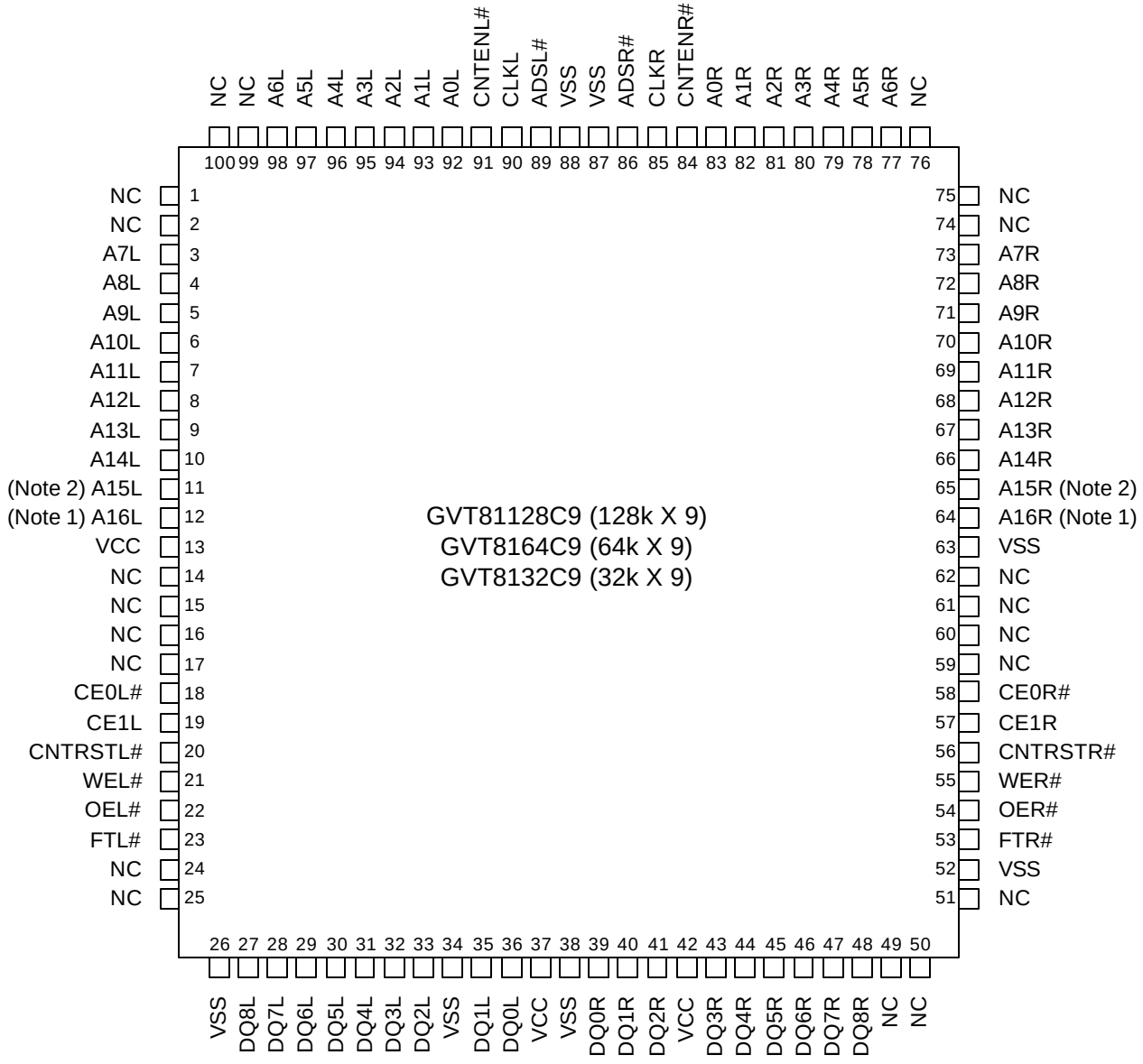
32K/64K/128K X 8, 100-PIN TQFP (Top View)



Notes:

1. These pins are NC for 64K x 8 and 32K x 8 devices.
2. These pins are NC for 32K x 8 devices.

32K/64K/128K X 9, 100-PIN TQFP (Top View)



Notes:

1. These pins are NC for 64K x 9 and 32K x 9 devices.
2. These pins are NC for 32K x 9 devices.

PIN DESCRIPTIONS

Left Port	Right Port	TYPE	DESCRIPTION
A0L - A16L	A0R-A16R	Input-Synchronous	Address Inputs: A0-A13 for 16K; A0-A14 for 32K; A0-A15 for 64K; and A0-A16 for 128K devices.
ADSL#	ADSR#	Input-Synchronous	Adress Strobe Input: Used as an address qualifier. This signal should be asserted LOW to access the part using an externallly supplied address. Asserting this signal LOW also loads the burst counter with the address presented on the address pins.
CE0L#, CE1L	CE0R#, CE1R	Input-Synchronous	Chip Enable Inputs: To select either the left or right port, both CE0# and CE1 must be asserted to their active states (CE0# < V_{IL} and CE1 > V_{IH}).
CLKL	CLKR	Input-Synchronous	Clock Signal: This input can be free running or stropped. Maximum clock input rate is f_{MAX}.
CNTENL#	CNTENR#	Input-Synchronous	Counter Enable Input: Asserting this signal LOW increments the burst address counter of its respective port on each rising edge of CLK. CNTEN# is disabled if ADS# or CNTRST# is asserted LOW.
CNTRSTL#	CNTRSTR#	Input-Synchronous	Counter Reset Input: Asserting this signal LOW resets the burst address counter of its respective port to zero. CNTRST# is not disabled by asserting ADS# or CNTEN#.
DQ17L - DQ0L	DQ17R - DQ0R	input-Output	Data Bus Inputs/Outputs: DQ7-DQ0 for x 8 devices; DQ8-DQ0 for x 9 devices; DQ15-DQ0 for x 16 devices; DQ17-DQ0 for x 18 devices.
WEL#	WER#	input-Synchronous	Read/Write Enable Input: This signal is asserted LOW to write to the dual port memory array. For read operations, assert this pin HIGH.
UBL#	UBR#	input-Synchronous	Upper Byte Select Input: This signal is asserted LOW to write to or read from the upper byte of the dual port memory array. This signal only applies to x16 and x18 devices. For x16 devices, DQ15-DQ8 is upper byte. For x18 devices, DQ17-DQ9 is upper byte.
LBL#	LBR#	input-Synchronous	Lower Byte Select Input: This signal is asserted LOW to write to or read from the lower byte of the dual port memory array. This signal only applies to x16 and x18 devices. For x16 devices, DQ7-DQ0 is lower byte. For x18 devices, DQ8-DQ0 is lower byte.
OEL#	OER#	input-Asynchronous	Output Enable Input: This signal must be asserted LOW to enable the I/O data pins during read operations.
FTL#	FTR#	Input-Static	Flow-Through/Pipelined Select Input: For flow-through mode operation, assert this pin LOW. For pipeline mode operation, assert this pin HIGH.
VCC		Supply	Power Supply: From +3.0V to +3.6V.
VSS		Ground	Ground: GND.
NC		-	No Connect: These pins are not internally connected. User can connect them to VCC, VSS or leave them floating.

TRUTH TABLE I --READ/WRITE AND ENABLE CONTROL (1, 2, 3, 4, 5)

OE#	CLK	CE0#	CE1	UB#	LB#	WE#	Upper Byte	Lower Byte	OPERATION
X	L-H	H	X	X	X	X	High-Z	High-Z	Deselected (6)
X	L-H	X	L	X	X	X	High-Z	High-Z	Deselected (6)
X	L-H	L	H	H	H	X	High-Z	High-Z	Both Bytes Deselect
X	L-H	L	H	L	H	L	X	L-H	Write to Upper Byte
X	L-H	L	H	H	L	L	X	L-H	Write to Lower Byte
X	L-H	L	H	L	L	L	L	L-H	Write to Both Bytes
L	L-H	L	H	L	H	H	H	L-H	Read from Upper Byte (6)
L	L-H	L	H	H	L	H	H	L-H	Read from Lower Byte (6)
L	L-H	L	H	L	L	H	H	L-H	Read from Both Bytes (6)
H	L-H	L	H	L	L	X	X	L-H	Output Disabled

TRUTH TABLE II --ADDRESS COUNTER CONTROLOPERATION (1, 2, 7, 8, 9)

ADDRESS	PREVIOUS ADDRESS	CLK	ADS#	CNTEN#	CNTRST#	DQ	MODE	OPERATION
X	X	L-H	X	X	L	Q_0	Reset	Counter Reset to Address 0
A_n	X	L-H	L	X	H	Q_n	Load	Address Loaded into Counter
X	A_n	L-H	H	H	H	Q_n	Hold	External Address Blocked Counter Disabled
X	A_n	L-H	H	L	H	Q_{n+1}	Increment	Internal Address Generated Counter Enabled

Note:

1. “X” means “don’t care.” “H” means logic HIGH. “L” means logic LOW.
2. UB# and LB# are for x16 and x18 devices only.
3. ADS#, CNTEN#, CNTRST# = “don’t care.”
4. OE# is an asynchronous input signal. All inputs except OE# must meet setup and hold times around the rising edge (LOW to HIGH) of CLK.
5. This device contains circuitry that will ensure the outputs will be in High-Z during power-up.
6. When CE0# or CE1 changes state in the pipelined mode, deselection and read happen in the following clock cycle.
7. CE0# and OE# are logic LOW; CE1 and WE# are logic HIGH. UB# and LB# are logic LOW for x16 and x18 devices.
8. Data shown for flow-through mode; pipelined mode output will be delayed by one cycle.
9. Counter operation is independent of CE0# and CE1.

ABSOLUTE MAXIMUM RATINGS*

Voltage on VCC Supply Relative to VSS.....-0.5V to +4.6V
V_{IN} .....-0.5V to VCC+0.5V
Storage Temperature (plastic) .....-55°C to +150°
Junction Temperature .....+150°
Power Dissipation 1.0W
Short Circuit Output Current 50mA

*Stresses greater than those listed uunder "Absolute Maximum Ratings" may cause permanent damage to the device.This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING RANGE

RANGE	AMBIENT TEMPERATURE	VCC
Commercial	0°C to +70°C	3.3V ± 0.3V
Industrial	-40°C to +85°C	3.3V ± 0.3V

DC ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

(Over the Operating Range)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage	Data Inputs (DQx)	V_{IHD}	2.2	VCC+0.3	V	1,2
	All Other Inputs	V_{IH}	2.2	4.6	V	1,2
Input Low (Logic 0) Voltage		V_{II}	-0.5	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ VCC	IL_I	-5	5	uA	
Output Leakage Current	Output(s) disabled, 0V ≤ V_{OUT} ≤ VCC	IL_O	-10	10	uA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1, 9
Output Low Voltage	I_{OL} = 4.0mA	V_{OL}		0.4	V	1, 9
Supply Voltage		VCC	3.0	3.6	V	1

DESCRIPTION	CONDITIONS	SYM	RANGE	TYP	-8	-10	-12	-15	UNITS	NOTES
Power Supply Current: Operating	Device selected; all inputs ≤ V_{IL} or ≥ V_{IH}; VCC =MAX; f = f_{MAX}; outputs open	Icc	Com'l	120	450	350	275	230	mA	3, 10, 11
			Indust.	120	-	380	350	300	mA	
Standby Current (Both Ports TTL Level)	Device deselected for both ports; CE1 ≤ V_{IL} or CE0# ≥ V_{IH}; f = f_{MAX}; VCC = MAX	I_{SB1}	Com'l	20	120	95	85	75	mA	10, 11
			Indust.	20	-	120	95	85	mA	
Standby Current (One Port TTL Level)	Device deselected for one port; CE1 ≤ V_{IL} or CE0# ≥ V_{IH}; f = f_{MAX}; VCC = MAX	I_{SB2}	Com'l	85	280	220	175	155	mA	10, 11
			Indust.	85	-	230	185	165	mA	
Standby Current (Both Ports CMOS Level)	Device deselected for both ports; CE1 ≤ VSS +0.2 or CE0# ≥ VCC - 0.2; f = 0; VCC = MAX	I_{SB3}	Com'l	5	10	10	10	10	mA	10, 11
			Indust.	5	-	10	10	10	mA	
Standby Current (One Port CMOS Level)	Device deselected for one port; CE1 ≤ VSS +0.2 or CE0# ≥ VCC - 0.2; f = f_{MAX}; VCC = MAX	I_{SB4}	Com'l	75	145	135	125	115	mA	10, 11
			Indust.	75	-	145	135	125	mA	

AC ELECTRICAL CHARACTERISTICS (Over the Operating Range) (Note 5)

DESCRIPTION		-8 125MHz		-10 100MHz		-12 83MHz		-15 67MHz			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Clock											
Clock frequency (Flow-Through)	^{f}MAX1		83		75		60		50	MHz	
Clock cycle time (Flow-Through)	^{t}KC1	12		13.3		16.6		20		ns	
Clock HIGH time (Flow-Through)	^{t}KH1	5.0		5.0		6.0		7.0		ns	
Clock LOW time (Flow-Through)	^{t}KL1	5.0		5.0		6.0		7.0		ns	
Clock frequency (Pipelined)	^{f}MAX2		125		100		83		67	MHz	
Clock cycle time (Pipelined)	^{t}KC2	8.0		10		12		15		ns	
Clock HIGH time (Pipelined)	^{t}KH2	3.2		4.0		5.0		6.0		ns	
Clock LOW time (Pipelined)	^{t}KL2	3.2		4.0		5.0		6.0		ns	
Clock rise time	^{t}R		3.0		3.0		3.0		3.0	ns	
Clock fall time	^{t}F		3.0		3.0		3.0		3.0	ns	
Output Times											
Clock to output valid (Flow-Through)	^{t}CD1		11		12.5		15		18	ns	
Clock to output valid (Pipelined)	^{t}CD2		4.5		5.0		6.0		6.0	ns	
Clock to output invalid	^{t}DC	2.0		2.0		2.0		2.0		ns	
Clock to output in Low-Z	^{t}KQLZ	2.0		2.0		2.0		2.0		ns	4, 6,7
Clock to output in High-Z	^{t}KQHZ	2.0	4.0	2.0	4.0	2.0	4.0	2.0	5.0	ns	4, 6,7
OE to output valid	^{t}OEQ		4.5		5.0		6.0		6.0	ns	
OE to output in Low-Z	^{t}OELZ	2.0		2.0		2.0		2.0		ns	4, 6,7
OE to output in High-Z	^{t}OEHZ	1.0	4.0	1.0	4.0	1.0	4.0	1.0	5.0	ns	4, 6,7
Setup Times											
Address, Controls and Data In	^{t}S	2.5		2.5		2.5		3.5		ns	8
Hold Times											
Address, Controls and Data In	^{t}H	0.0		0.0		0.0		1.0		ns	8
Port to Port Delay Times											
Write port clock HIGH to output valid at Read port	^{t}CWDD		20		30		35		40	ns	
Clock to clock setup time	^{t}CCS		5.0		7.0		10		15	ns	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	TYP	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz VCC = 3.3V	C_I	7	8	pF	4
Input/Output Capacitance (DQ)		C_O	7	8	pF	4

AC TEST CONDITIONS FOR 3.3V I/O

Input pulse levels	0V to 3.0V
Input rise and fall times	2ns
Input timing reference levels	1.4V
Output reference levels	1.4V
Output load	See Figures 1

OUTPUT LOADS FOR 3.3V I/O

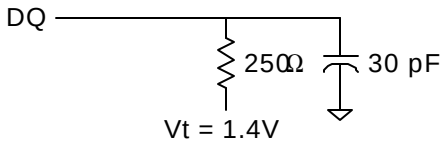


Fig. 1 OUTPUT LOAD EQUIVALENT

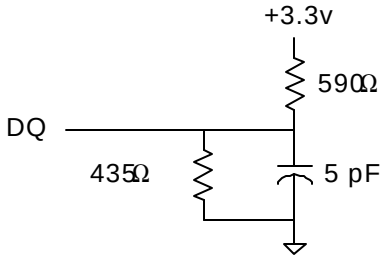


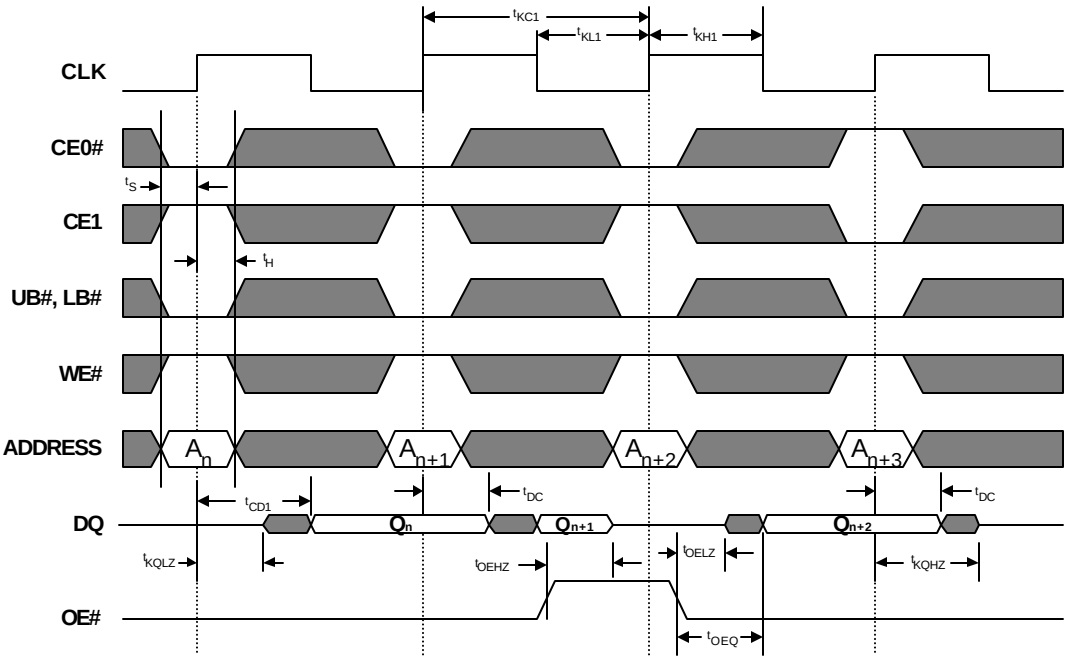
Fig. 2 OUTPUT LOAD EQUIVALENT

NOTES

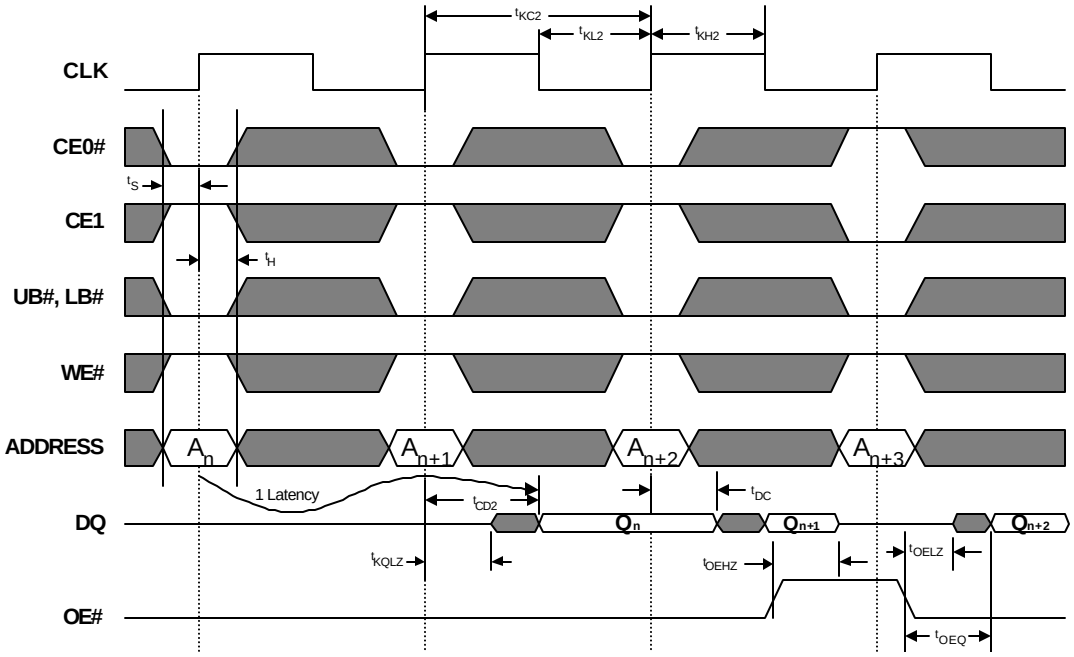
1. All voltages referenced to VSS (GND).
2. Overshoot: $V_{IH} \leq +6.0V$ for $t \leq {}^tKC/2$.
   Undershoot: $V_{IL} \leq -2.0V$ for $t \leq {}^tKC/2$
3. I_{cc} is given with no output current. I_{cc} increases with greater output loading and faster cycle times.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. Output loading is specified with CL=5pF as in Fig. 2.
7. At any given temperature and voltage condition, ${}^tKQHZ$ is less than ${}^tKQLZ$ and ${}^tOEHZ$ is less than ${}^tOELZ$.
8. This is a synchronous device. All synchronous inputs must meet specified setup and hold time, except for “don’t care” as defined in the truth table.
9. AC I/O curves are available upon request.
10. “Device Deselected” means the device is in POWER -DOWN mode as defined in the truth table. “Device Selected” means the device is active.
11. Typical values are measured at 3.3V, 25°C and 20ns cycle time.

SWITCHING WAVEFORMS

Read Cycle for Flow-Through Output (FT#= V_{IL}) [1, 2, 4, 5]



Read Cycle for Pipelined Output (FT#= V_{IH}) [1, 2, 3, 4, 5]

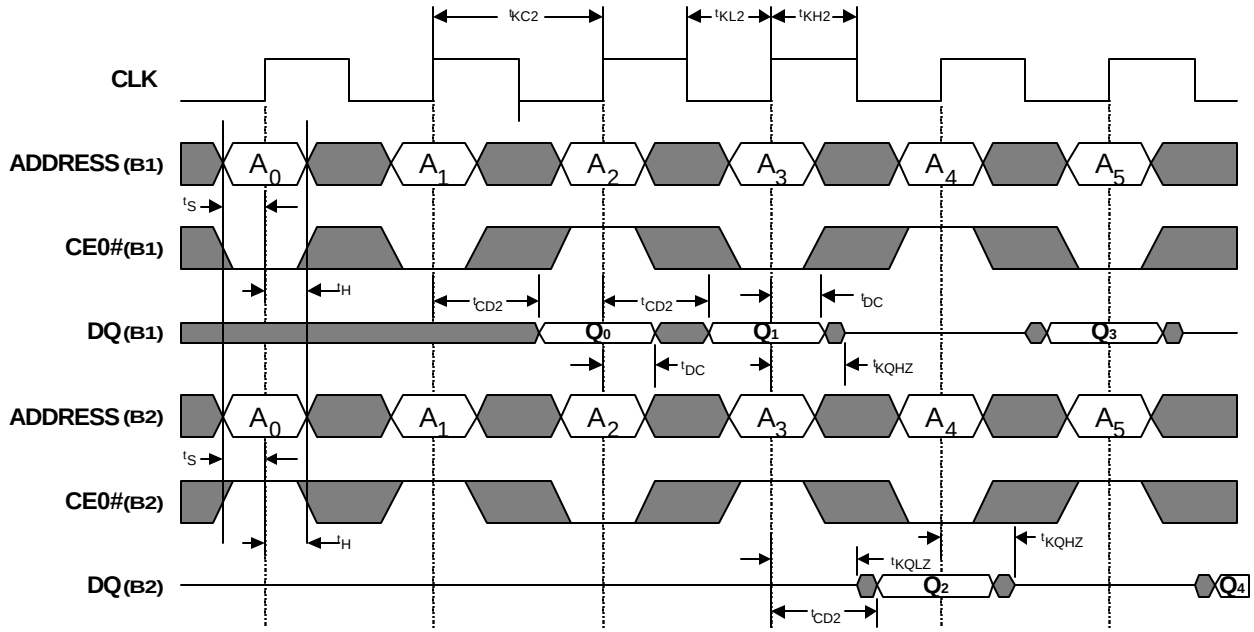


Note:

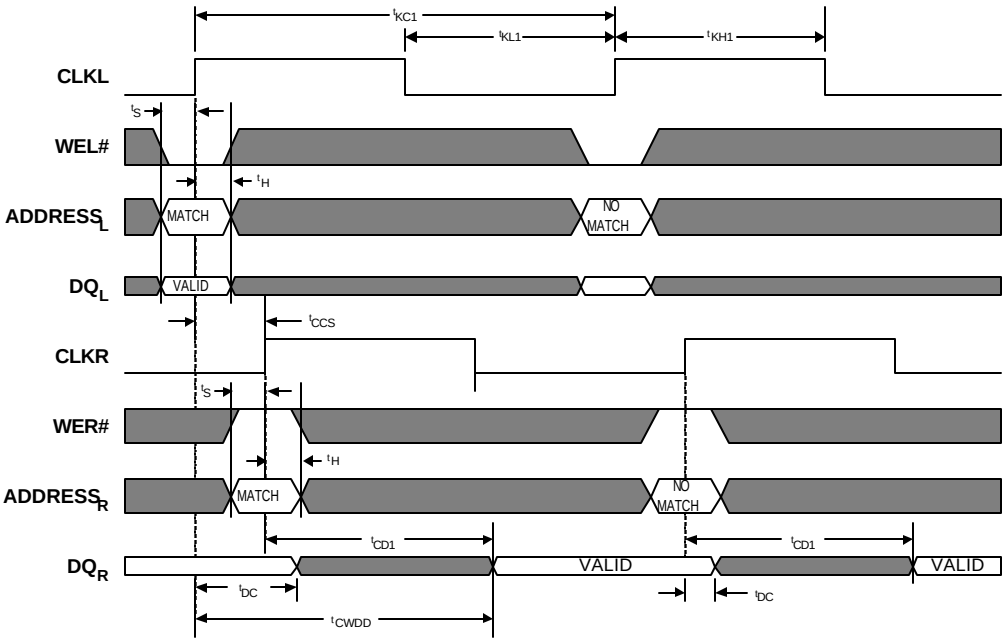
1. OE# is asynchronous signal; all other inputs are synchronous to the rising edge of clock (CLK).
2. ADS# = V_{IL}; CNTEN# and CNTRST# = V_{IH}.
3. The output is disabled (high impedance state) by CE0#=V_{IH} or CE =V_{IL} following the next rising edge of the clock.
4. Addresses do not have to be accessed sequentially since ADS#=V_{IL} constantly loads the addresses on the rising edge of the CLK. Numbers are for reference only.
5. UB# and LB# are for x16 and x18 devices only.

SWITCHING WAVEFORMS (continued)

Bank Select Pipelined Read (FT#= V_{IH}) [1, 2]



Left Port Write to Flow-Through Right Port Read (FTR#= V_{IL}) [3, 4, 5, 6]

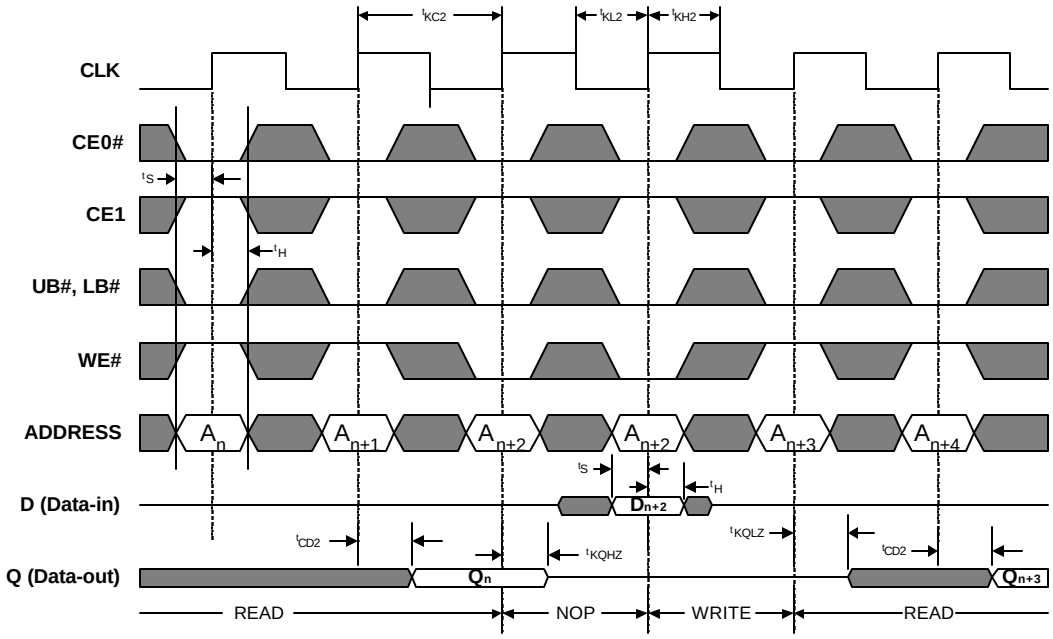


Note:

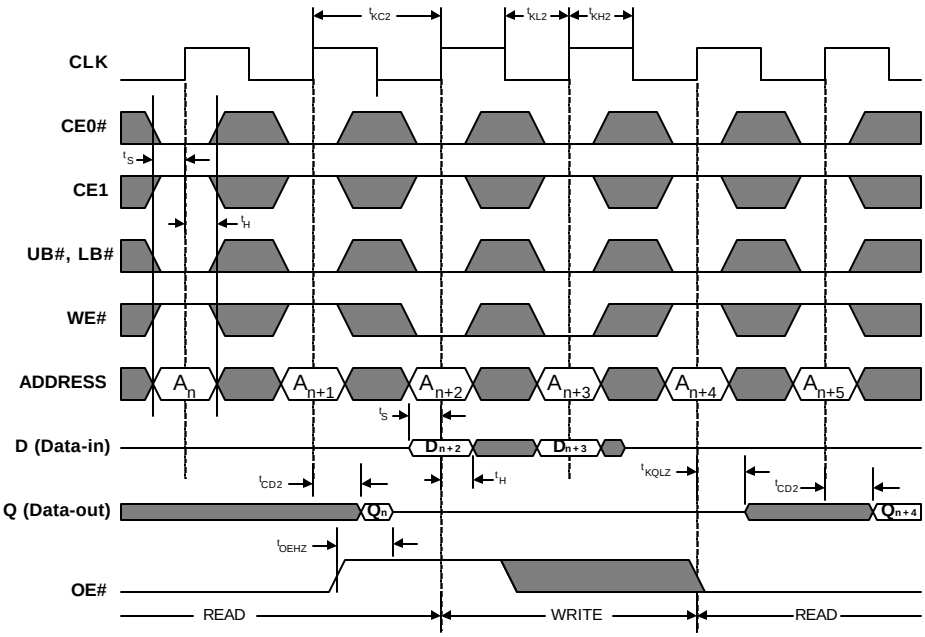
1. In the depth expansion example, B1 represents Bank #1 and B2 represents Bank #2; each bank consists of one Galvantech dual-port device from this datasheet. $ADDRESS_{(B1)}$=$ADDRESS_{(B2)}$.
2. OE# and ADS# = V_{IL}; $CE1_{(B1)}$, $CE1_{(B2)}$, WE#, CNTEN# and CNTRST# = V_{IH}. UB# and LB# = V_{IL} for x16 & x18 devices.
3. The same waveforms apply for a right port write to Flow-Through left port read.
4. CE0# and ADS# = V_{IL}; CE1, CNTEN# and CNTRST# = V_{IH}. UB# and LB# = V_{IL} for x16 & x18 devices.
5. OE# = V_{IL} for the right port, whcih is being read from, OE# = V_{IH} for the left port, whcih is being written to.
6. If $t_{CCS} \leq$ maximum specified, then data from right port READ is not valid until the maximum specified for t_{CWDD}. If t_{CCS} > maximum specified, then data is not valid until $t_{CCS} + t_{CD1}$. t_{CWDD} does not apply in this case.

SWITCHING WAVEFORMS (continued)

Pipelined Read-to-Write-to-Read (FT#= V_{IH}; OE#= V_{IL}) [1, 2, 3, 4]



Pipelined Read-to-Write-to-Read with OE# Control (FT#= V_{IH}) [1, 2, 3, 4]

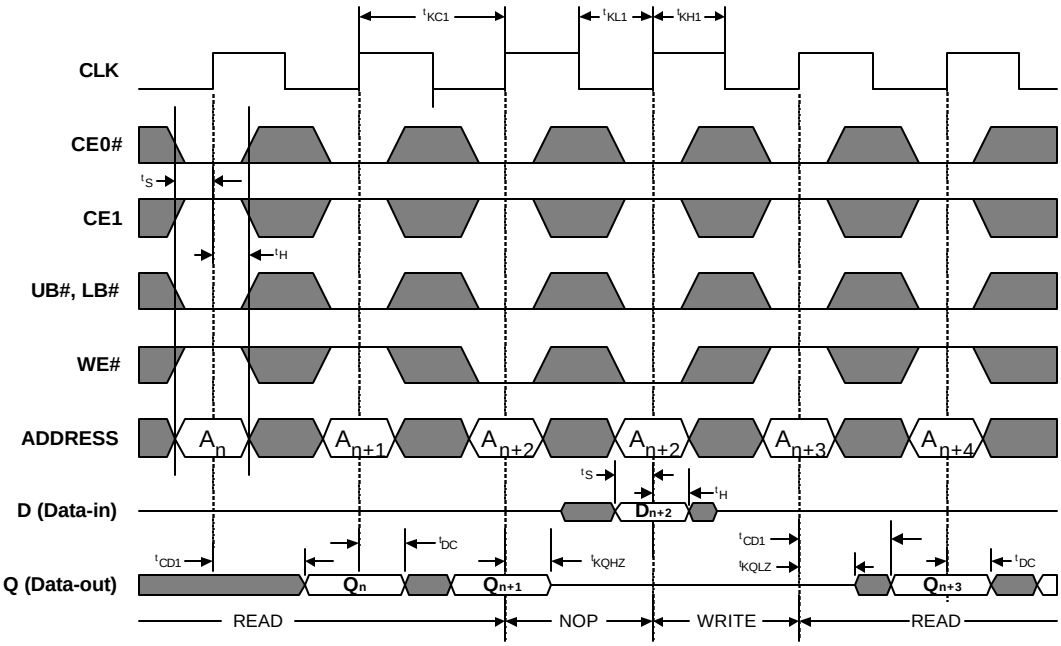


Note:

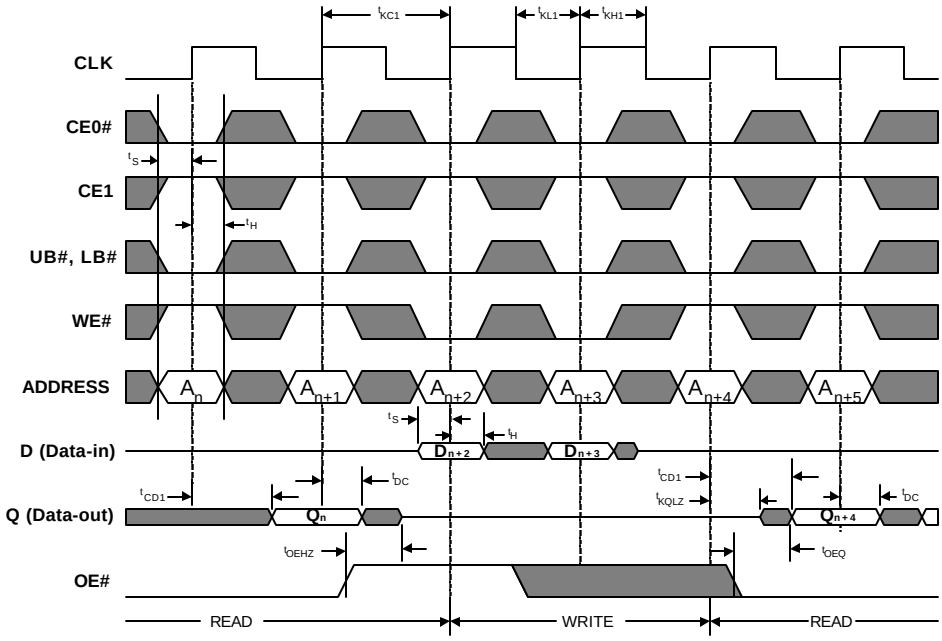
1. Addresses do not have to be accessed sequentially since ADS#=V_{IL} constantly loads the addresses on the rising edge of the CLK. Numbers are for reference only.
2. Output state (HIGH, LOW, or High-Impedance) is determined by the previous cycle control signals.
3. CE0# and ADS# = V_{IL}; CE1, CNTEN# and CNTRST# = V_{IH}.
4. during "No Operation", data in memory at the selected address may be corrupted and should be re-written to ensure data integrity.

SWITCHING WAVEFORMS (continued)

Flow-Through Read-to-Write-to-Read (FT#= V_{IL}; OE#= V_{IL}) [1, 2, 3, 4, 5]



Flow-Through Read-to-Write-to-Read with OE# Control (FT#= V_{IL}) [1, 2, 3, 4, 5]

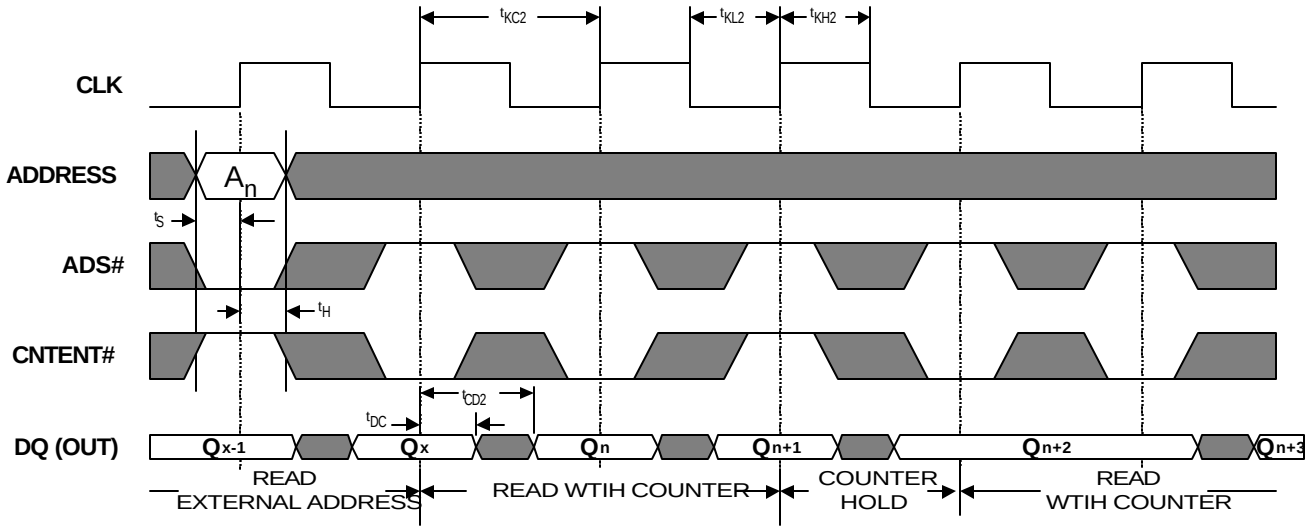


Note:

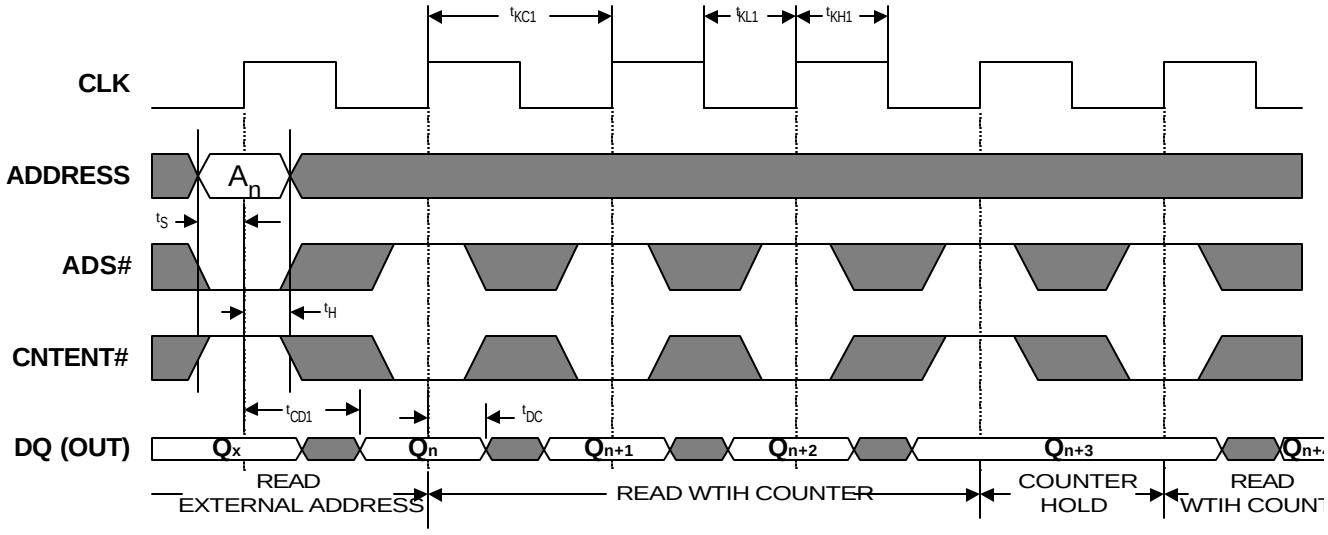
1. ADS# = V_{IL}; CNTEN# and CNTRST# = V_{IH}.
2. Addresses do not have to be accessed sequentially since ADS#=V_{IL} constantly loads the addresses on the rising edge of the CLK. Numbers are for reference only.
3. Output state (HIGH, LOW, or High-Impedance) is determined by the previous cycle control signals.
4. CE0# and ADS# = V_{IL}; CE1, CNTEN# and CNTRST# = V_{IH}.
5. during “No Operation”, data in memory at the selected address may be corrupted and should be re-written to ensure data integrity.

SWITCHING WAVEFORMS (continued)

Pipelined Read with Address Counter Advance (FT#= V_{IH}) [1]



Flow-Through Read with Address Counter Advance (FT#= V_{IL}) [1]

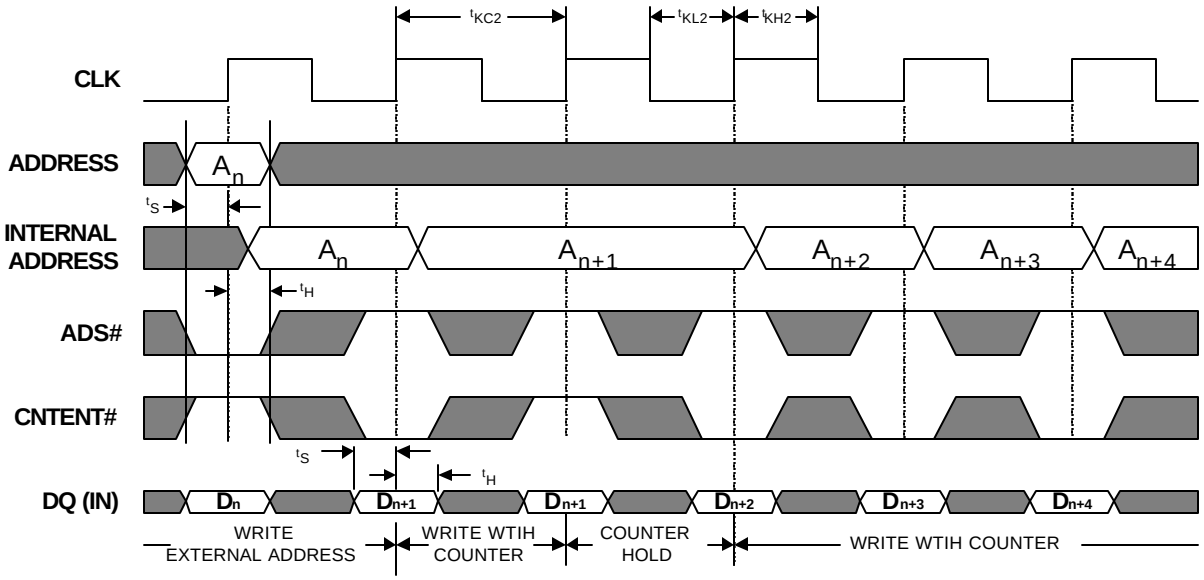


Note:

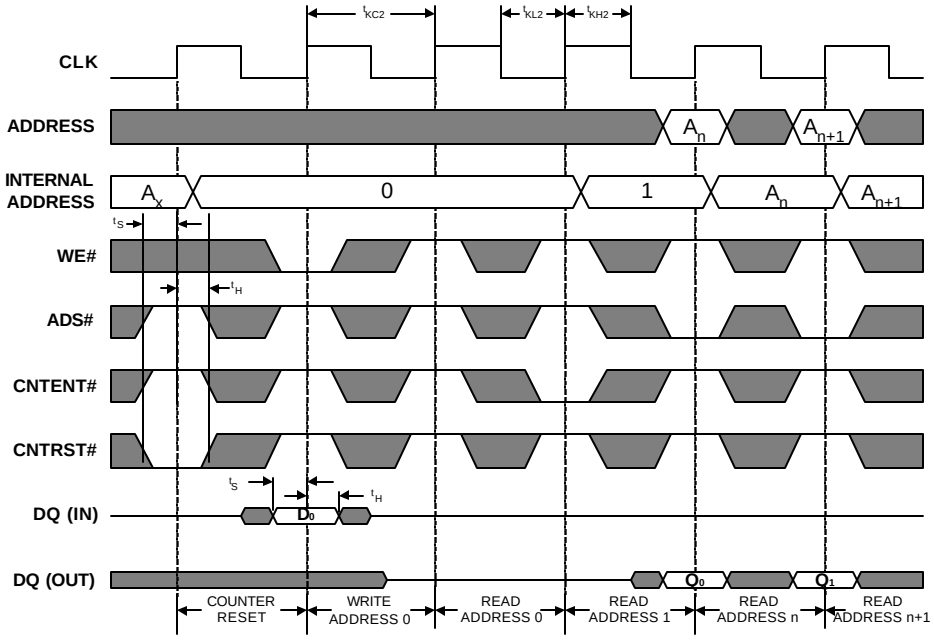
1. CE0# and OE# = V_{IL}; CE1, WE# and CNTRST# = V_{IH}.

SWITCHING WAVEFORMS (continued)

Write with Address Counter Advance (Flow-Through or Pipelined Outputs) [1, 2]



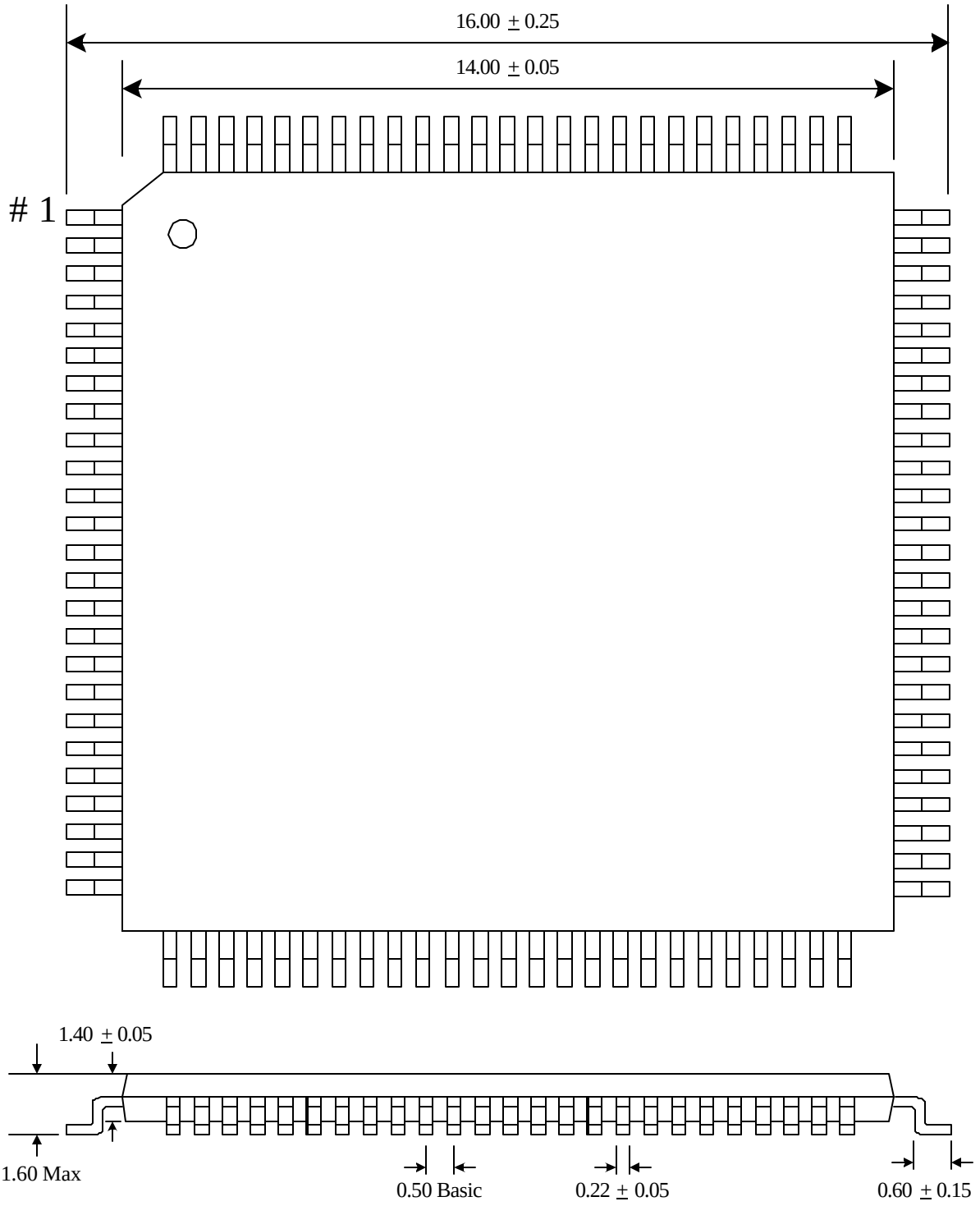
Counter Reset with Pipelined Outputs (FT#= V_{IH}) [3, 4, 5, 6]



Note:

1. CE0# and WE# = V_{IL}; CE1and CNTRST# = V_{IH}.
2. The "Internal Address" is equal to the "External Address" when ADS# = $V_{IL}$and is equal to the counter output when ADS# = V_{IH}.
3. Addresses do not have to be accessed sequentially since ADS#=V_{IL} constantly loads the addresses on the rising edge of the CLK. Numbers are for reference only.
4. Output state (HIGH, LOW, or High-Impedance) is determined by the previous cycle control signals.
5. CE0# and WE# = V_{IL}; CE1and CNTRST# = V_{IH}.
6. No dead cycle exists during counter reset. A READ or WRITE cycle may be coincidental with the counter reset.

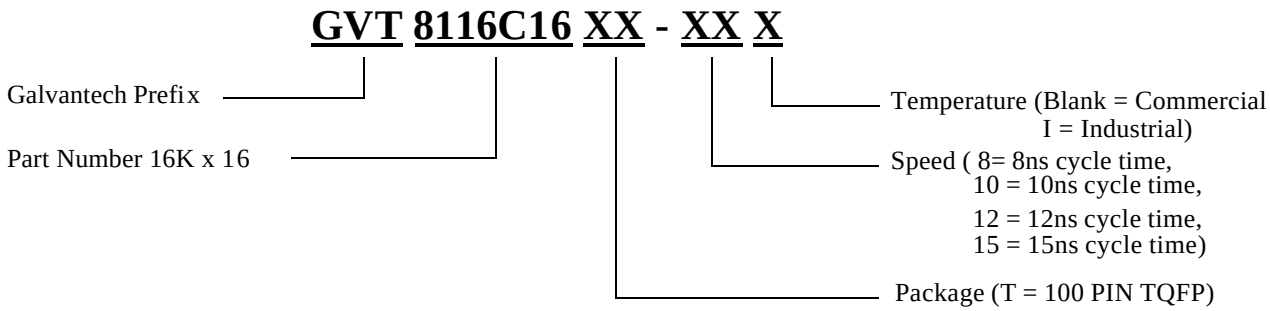
100 Pin TQFP Package Dimensions



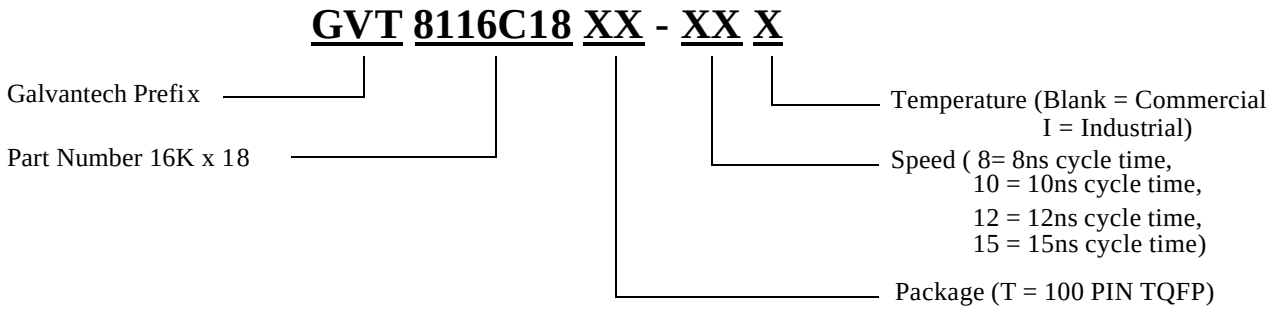
Note: All dimensions in Millimeters

Ordering Information

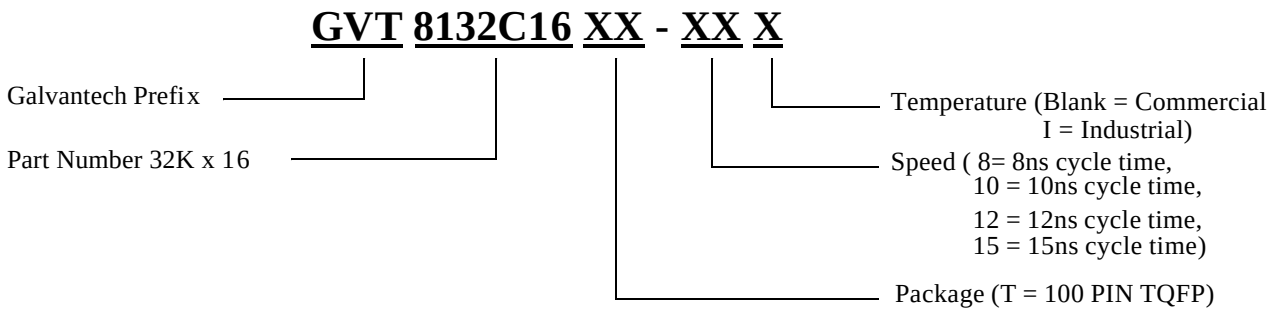
16K x 16



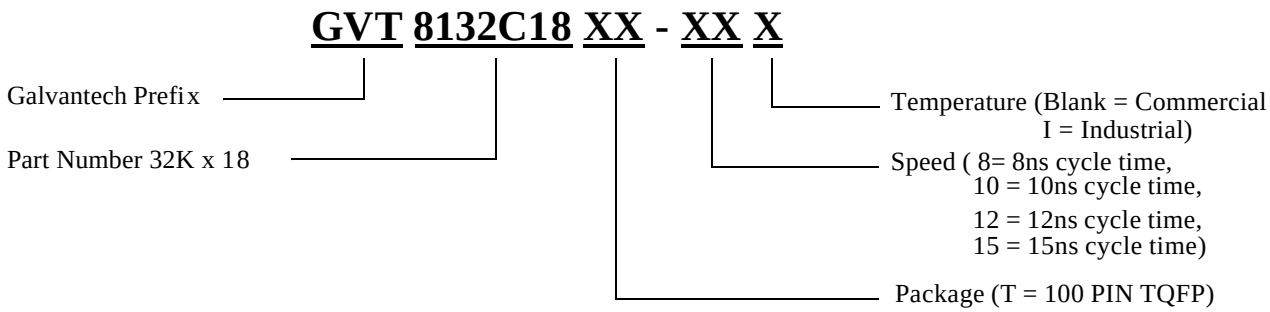
16K x 18



32K x 16



32K x 18



Ordering Information (continued)

64K x 16

GVT 8164C16 XX - XX X

- Galvantech Prefix
- Part Number 64K x 16
- Temperature (Blank = Commercial, I = Industrial)
- Speed (8= 8ns cycle time, 10 = 10ns cycle time, 12 = 12ns cycle time, 15 = 15ns cycle time)
- Package (T = 100 PIN TQFP)

64K x 18

GVT 8164C18 XX - XX X

- Galvantech Prefix
- Part Number 64K x 18
- Temperature (Blank = Commercial, I = Industrial)
- Speed (8= 8ns cycle time, 10 = 10ns cycle time, 12 = 12ns cycle time, 15 = 15ns cycle time)
- Package (T = 100 PIN TQFP)

32K x 8

GVT 8132C8 XX - XX X

- Galvantech Prefix
- Part Number 32K x 8
- Temperature (Blank = Commercial, I = Industrial)
- Speed (8= 8ns cycle time, 10 = 10ns cycle time, 12 = 12ns cycle time, 15 = 15ns cycle time)
- Package (T = 100 PIN TQFP)

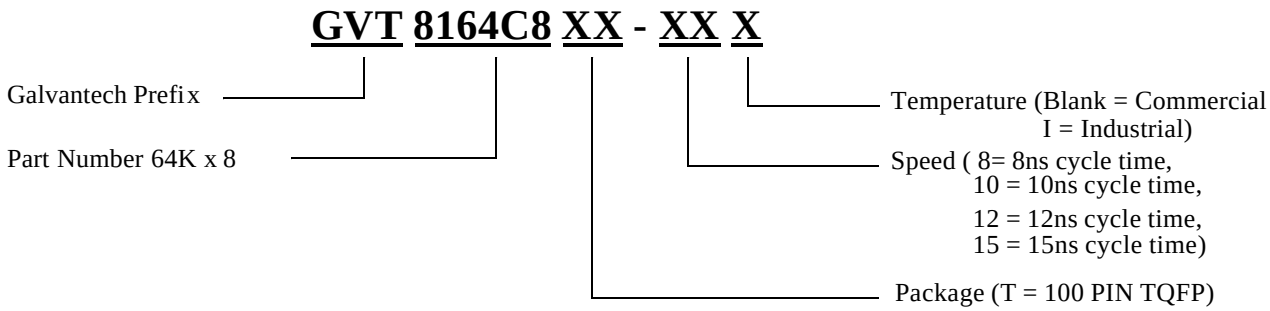
32K x 9

GVT 8132C9 XX - XX X

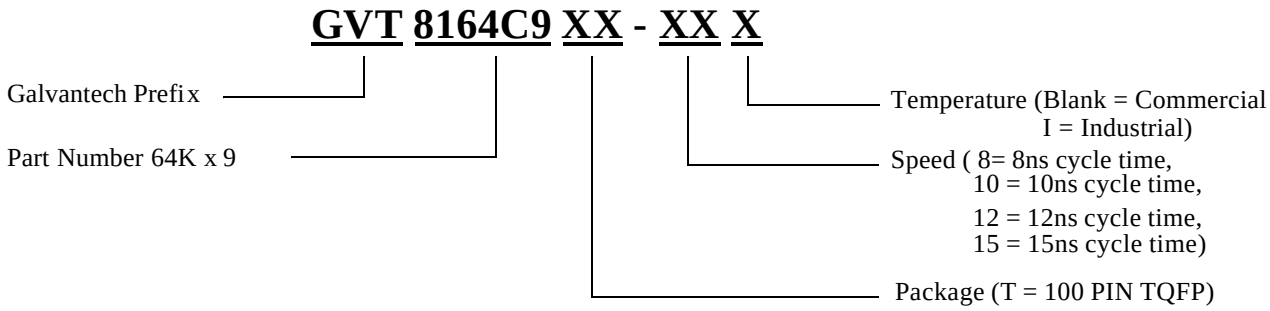
- Galvantech Prefix
- Part Number 32K x 9
- Temperature (Blank = Commercial, I = Industrial)
- Speed (8= 8ns cycle time, 10 = 10ns cycle time, 12 = 12ns cycle time, 15 = 15ns cycle time)
- Package (T = 100 PIN TQFP)

Ordering Information (continued)

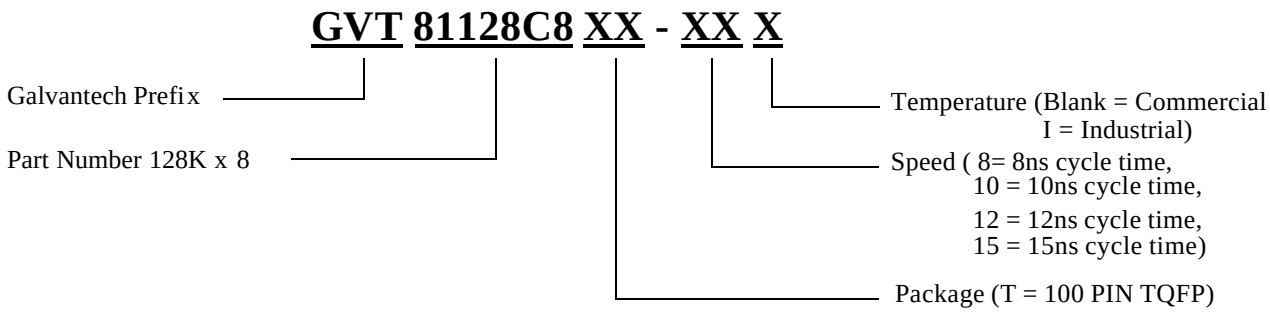
64K x 8



64K x 9



128K x 8



128K x 9