

SED1230 Series

Dot Matrix LCD Controller Driver

- ullet 12 Character \times 4 Line (5 \times 7 dot)
- Built-in Character Generator ROM and RAM
- Built-in Power Supply Circuit for LCD

■ DESCRIPTION

The SED1230 Series is a dot matrix LCD controller driver for character display, and can display a maximum of 48 characters, 4 user-defined characters, and a maximum of 64 symbols by means of 4-bit, 8-bit or serial data sent from a microcomputer.

A built-in character generator ROM is prepared for 256 character types, and each character font consists of 5×7 dots. A user-defined character RAM for four characters of 5×7 dots are incorporated, and a symbol register is also incorporated. With these, it is possible to apply this Series to display with a high degree of freedom. This Series can operate handy units with a minimum power consumption by means of its low power consumption and standby mode.

The SED1230 Series are classified into SED1230, SED1231, SED1232, and SED1233 depending on the duty of use and the number of display columns.

■ FEATURES

- Built-in display RAM
 - 48 characters + 4 user-defined characters + 64 symbols
- CGROM (for up to 256 characters), CGRAM (4 characters), and symbol register (64 symbols)
- Number of display columns × number of lines

(12 columns + 1 column for signal) \times 4 lines + 52 symbols: SED1230 (12 columns + 1 column for signal) \times 3 lines + 52 symbols: SED1231 (12 columns + 1 column for signal) \times 2 lines + 52 symbols: SED1232 16 columns \times 2 lines + 64 symbols: SED1233

- CR oscillating circuit (incorporating C and R)
- High-speed MPU interface

Interfacing with both 68 series and 80 series MPU Interfacing in 4 bits/8 bits

Serial interface

• Character font 5×7 dots

Duty ratio
 1/16 (SED1232, SED1233)

1/23 (SED1231) 1/30 (SED1230)

- Simple command setting
- Built-in liquid crystal driving power circuit

Voltage boosting circuit, voltage regulating circuit, voltage follower × 4

- Built-in electronic volume function
- Low power consumption

 $100 \,\mu\text{A}$ Max. (In normal operation mode:

Including the operating current of the built-in power supply)

20 μA Max. (In standby display mode)

Power supply

VDD - VSS (logic section): −2.4 V to −3.6 V

VDD - V5 (liquid crystal drive section): -5.0 V to -11.0 V (In the case of external power supply)

Wide operating temperature range

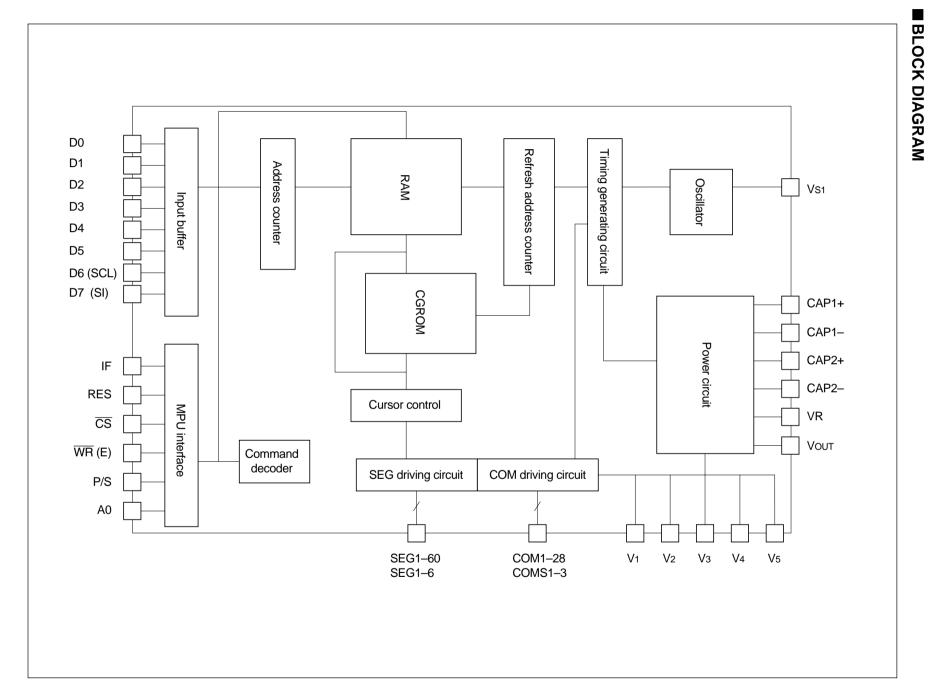
 $Ta = -30 \text{ to } 85^{\circ}C$

- CMOS process
- ◆ Package: Die form SED123*D*B, SED123*D*E (Au bump)

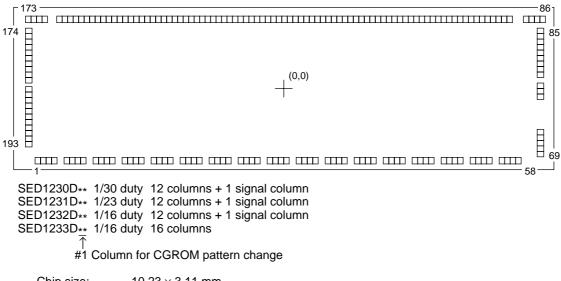
SED123*D*A, SED123*D*C (Al pad)

TCP SED123*T**

This IC is not designed with a protection against radioactive rays.



■ PAD SPECIFICATION



Chip size: 10.23×3.11 mm Pad pitch: $110 \mu m$ (Min.)

Chip thickness: $625 \pm 25 \mu m (SED123 *D*A, SED123 *D*B)$ $525 \pm 25 \mu m (SED123 *D*c, SED123 *D*E)$

1) A1 pad specification (SED123*D*A)

Pad size: A $86 \mu m \times 135 \mu m$ B $135 \mu m \times 86 \mu m$

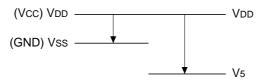
2) Au bump specification (SED123*D*B*)

For reference:

Bump size A $80~\mu m \times 129~\mu m$ B $129~\mu m \times 80~\mu m$ Bump height $22.5~\mu m \pm 5.5~\mu m$

■ ABSOLUTE MAXIMUM RATINGS

Rating		Symbol	Value	Unit
Power supply voltage	(1)	Vss	-6.0 to +0.3	V
Power supply voltage	(2)	V5	-16.0 to +0.3	V
Power supply voltage	(3)	V1, V2, V3, V4	V5 to +0.3	V
Input voltage		Vin	Vss-0.3 to +0.3	V
Output voltage		Vo	Vss-0.3 to +0.3	V
Operating temperature		Topr	-30 to +85	°C
Storage temperature	TCP	T _{str}	-55 to +100	°C
Otorage temperature	Bare chip	i su	-75 to +125	



Notes: 1. All the voltage values are based on VDD = 0 V.

- 2. For voltages of V₁, V₂, V₃ and V₄, keep the condition of V_{DD} \geq V₁ \geq V₂ \geq V₃ \geq V₄ \geq V₅ at all times.
- 3. If the LSI is used exceeding the absolute maximum ratings, it may lead to permanent destruction. In ordinary operation, it is desirable to use the LSI in the condition of electrical characteristics. If the LSI is used out of this condition, it may cause a malfunction of the LSI and have a bad effect on the reliability of the LSI.

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■ DC CHARACTERISTICS

 $(VDD = 0 \text{ V}, \text{Vss} = -3.6 \text{ V} \text{ to } -2.4 \text{ V}, \text{Ta} = -30 \text{ to } 85^{\circ}\text{C} \text{ unless otherwise specified.})$

Characteristic			Symbol		Cor	ndition	Min.	Тур.	Max.	Unit	Applicable pin	
Powe	er	Recommended operation Operable						-3.6	-3.0	-2.4	V	Vss
supp	ly			Vss								
volta	ge (1)							-5.5	-3.0	-2.0		*1
Powe	er	Recommended						-11.0		-5.0	V	V5
supp	oly operation		V5									
voltage (2)		Operable						-11.0		-4.5		*2
		Operable Operable		V1, V2				0.6×V5		Vdd	V	V1, V2
				V3, V4				VDD		0.8×V5	V	V3, V4
High-level input voltage			VIHC				0.2×Vss		Vdd	V	*3	
Low-level input voltage			VILC				Vss		0.8×Vss	V	*3	
Input leakage current			llı	VIN:	= Vdd or	Vss	-1.0		1.0	μA	*3	
LC driver ON resistance			Ron		25°C :0.1V	V5=-7.0V		20	40	ΚΩ	COM,SEG *4	
Static current consumption			IDDQ					0.1	5.0	μA	VDD	
Dynamic current IDD			Display S	splay State $V_5 = -7 \text{ V}$ without load					100	μA	VDD *5	
consumption		Standby state		Oscillat Power (•			20	μA	VDD *6		
				Sleep state		Oscillat Power (ation OFF,			5	μΑ	VDD
			Access s	tate	fcyc=200	OKHz			500	μA	VDD *7	
Input pin capacity			CIN	T	a=25°C	f=1MHz		5.0	8.0	pF	*3	
Reset time			t R				1.0			μs	*8	
Reset pulse width			trw				10			μs	*9	
éd	Input	put voltage		Vss				-3.6		-2.4	V	*10
dns	Boost	ooster output voltage		Vout	Vout Do		sting state	-7.2			V	Vout
Built-in power supply					Tri	iple boos	ting state	-10.8				
	Voltag	Voltage follower		V5				-11.0		-4.5	V	
Ξ		rating voltage										
Reference voltage			VREG	Ta	= 25°C		-3.5	-3.1	-2.7	V		

^{*1:} A wide operating voltage range is guaranteed but an abrupt voltage variation in the access status of the MPU is not guaranteed.

(ΔI: Current flowing when 0.1 V is applied between the power and output)

- *5: Character " display. This is applicable to the case where no access is made from the MPU and the built-in power circuit and oscillating circuit are in operation.
 - and disclinating circuit are in operation.

 3: This disclinating circuit are in operation.

 4: This disclinating circuit are in operation.

 5: This disclinating circuit are in operation.

 5: This disclinating circuit are in operation.

 5: This disclinating circuit are in operation.

 6: This disclinating circuit are in operation.

 6: This disclinating circuit are in operation.

 7: This disclinating circuit are in operation.

 7: This disclinating circuit are in operation.

 8: This disclinating circuit are in operation.

 8: This disclinating circuit are in operation.

 8: This disclinating circuit are in operation.

 9: This disclination circuit are c
- mode.
- *7: Current consumption when data is always written by fcyc. The current consumption in the access state is almost proportional to the access frequency (fcyc). When no access is made, only IDD (I) occurs.
- *8: tk (reset time) indicates the internal circuit reset completion time from the edge of the RES signal. Accordingly, the SED123* usually enters the operating state after tk.
- *9: The minimum pulse width of the RES signal is specified.
 - To cause a reset operation, it is necessary to input a pulse width exceeding tRW.
- *10: When operating the boosting circuit, the power supply Vss must be used within the input voltage range.

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^{*2:} The operating voltage range is applicable to the case where an external power supply is used.

^{*3:} D0 - D5, D6 (SCL), D7 (SI), A0, RES, CS WR (E), P/S, IF

^{*4:} This is a resistance value when a voltage of 0.1 V is applied between output pin SEGn, SEGSn, COMn or COMSn, and each power pin (V1, V2, V3 or V4). It is specified in the range of operating voltage (2).

RON = 0.1 V / ΔI

■ CHARACTOR FONT (JIS TYPE STANDARD)

● SED123*DA*



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● SED123*DB*



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● SED123*DG*



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SED1230 Series

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