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Using Microchip's Micropower LDOs

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INTRODUCTION

Microchip Technology, Inc.'s family of micropower LDOs utilizes low-voltage CMOS process technology. These LDOs provide similar ripple rejection and dropout characteristics as their bipolar equivalents, but are significantly more efficient. A typical bipolar regulator has base current equal to 1-2% of the output load, whereas Microchip's LDOs have approximately 60µA resulting in total operating current orders of magnitude lower than their bipolar counterparts. In addition, Microchip's LDOs can be placed in a shutdown mode, further enhancing their effectiveness in low-power applications.

This low-power operation makes Microchip's family of LDOs ideal for upgrading the LP2980 and MIC5205 bipolar LDOs in cellular phones, pagers, PDAs, laptops, hand-held meters, and other portable applications.

Microchip's micropower LDOs are available with fixed and adjustable outputs, supporting load currents up to 50mA, 100mA, 150mA and 300mA. SOT-23A-5, SOT-23A-6, SOT-223, and MSOP-8 packaging require minimal board space. Shutdown capability, thermal protection, and current limiting are standard in every device. Adjustable output, error flag, and noise bypass capability are provided on select devices (see Table 3).

APPLICATIONS

Optimizing Output Voltage Accuracy of 1070/1071 Adjustable LDOs

Microchip's LDOs are available in both adjustable and fixed output voltage options. The accuracy of the output depends on the initial accuracy, stability, and temperature coefficient of the internal bandgap reference and the feedback resistors.

Rather than specifying V_{OUT} accuracy on adjustable regulators, the initial accuracy and temperature coefficient of the internal reference is specified. V_{OUT} accuracy is not specified because it depends on the external feedback resistors. Figure 1 shows a typical adjustable LDO feedback circuit in which resistors R1 and R2 set the output voltage per the following formula:

$$V_{OUT} = V_{REF}\,[(R1/R2) + 1]$$

Where: $V_{REF} = 1.20V$

EQUATION 1:

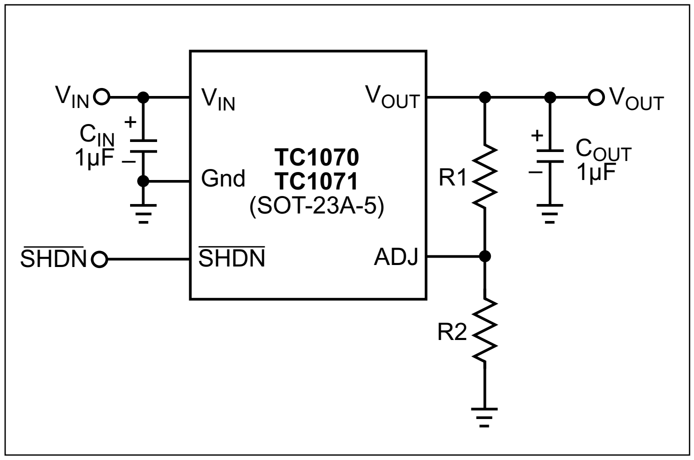

FIGURE 1: *Adjustable LDO feedback circuit.*

The ADJ pin is a high impedance CMOS input. Consequently, resistor values can be between 300KΩ and 1MΩ to minimize the current through R1 and R2.

Inspection of Equation 1 reveals the following:

1. When V_{OUT} is made equal to V_{REF} (i.e., R1 is zero), the tolerance of V_{OUT} will be approximately that of V_{REF}.
2. The tolerance of V_{OUT} is a function of *both* the tolerance of V_{REF} and the tolerance of the R1/R2 ratio when V_{OUT} is greater than V_{REF} (i.e., when R1/R2 > 0).

For the purposes of worst case analysis, the tolerances of R1 and R2 are additive. For example, if R1 and R2 are both 1% resistors, the maximum tolerance of the R1/R2 ratio is 2%.

Re-examining the effect of tolerances on Equation 1 reveals that the tolerance of V_{OUT} worsens proportionally as the V_{OUT} setting departs the value of V_{REF}. Stated another way:

$$ERROR_{VOUT} \propto (V_{OUT} - V_{REF})$$

EQUATION 2:

Table 1 shows that percentage of total output voltage error contributed by the tolerances of V_{REF} and R1/R2 for various values of V_{OUT}.

V_{OUT} (V)	Reference Tolerance (%)	Resistor Tolerance (%)	Resistor Error (%)	Total Output Error (%)
1.23	2	1	0	2
1.23	2	2	0	2
2.0	2	1	0.77	2.77
2.0	2	2	1.54	3.54
2.46	2	1	1.0	3.0
2.46	2	2	2.0	4.0
3.0	2	1	1.2	3.2
3.0	2	2	2.4	4.2
4.0	2	1	1.38	3.38
4.0	2	2	2.76	4.76
5.0	2	1	1.50	3.5
5.0	2	2	3.0	5.0

TABLE 1: *Output error contributors.*

The output voltage accuracy of the adjustable regulator improves with tighter tolerance resistors. However, accuracy will be limited to ±2% due to the accuracy of the reference. Table 2 shows output voltage accuracy for the adjustable LDO using 1%, 0.5%, and 0.1% tolerance resistors.

V_{OUT}	V_{OUT} Error		
	1% Resistor Tol.	**0.5% Resistor Tol.**	**0.1% Resistor Tol.**
5.0V	3.5%	2.75%	2.15%
4.0V	3.38%	2.69%	2.14%
3.0V	3.2%	2.6%	2.12%
2.46V	3.0%	2.5%	2.10%
2.0V	2.77%	2.39%	2.08%
1.23V	2.0%	2.0%	2.0%

TABLE 2: *Resistor tolerance effect on V_{OUT} error.*

Power-Saving Shutdown Mode

All of Microchip's micropower LDOs have a shutdown input that allows the user to digitally disconnect the load from the power source and send the regulator into a low-power "sleep" mode. The supply current is reduced from 50µA, during normal operation, to 0.05µA in shutdown.

The $\overline{\text{SHDN}}$ pin input current is guaranteed to be no greater than 1µA (an order of magnitude lower than bipolar counterparts).

Shutdown mode is activated when $\overline{\text{SHDN}}$ is below 0.2 x V_{IN}. In this mode, the pass transistor is turned OFF, disconnecting the load from the power source.

Shutdown mode is disabled, allowing normal device operation, when the input is above 0.4 x V_{IN}. This V_{IN} is low enough to ensure that a control output from a 3.3V microcontroller, operating from four fully-charged NiCad/NiMH cells (6V), can enable the LDO. If not used, $\overline{\text{SHDN}}$ should not be left floating, but rather connected to V_{IN}.

Out-of-Regulation ($\overline{\text{ERROR}}$) Flag

The TC1070/1/2/3 and TC1054/5 each have Error Flag outputs that are asserted when the LDO falls out of regulation by approximately –5%.

The $\overline{\text{ERROR}}$ pin is an N-channel open drain output that can sink up to 1mA. However, larger value pull-up resistors should be selected so that energy loss through $\overline{\text{ERROR}}$ is kept to a minimum. $\overline{\text{ERROR}}$ must be pulled to any supply voltage less than 7V through a pull-up resistor.

$\overline{\text{ERROR}}$ output is valid for input voltages above 1V and undefined for voltages below 1V. As the output is transitioning between 0V and 1.0V during power up/down, the Error output may float momentarily to 1.0V. If 1.0V is high enough to be interpreted as a logic 1, the two-resistor network shown in Figure 3 may be used. This will ensure that $\overline{\text{ERROR}}$ never will rise above 0.5V during invalid states. Keep in mind the maximum that Error output can be in its high state is $V_{OUT}/2$.

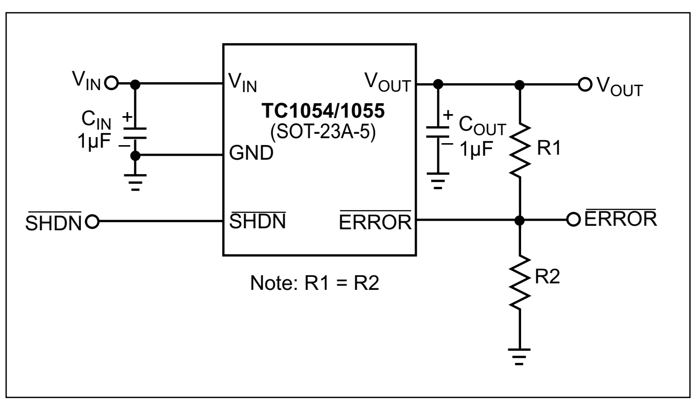

FIGURE 2: *Ensuring valid error output for low V_{IN} levels.*

By connecting an RC on $\overline{\text{ERROR}}$ output, it can be used as a power on reset. During power up, the Error comparator will go high as soon as the regulator output is within tolerance. $\overline{\text{ERROR}}$ will be delayed by the RC network before releasing the microcontroller from reset.

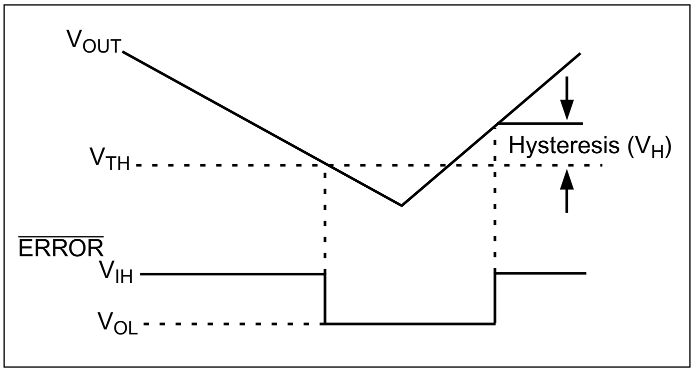

FIGURE 3: *Out-of-regulation error flag.*

$\overline{\text{ERROR}}$ also can be used as a power quality monitor. If a low input voltage or an over-current condition causes the output to fall out of regulation, $\overline{\text{ERROR}}$ will pull low, signifying an unstable power condition. This flags the microcontroller, which now can activate proper shutdown sequencing, ensuring orderly system operation.

The Error comparator has 50mV of positive hysteresis to provide some V_{IN} noise immunity.

Input, Output and Bypass Capacitors

It is recommended that input, output, and bypass capacitors be used for optimal device performance. To ensure stability in the LDO's feedback loop, a capacitor is required from the output to ground (Figures 4 and 5). Capacitors must be chosen that meet the ESR value range and minimum capacitance identified in device datasheets. In general, a 1µF-2.2µF capacitor is recommended to ensure stable operation under maximum load conditions. Larger value capacitors (4.7 to 10µF) will increase transient load response and ripple rejection performance.

Ceramic capacitors offer the lowest ESR followed by, in order of increasing ESR, OS-CON, film, aluminum electrolytic, and tantalum. Film capacitors provide good performance, but usually are not a viable solution due to excessive cost and size. Ceramics combine excellent ESR with relatively small size. However, the ESR of ceramic capacitors sometimes can be too low, requiring a 1Ω series resistor to ensure stability. OS-CON capacitors offer an ESR only slightly higher than ceramics, but consume more volume. The OS-CON capacitors exhibit rock-solid ESR from –55°C to 125°C. Aluminum electrolytics are ideal for low-cost commercial temperature grade applications where board space is not a concern. Like OS-CON capacitors, electrolytics typically are offered in a radial lead package, but are available in surface mount styles. Tantalums offer an ESR similar to aluminum electrolytics. They also provide a reasonable cost, high-volume efficiency solution and are usually the capacitor of choice.

A 1µF input capacitor should be installed from V_{CC} to GND (Figures 4 and 5) if the IC is powered from a battery or if there is excessive (>1ft) distance between the regulator and the AC filter capacitor. A larger value capacitor will provide better V_{CC} noise rejection and improved performance when the supply has a high AC impedance. A 470pf bypass capacitor can be tied to the bypass pin on the TC1014/1015 and TC1072/1073 or the ADJ pin on the TC1070/1071 (see Figure 5) to reduce the V_{REF} noise.

Thermal Issues

The amount of power that the LDO dissipates is a function of the bias supply current and the pass-through current. The pass-through current is the current that flows from V_{CC} through the pass transistor of the LDO to the load. The following equation is used to calculate power dissipation:

$$P_D = (V_{CC} \times I_s) + [(V_{CC} - V_{OUT})\, I_{LOAD}]$$

EQUATION 3:

Maximum values of V_{CC} and I_{LOAD} and minimum values for V_{OUT} should be used when calculating P_D to ensure worst case conditions are met.

The amount of power that the LDO can dissipate depends on the ambient temperature (T_A). A guardbanded maximum die temperature (T_{JMAX}) of 125°C is used to account for variations in thermal conductivity of PC boards and variations in airflow.

$$\theta_{JA} = (T_{JMAX} - T_A)/P_{DMAX}$$
$$\theta_{JA} = \theta_{JC} + \theta_{CA}$$

EQUATION 4:

θ_{JC} is the thermal resistance from the die surface to the package body and leads. θ_{CA} is the thermal resistance from the package body and leads to the surrounding air, PC board dielectric, and traces.

The SOT-23A-5 and SOT-23A-6 packages have a worst case θ_{JA} of 220°C/W when mounted on a single-layer FR4 dielectric copper-clad PC board. This θ_{JA} can be reduced by using a PC board made with a dielectric that has a better heat transfer coefficient. Additionally, adding a ground plane and large supply traces to the IC will provide better thermal conductivity. The values for θ_{JA} are for a system that uses natural convection. A significant reduction in θ_{CA} can be induced with forced airflow.

Given: $\theta_{JA} = 220°C/W$
$\therefore P_{DMAX} = (125°C - T_A)/\ 220°C/W$

Ambient Temperature	P_{DMAX}
25°C	0.454W
50°C	0.341W
85°C	0.182W

Excessive power dissipation will result in elevated die temperatures that could activate the device's thermal shutdown. The LDOs have an integrated thermal protection circuitry that disables the LDO when die temperatures exceed approximately 160°C. Ten degrees Celsius of hysteresis is built into the protection circuitry, such that the LDO is not released from thermal shutdown until the die temperature drops to 150°C. In addition to thermal protection, an internal sense resistor in series with the pass element provides a short-circuit limit.

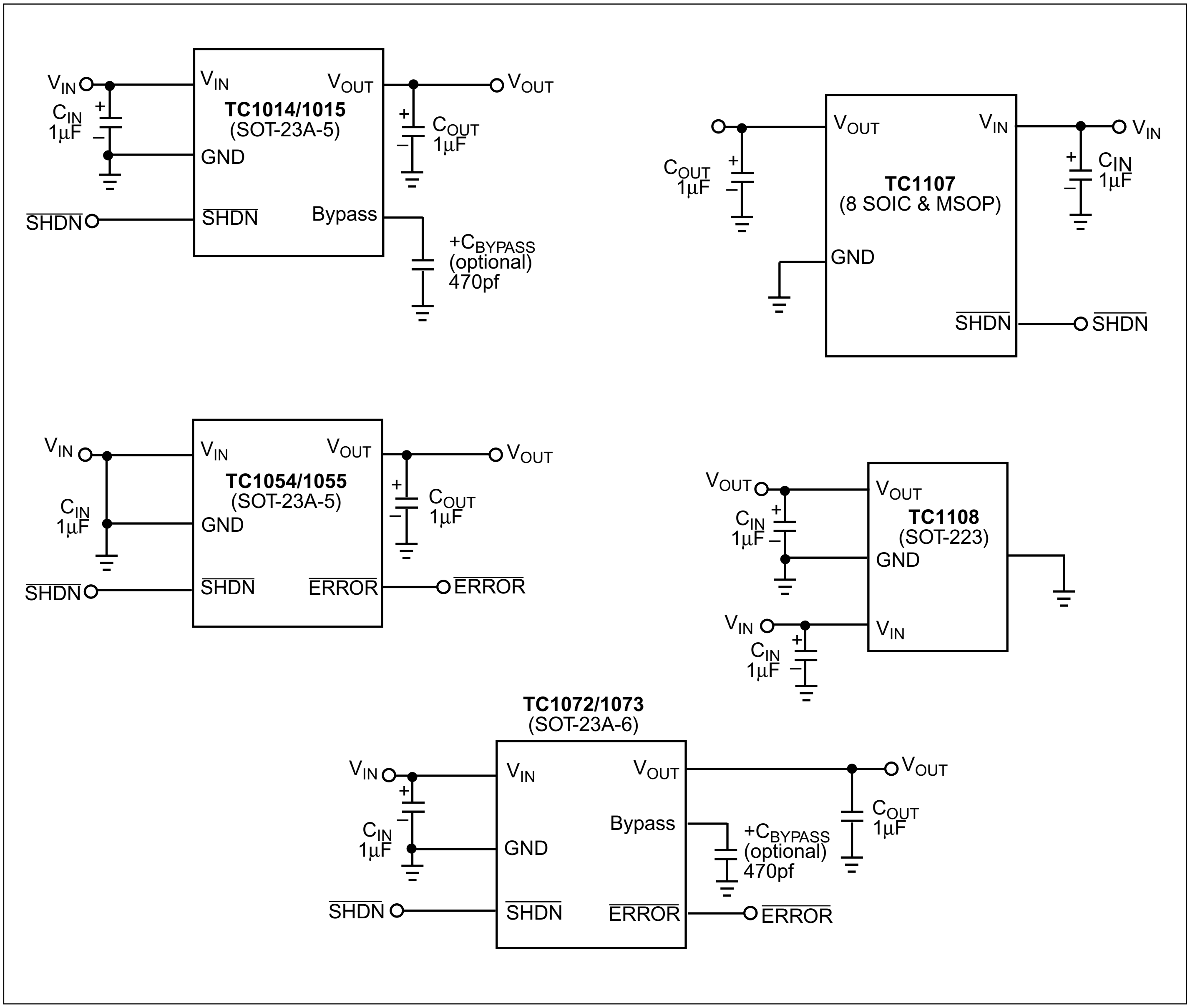

FIGURE 4: Typical application circuit (fixed output).

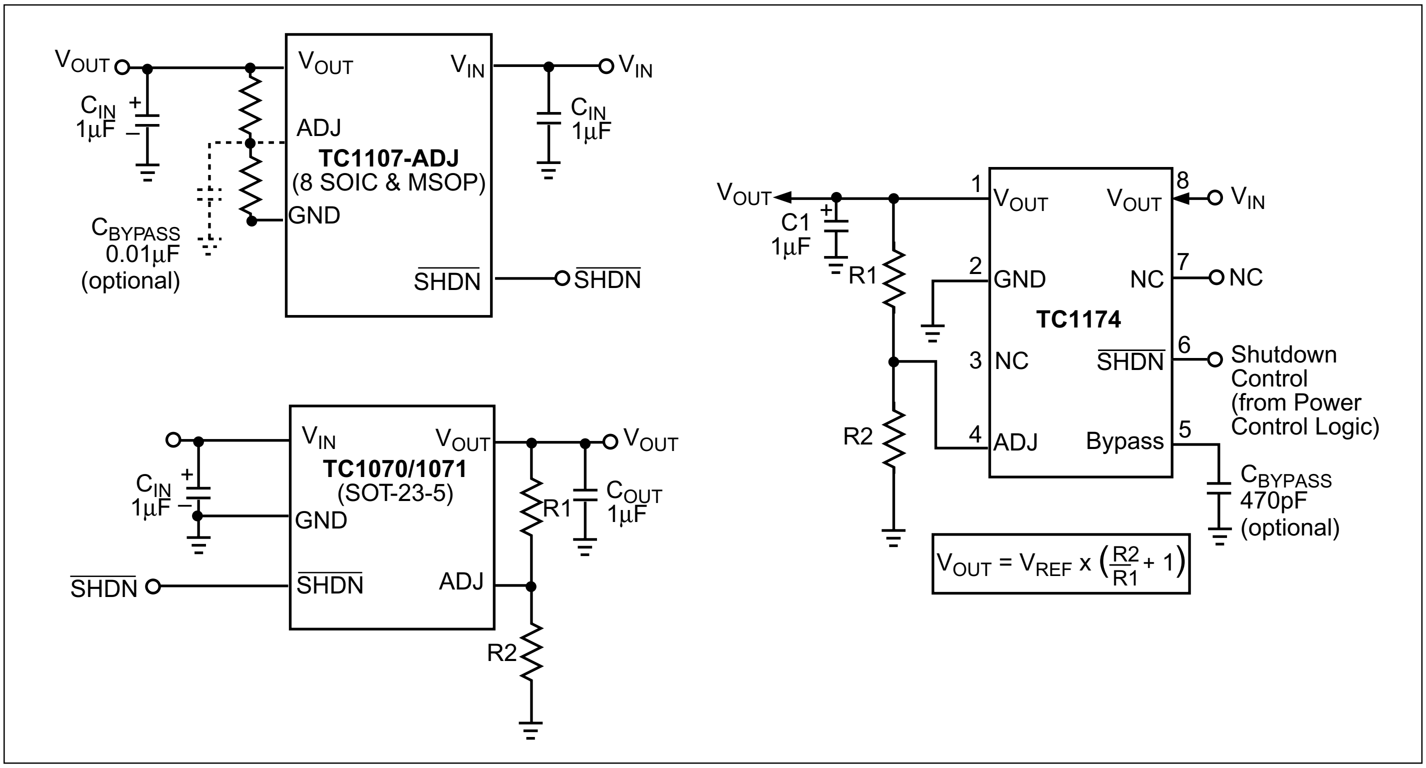

FIGURE 5: *Typical application circuit (adjustable output).*

Part No.	Package	Output Voltage**											Adj	SHDN	Error Flag	Bypass	I_{SS} Typ. (µA)	I_{OUT} Max (mA)	V_{DROP} Typ. (mV)
		2.5V	2.7V	2.8V	2.84V	2.85V	3.0V	3.15V	3.3V	3.6V	4.0V	5.0V							
TC1014	SOT-23A-5	X	X			X	X		X	X	X	X		X		X	50	50	85
TC1015	SOT-23A-5	X	X			X	X		X	X	X	X		X		X	50	100	180
TC1054	SOT-23A-5	X	X			X	X		X	X	X	X		X	X		50	50	85
TC1055	SOT-23A-5	X	X			X	X		X	X		X		X	X		50	100	180
TC1070	SOT-23A-5												X	X			50	50	85
TC1071	SOT-23A-5												X	X			50	100	180
TC1072	SOT-23A-6	X	X			X	X		X	X	X	X		X		X	50	50	85
TC1073	SOT-23A-6	X	X			X	X		X	X	X	X		X		X	50	100	180
TC1107	MSOP-8, SO-8			X			X		X			X		X		X	50	300	240
TC1108	SOT-223			X			X		X			X					50	300	240
TC1173	MSOP-8, SO-8			X			X		X			X		X	X	X	50	100	180
TC1174	MSOP-8, SO-8												X	X		X	50	300	240
TC1185	SOT-23A-5	X	X			X	X		X	X	X	X		X		X	50	150	270
TC1186	SOT-23A-5	X	X			X	X		X	X	X	X		X	X		50	150	270
TC1187	SOT-23A-5												X	X	X		50	150	270
TC1188*	SOT-23A-5			X	X			X						X			50	100	55
TC1189*	SOT-23A-5			X	X			X						X			50	100	55
TC1223	SOT-23A-5	X	X			X	X		X	X	X	X		X			50	50	85
TC1224	SOT-23A-5	X	X			X	X		X	X	X	X		X			50	100	180

Notes: *Pin Compatible Replacement for MAX8863/8864 **Custom Output Voltages Available – Contact Microchip Technology

TABLE 3: *CMOS LDOs selection guide.*

DNV Certification, Inc.
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DNV MSC
The Netherlands
Accredited by the RvA

ISO 9001 / QS-9000
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