V54C31732G2V

PRELIMINARY

HIGH PERFORMANCE 166/143 MHz
3.3 VOLT ENHANCED GRAPHICS
512K X 32 SDRAM 2 BANKS X 256Kbit X 32

V54C31732G2V	-6	-7	-8	-10	Unit
Clock Frequency (t_{CK})	166	143	125	100	MHz
Latency	3	3	3	3	clocks
Cycle Time (t_{CK})	6	7	8	10	ns
Access Time (t_{AC})	5.4	5.4	6	7	ns

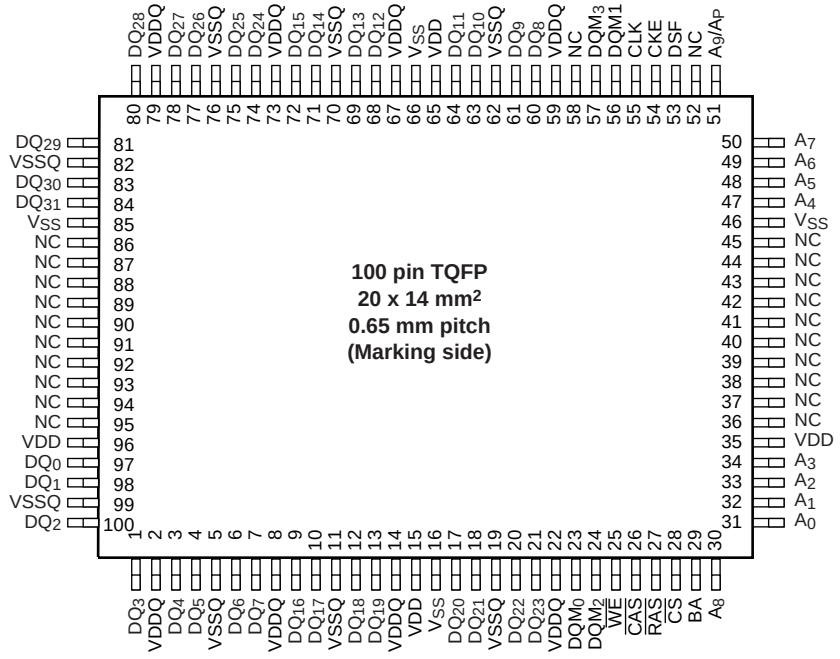
Features

- JEDEC Standard 3.3V Power Supply
- Specially screened for graphics applications
- Single Pulsed $\overline{RAS}$ Interface
- Programmable $\overline{CAS}$ Latency: 2, 3
- All Inputs are sampled at the positive going edge of clock
- Programmable Wrap Sequence: Sequential or Interleave
- Programmable Burst Length: 1, 2, 4, 8 and Full Page for Sequential and 1, 2, 4, 8 for Interleave
- DQM 0-3 for Byte Masking
- Auto & Self Refresh
- 2K Refresh Cycles/32 ms
- Special Mode Registers
- One Color Register
- Burst Read with Single Write Operation
- Block Write (8 Columns)

Description

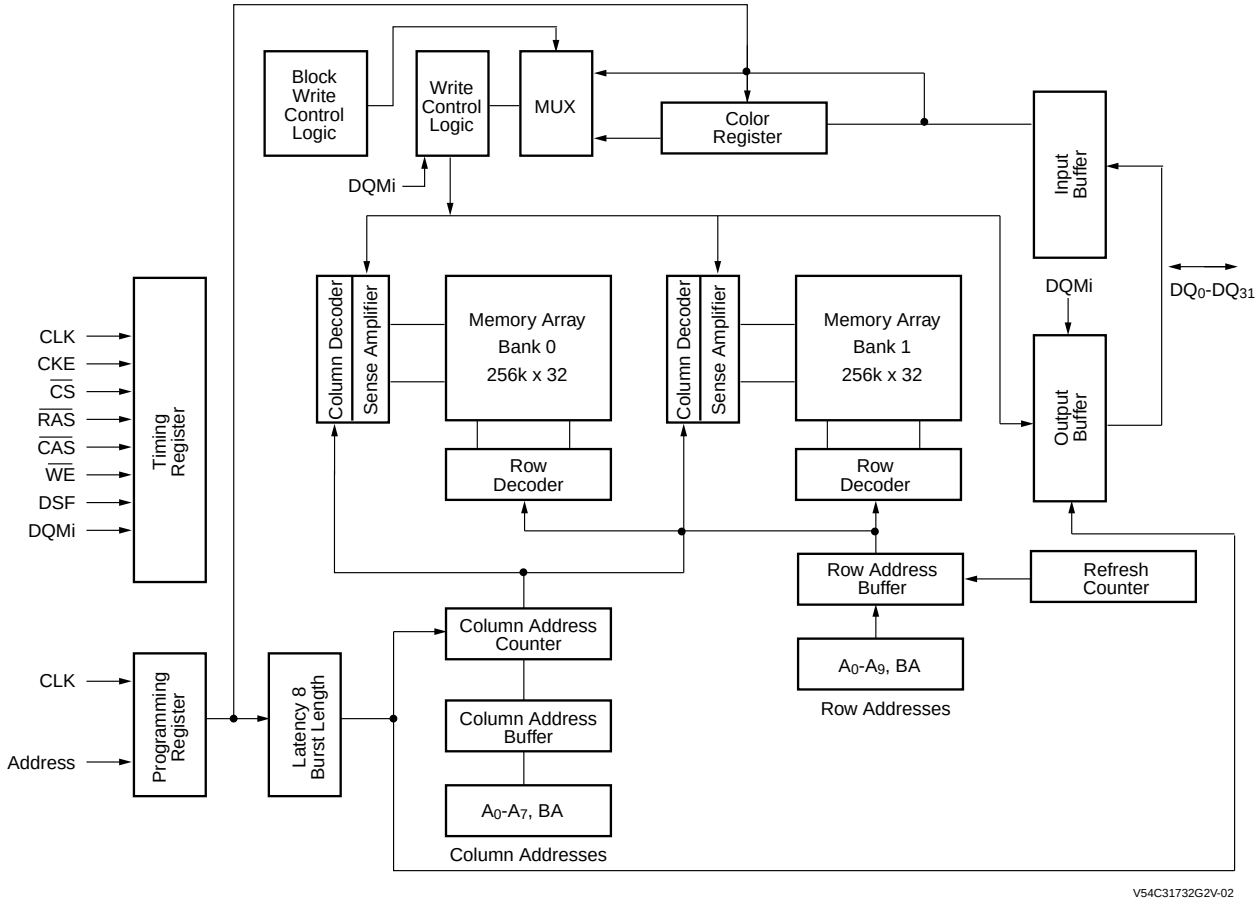
The V54C31732G2V is a 33,554,432 bits synchronous high data rate DRAM organized as 2 x 262,144 words by 32 bits. The device is designed to comply with JEDEC standards set for synchronous DRAM products, both electrically and mechanically. Synchronous design allows precise cycle control with the system clock. The CAS latency, burst length and burst sequence must be programmed into device prior to access operation. In addition, it features block write and masked block write functions by making a programmable mode register and special mode register, the system can select modes to maximize its performance.

100 Pin TQFP
PIN CONFIGURATION
Top View



V54C31732G2V-01

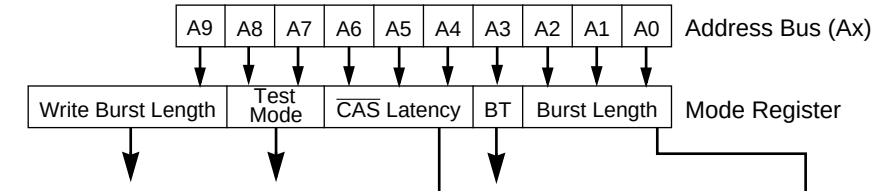
Block Diagram



Signal Pin Description

Pin	Name	Input Function
CLK	Clock Input	System clock input. Active on the positive rising edge to sample all inptus
CKE	Clock Enable	Activates the CLK signal when high and deactivates the CLK when low. CKE low initiates the power down mode, suspend mode, or the self refresh mode
$\overline{CS}$	Chip Select	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQMi
$\overline{RAS}$	Row Address Strobe	Latches row addresses on the positive edge of CLK with $\overline{RAS}$ low. Enables row access & precharge
$\overline{CAS}$	Column Address Strobe	Latches column addresses on the positive edge of CLK with $\overline{CAS}$ low. Enables column access
$\overline{WE}$	Write Enable	Enables write operation
A_0-A_9	Address	During a bank activate command, A_0-A_9 defines the row address. During a read or write command, A_0-A_7 defines the column address. In addition to the column address A_9 is used to invoke auto precharge BA define the bank to be precharged. A_9 is low, auto precharge is disabled during a precharge cycle, If A_9 is high, both bank will be precharged ,if A_9 is low, the BA is used to decide which bank to precharge
BA	Bank Select	Selects which bank to activate. BA low select bank A and high selects bank B
DQ_0-DQ_{31}	Data Input/Output	Data inputs/output are multiplexed on the same pins
DQMi	Data Input/Output Mask	Makes data output Hi-Z. Blocks data input when DQM is active
VDD/VSS	Power Supply/Ground	Power Supply. +3.3V $\pm$ 0.3V/ground
VDDQ/VSSQ	Data Output Power/Ground	Provides isolated power/ground to DQs for improved noise immunity
DSF	Define Special Function	Enables block write and special mode register set
NC	No Connection	

Address Input for Mode Set (Mode Register Operation)



Write Burst Length

A9	Length
0	Burst
1	Single Bit

Test Mode

A8	A7	Mode
0	0	Mode Reg Set

Burst Type

A3	Type
0	Sequential
1	Interleave

CAS Latency

A6	A5	A4	Latency
0	0	0	Reserve
0	0	1	Reserve
0	1	0	2
0	1	1	3
1	0	1	Reserve
1	1	0	Reserve
1	1	1	Reserve

Burst Length

A2	A1	A0	Length	
			Sequential	Interleave
0	0	0	1	1
0	0	1	2	2
0	1	0	4	4
0	1	1	8	8
1	0	0	Reserve	Reserve
1	0	1	Reserve	Reserve
1	1	0	Reserve	Reserve
1	1	1	Full Page	Reserve

Special Mode Set SMRS

A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	Functions
X			0	X	X					Unchanged
X			1	X	X					Load Color Register

Power On and Initialization

The default power on state of the mode register is supplier specific and may be undefined. The following power on and initialization sequence guarantees the device is preconditioned to each users specific needs. Like a conventional DRAM, the Synchronous DRAM must be powered up and initialized in a predefined manner. During power on, all VCC and VCCQ pins must be built up simultaneously to the specified voltage when the input signals are held in the “NOP” state. The power on voltage must not exceed VCC+0.3V on any of the input pins or VCC supplies. The CLK signal must be started at the same time. After power on, an initial pause of 200 µs is required followed by a precharge of both banks using the precharge command. To prevent data contention on the DQ bus during power on, it is required that the DQM and CKE pins be held high during the initial pause period. Once all banks have been precharged, the Mode Register Set Command must be issued to initialize the Mode Register. A minimum of eight Auto Refresh cycles (CBR) are also required.These may be done before or after programming the Mode Register. Failure to follow these steps may lead to unpredictable start-up modes.

Programming the Mode Register

The Mode register designates the operation mode at the read or write cycle. This register is divided into 4 fields. A Burst Length Field to set the length of the burst, an Addressing Selection bit to program the column access sequence in a burst cycle (interleaved or sequential), a CAS **Latency** Field to set the access time at clock cycle and a Operation mode field to differentiate between normal operation (Burst read and burst Write) and a special Burst Read and Single Write mode. The mode set operation must be done before any activate command after the initial power up. Any content of the

mode register can be altered by re-executing the mode set command. All banks must be in pre-charged state and CKE must be high at least one clock before the mode set operation. After the mode register is set, a Standby or NOP command is required. Low signals of $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ and DSF at the positive edge of the clock activate the mode set operation. Address input data at this timing defines parameters to be set as shown in the previous table.

Read and Write Operation

When $\overline{RAS}$ is low and both $\overline{CAS}$ and $\overline{WE}$ are high at the positive edge of the clock, a RAS cycle starts. According to address data, a word line of the selected bank is activated and all of sense amplifiers associated to the wordline are set. A $\overline{CAS}$ cycle is triggered by setting $\overline{RAS}$ high and $\overline{CAS}$ low at a clock timing after a necessary delay, t_{RCD}, from the $\overline{RAS}$ timing. $\overline{WE}$ is used to define either a read ($\overline{WE}$ = H) or a write ($\overline{WE}$ = L) at this stage.

SDRAM provides a wide variety of fast access modes. In a single CAS cycle, serial data read or write operations are allowed at up to a 166 MHz data rate. The numbers of serial data bits are the burst length programmed at the mode set operation, i.e., one of 1, 2, 4, 8 and full page. Column addresses are segmented by the burst length and serial data accesses are done within this boundary. The first column address to be accessed is supplied at the CAS timing and the subsequent addresses are generated automatically by the programmed burst length and its sequence. For example, in a burst length of 8 with interleave sequence, if the first address is '2', then the rest of the burst sequence is 3, 0, 1, 6, 7, 4, and 5.

Full page burst operation is only possible using the sequential burst type and page length is a function of the I/O organisation and column addressing. Full page burst operation do not self terminate once the burst length has been reached. In other words, unlike burst length of 2, 3 or 8, full page burst continues until it is terminated using another command.

Similar to the page mode of conventional DRAM's, burst read or write accesses on any column address are possible once the RAS cycle latches the sense amplifiers. The maximum t_{RAS} or the refresh interval time limits the number of random column accesses. A new burst access can be done even before the previous burst ends. The interrupt operation at every clock cycles is supported. When the previous burst is interrupted, the remaining addresses are overridden by the new address with the full burst length. An interrupt which accompanies with an operation change from a read to a write is possible by exploiting DQM to avoid bus contention.

When two or more banks are activated sequentially, interleaved bank read or write operations are possible. With the programmed burst length, alternate access and precharge operations on two or more banks can realize fast serial data access modes among many different pages. Once two or more banks are activated, column to column interleave operation can be done between different pages.

Burst Length and Sequence:

Burst Length	Starting Address (A2 A1 A0)	Sequential Burst Addressing (decimal)	Interleave Burst Addressing (decimal)
2	xx0	0, 1	0, 1
	xx1	1, 0	1, 0
4	x00	0, 1, 2, 3	0, 1, 2, 3
	x01	1, 2, 3, 0	1, 0, 3, 2
	x10	2, 3, 0, 1	2, 3, 0, 1
	x11	3, 0, 1, 2	3, 2, 1, 0
8	000	0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7
	001	1 2 3 4 5 6 7 0	1 0 3 2 5 4 7 6
	010	2 3 4 5 6 7 0 1	2 3 0 1 6 7 4 5
	011	3 4 5 6 7 0 1 2	3 2 1 0 7 6 5 4
	100	4 5 6 7 0 1 2 3	4 5 6 7 0 1 2 3
	101	5 6 7 0 1 2 3 4	5 4 7 6 1 0 3 2
	110	6 7 0 1 2 3 4 5	6 7 4 5 2 3 0 1
	111	7 0 1 2 3 4 5 6	7 6 5 4 3 2 1 0
Full Page	nnn	Cn, Cn+1, Cn+2,.....	not supported

Refresh Mode

SDRAM has two refresh modes, Auto Refresh and Self Refresh. Auto Refresh is similar to the $\overline{CAS}$ -before-$\overline{RAS}$ refresh of conventional DRAMs. All of banks must be precharged before applying any refresh mode. An on-chip address counter increments the word and the bank addresses and no bank information is required for both refresh modes.

The chip enters the Auto Refresh mode, when $\overline{RAS}$ and $\overline{CAS}$ are held low and CKE and $\overline{WE}$ are held high at a clock timing. The mode restores word line after the refresh and no external precharge command is necessary. A minimum tRC time is required between two automatic refreshes in a burst refresh mode. The same rule applies to any access command after the automatic refresh operation.

The chip has an on-chip timer and the Self Refresh mode is available. It enters the mode when $\overline{RAS}$, $\overline{CAS}$, and CKE are low and $\overline{WE}$ is high at a clock timing. All of external control signals including the clock are disabled. Returning CKE to high enables the clock and initiates the refresh exit operation. After the exit command, at least one t_{RC} delay is required prior to any access command.

DQM Function

DQM has two functions for data I/O read and write operations. During reads, when it turns to "high" at a clock timing, data outputs are disabled and become high impedance after two clock delay (DQM Data Disable Latency t_{DQZ}). It also provides a data mask function for writes. When DQM is activated, the write operation at the next clock is prohibited (DQM Write Mask Latency t_{DQW} = zero clocks). DQM is used for device selection, byte selection and bus control in a memory system. DQM0 controls DQ0 to DQ7, DQM1 controls DQ8 to DQ15, DQM2 controls DQ16 to DQ23, DQM3 controls DQ24 to DQ31.

Suspend Mode

During normal access mode, CKE is held high enabling the clock. When CKE is low, it freezes the internal clock and extends data read and write operations. One clock delay is required for mode entry and exit (Clock Suspend Latency t_{CSL}).

Power Down

In order to reduce standby power consumption, a power down mode is available. All banks must be precharged and the necessary Precharge delay (trp) must occur before the SDRAM can enter the Power Down mode. Once the Power Down mode is initiated by holding CKE low, all of the receiver circuits except CLK and CKE are gated off. The Power Down mode does not perform any refresh operations, therefore the device can't remain in Power Down mode longer than the Refresh period (tref) of the device. Exit from this mode is performed by taking CKE "high". One clock delay is required for mode entry and exit.

Auto Precharge

Two methods are available to precharge SDRAMs. In an automatic precharge mode, the CAS timing accepts one extra address, A9, to determine whether the chip restores or not after the operation. If A9 is high when a Read Command is issued, the **Read with Auto-Precharge** function is initiated. The SDRAM automatically enters the precharge operation one clock before the last data out for $\overline{CAS}$ latencies 2, two clocks for $\overline{CAS}$ latencies 3. If A9 is high when a Write Command is issued, the **Write with Auto-Precharge** function is initiated. The SDRAM automatically enters the precharge operation a time delay equal to t_{WR} (Write recovery time) after the last data in.

Define Special Function

The DSF controls the graphic applications of graphic SDRAM. If DSF is tied to low SGRM functions as 2 x 256K x 32 SDRAM. All the graphic function modes can be entered only by setting DSF high when issuing commands which otherwise would be normal SDRAM commands.

Special Mode Register Set (SMRS)

There is one special mode registers in graphic SDRAM. It's the color register. The usage will be in block write function. When A6 and DSF goes high in the same cycle as $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ going Low, Load Color Register (LCR) process is executed and the color register is filled with color data for associated DQ's through the DQ pins.

Block Write

Block write is a feature allowing the simultaneous writing of consecutive 8 columns of data within a RAM device during a single access cycle. During block write the data to be written comes from an internal color register and DQ I/O pins are used for independent column selection. The block of column to be written is aligned on 8 column boundries. Write command with DSF=1 enables block write for the associated bank. Write command with DSF=0 is for normal write. The color register has the same

width of the I/Os. Block writes are always non-burst, independent of burst length that has been programmed into the mode register. Back to back block writes are allowed provided that the specified block write cycle time (t_{BWC}) is satisfied.

Precharge Command

There is also a separate precharge command available. When $\overline{RAS}$ and $\overline{WE}$ are low and $\overline{CAS}$ is high at a clock timing, it triggers the precharge operation. With A9 being low, the BA is used select bank to precharge. The precharge command can be imposed one clock before the last data out for CAS latency = 2, two clocks before the last data out for CAS latency = 3. Writes require a time delay twr from the last data out to apply the precharge command.

Enhanced Graphic SDRAM vs SDRAM

Function	MRs		Write	
DSF	L	H	L	H
Enhanced Graphic Function	MRS	SMRS	Normal Write	Block Write

Burst Termination

Once a burst read or write operation has been initiated, there are several methods in which to terminate the burst operation prematurely. These methods include using another Read or Write Command to interrupt an existing burst operation, use a Precharge Command to interrupt a burst cycle and close the active bank, or using the Burst Stop Command to terminate the existing burst operation but leave the bank open for future Read or Write Commands to the same page of the active bank. When interrupting a burst with another Read or Write Command care must be taken to avoid I/O contention. The Burst Stop Command, however, has the fewest restrictions making it the easiest method to use when terminating a burst operation before it has been completed. If a Burst Stop command is issued during a burst write operation, then any residual data from the burst write cycle will be ignored. Data that is presented on the I/O pins before the Burst Stop Command is registered will be written to the memory.

Summary of Enhanced Graphic SDRAM Basic Features and Benefits

Features	256K x 32 x 2 SGRAM	Benefits
Interface	Synchronous	Better interaction between memory and system without wait-state of asynchronous DRAM. High speed vertical and horizontal drawing. High operating frequency allows performance gain for SCROLL, FILL, and BitBLT.
Bank	2 ea	Pseudo-infinite row length by on-chip interleaving operation. Hidden row activation and precharge.
Page Depth / 1 Row	8Kbit	High speed vertical and horizontal drawing.
Total Page Depth	1K row	High speed vertical and horizontal drawing.
Burst Length(Read)	1, 2, 4, 8 Full Page	Programmable burst of 1, 2, ,4, 8 and full page transfer per column addresses.
Burst Length(Write)	1, 2, 4, 8 Full Page	Programmable burst of 1, 2, ,4, 8 and full page transfer per column addresses.
	BRSW	Switch to burst length of 1 at write without MRS.
Burst Type	Sequential & Interleave	Compatible with Intel and Motorola CPU based system.
CAS Latency	3	Programmable CAS latency.
Block Write	8 Columns	High speed FILL, CLEAR, Text with color registers. Maximum 32 byte data transfers(e.g. for 8bpp : 32 pixels) with plane and byte masking functions.
Color Register	1 ea.	A and B bank share.
Mask function	DQM0-3	Byte masking (pixel masking for 8bpp system) for data-out/in

*Absolute Maximum Ratings**

Operating temperature range .....0 to 70 °C
Storage temperature range ..... -55 to 150 °C
Input/output voltage ..... -0.3 to (V_{CC}+0.3) V
Power supply voltage ..... -0.3 to 4.6 V
Power dissipation ..... 1 W
Data out current (short circuit) ..... 50 mA

***Note:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage of the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operation and Characteristics

T_A = 0 to 70 °C; V_{SS} = 0 V; V_{CC},V_{CCQ} = 3.3 V ± 0.3 V

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Input high voltage	V_{IH}	2.0	Vcc+0.3	V	1, 2
Input low voltage	V_{IL}	– 0.3	0.8	V	1, 2
Output high voltage (I_{OUT} = – 2.0 mA)	V_{OH}	2.4	–	V	3
Output low voltage (I_{OUT} = 2.0 mA)	V_{OL}	–	0.4	V	3
Input leakage current, any input (0 V < V_{IN} < 3.6 V, all other inputs = 0 V)	$I_{I(L)}$	– 5	5	µA	
Output leakage current (DQ is disabled, 0 V < V_{OUT} < V_{CC})	$I_{O(L)}$	– 5	5	µA	

Note:
1. All voltages are referenced to V_{SS}.
2. V_{IH} may overshoot to V_{CC} + 2.0 V for pulse width of < 4ns with 3.3V. V_{IL} may undershoot to -2.0 V for pulse width < 4.0 ns with 3.3V. Pulse width measured at 50% points with amplitude measured peak to DC reference.

Operating Currents (T_A = 0 to 70°C, V_{CC} = 3.3V ± 0.3V)
(Recommended Operating Conditions unless otherwise noted)

Symbol	Parameter & Test Condition		Max. -6	Max. -7	Max. -8	Max. -10	Unit	Note
ICC1	Operating Current $t_{RC} = t_{RCMIN.}$, $t_{RC} = t_{CKMIN}$. Active-precharge command cycling, without Burst Operation	1 bank operation	230	210	190	170	mA	7
ICC2P	Precharge Standby Current in Power Down Mode	t_{CK} = min.	2	2	2	2	mA	7
ICC2PS	$\overline{CS}$ =V_{IH}, CKE≤ $V_{IL(max)}$	t_{CK} = Infinity	2	2	2	2	mA	7
ICC2N	Precharge Standby Current in Non-Power Down Mode	t_{CK} = min.	35	35	35	35	mA	
ICC2NS	$\overline{CS}$ =V_{IH}, CKE≥ $V_{IL(max)}$	t_{CK} = Infinity	15	15	15	15	mA	
ICC3P	Active Standby Current in Power-down mode	CKE ≤ V_{IL}(max), t_{ck} = min	3	3	3	3	mA	
ICC3PS		CKE ≤ V_{IL}(max), t_{ck} = infinity	3	3	3	3	mA	
ICC3N	Active Standby Current in non Power-down mode	CKE ≥ V_{IL}(max), t_{ck} = min	60	60	60	60	mA	
ICC3PS		CKE ≥ V_{IL}(max), t_{ck} = infinity	40	40	40	40	mA	
ICC4	Burst Operating Current t_{CK} = min Read/Write command cycling	CL = 3	310	280	250	210	mA	7,8
		CL = 2	180	180	180	170		
ICC5	Auto Refresh Current t_{CK} = min Auto Refresh command cycling		150	120	120	110	mA	7
ICC6	Self Refresh Current Self Refresh Mode, CKE=0.2V		2	2	2	2	mA	
		L-Power	400	400	400	400	µA	
ICC7	Operating Current (One Bank Block Write)		240	220	190	150	mA	

Notes:
7. These parameters depend on the cycle rate and these values are measured by the cycle rate under the minimum value of t_{CK} and t_{RC}. Input signals are changed one time during t_{CK}.
8. These parameter depend on output loading. Specified values are obtained with output open.

AC Characteristics [1,2,3]

T_A = 0 to 70°C; V_{SS} = 0 V; V_{CC} = 3.3 V ± 0.3 V, t_T = 1 ns

#	Symbol	Parameter	Limit Values -6 Min.	Limit Values -6 Max.	Limit Values -7 Min.	Limit Values -7 Max.	Limit Values -8 Min.	Limit Values -8 Max.	Limit Values -10 Min.	Limit Values -10 Max.	Unit	
Clock and Clock Enable												
1	t_{CK}	Clock Cycle Time										
		$\overline{CAS}$ Latency = 3	6	–	7	–	8	–	10	–	ns	
		$\overline{CAS}$ Latency = 2	10	–	10	–	10	–	13	–	ns	
2	t_{CK}	Clock Frequency										
		$\overline{CAS}$ Latency = 3	–	166	–	143	–	125	–	100	MHz	
		$\overline{CAS}$ Latency = 2	–	100	–	100	–	100	–	66	MHz	
3	t_{AC}	Access Time from Clock										
		$\overline{CAS}$ Latency = 3	–	5.4	–	5.4	–	6	–	7	ns	4
		$\overline{CAS}$ Latency = 2	–	7	–	7	–	7	–	9	ns	
4	t_{CH}	Clock High Pulse Width	2.5	–	2.5	–	3	–	3.5	–	ns	
5	t_{CL}	Clock Low Pulse Width	2.5	–	2.5	–	3	–	3.5	–	ns	
6	t_T	Transition time	1	10	1	10	1	10	1	10	ns	
Setup and Hold Times												
7	t_{CS}	Command Setup Time	2	–	2	–	2.5	–	2.5	–	ns	
8	t_{AS}	Address Setup Time	2	–	2	–	2.5	–	2.5	–	ns	
9	t_{DS}	Data In Setup Time	2	–	2	–	2.5	–	2.5	–	ns	
10	t_{CKS}	CKE Setup Time	2	–	2	–	2.5	–	2.5	–	ns	
11	t_{CH}	Command Hold Time	1	–	1	–	1	–	1	–	ns	
12	t_{AH}	Address Hold Time	1	–	1	–	1	–	1	–	ns	
13	t_{DH}	Data In Hold Time	1	–	1	–	1	–	1	–	ns	
14	t_{CKH}	CKE Hold Time	1	–	1	–	1	–	1	–	ns	
Common Parameters												
15	t_{RCD}	Row to Column Delay Time	16	–	16	–	16	–	20	–	ns	6
16	t_{RAS}	Row Active Time	48	100K	48	100K	48	100k	50	100k	ns	6
17	t_{RC}	Row Cycle Time	66	–	70	–	72	–	78	–	ns	6
18	t_{RP}	Row Precharge Time	18	–	21	–	24	–	26	–	ns	6
19	t_{RRD}	Activate(a) to Activate(b) Command period	12	–	14	–	16	–	20	–	ns	6
20	t_{CCD}	$\overline{CAS}$(a) to $\overline{CAS}$(b) Command period	1	–	1	–	1	–	1	–	CLK	
21	t_{RCS}	Mode Register Set-up time	12	–	14	–	16	–	20	–	ns	
22	t_{SB}	Power Down Mode Entry Time	6	–	7	–	0	8	0	10	ns	

AC Characteristics [1,2,3] (Continued)

T_A = 0 to 70°C; V_{SS} = 0 V; V_{CC} = 3.3 V ± 0.3 V, t_T = 1 ns

#	Symbol	Parameter	Limit Values -6 Min.	-6 Max.	-7 Min.	-7 Max.	-8 Min.	-8 Max.	-10 Min.	-10 Max.	Unit	
Refresh Cycle												
23	t_{REF}	Refresh Period (2048 cycles)	–	32	–	32	–	32	–	32	ms	
24	t_{SREX}	Self Refresh Exit Time	2 CLK + t_{RC}				2 CLK + t_{RC}					7
Read Cycle												
25	t_{OH}		2.5	–	2.5	–	2.5	–	2.5	–	ns	
27	t_{HZ}	$\overline{CAS}$ Latency = 3 $\overline{CAS}$ Latency = 2	– –	5.4 7	– –	5.4 7	– –	6 7	– –	7 8	ns	
28	t_{DQZ}	DQM Data Out Disable Latency	2	–	2	–	2	–	2	–	CLK	
Write Cycle												
29	t_{WR}	Write Recovery Time $\overline{CAS}$ Latency = 3 $\overline{CAS}$ Latency = 2	 6 10	 – –	 7 10	 – –	 8 10	 – –	 10 13	 – –	 ns ns	
30	t_{DQW}	DQM Write Mask Latency	0	–	0	–	0	–	0	–	CLK	
31	t_{BWC}	Block Write Cycle Time	1	–	1	–	1	–	1	–	CLK	

Notes for AC Parameters:

1. For proper power-up see the operation section of this data sheet.
2. AC timing tests have V_{IL} = 0.8V and V_{IH} = 2.0V with the timing referenced to the 1.4 V crossover point. The transition time is measured between V_{IH} and V_{IL}. All AC measurements assume t_T = 1ns with the AC output load circuit shown in Figure 1.

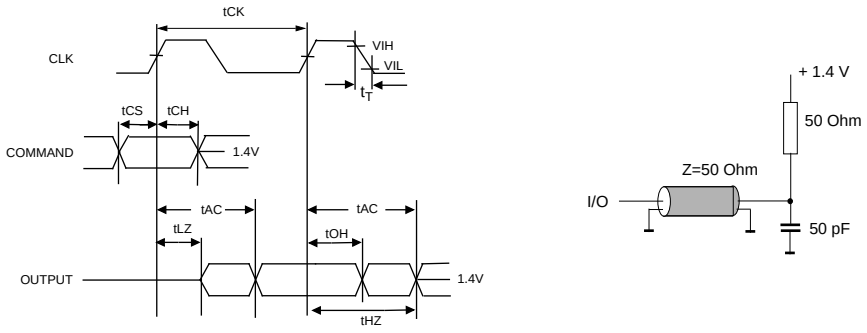


Figure 1.

4. If clock rising time is longer than 1 ns, a time (t_T/2 – 0.5) ns has to be added to this parameter.
5. If t_T is longer than 1 ns, a time (t_T – 1) ns has to be added to this parameter.
6. These parameter account for the number of clock cycle and depend on the operating frequency of the clock, as follows:

   the number of clock cycle = specified value of timing period (counted in fractions as a whole number)

   Self Refresh Exit is a synchronous operation and begins on the 2nd positive clock edge after CKE returns high. Self Refresh Exit is not complete until a time period equal to tRC is satisfied once the Self Refresh Exit command is registered.
7. Referenced to the time which the output achieves the open circuit condition, not to output voltage levels

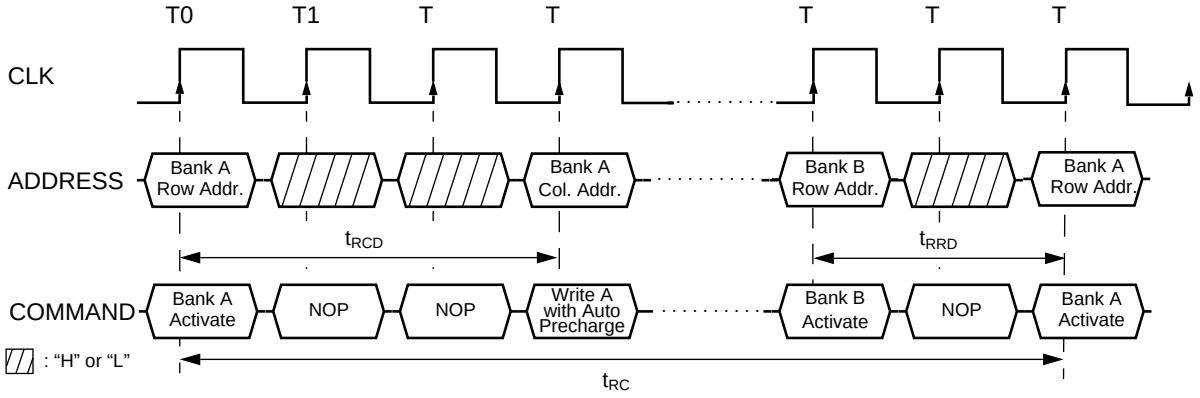
Timing Diagrams

Timing Diagrams (Cont'd)

16. Random Column Read (Page within same Bank)
    - 16.1 $\overline{CAS}$ Latency = 2
    - 16.2 $\overline{CAS}$ Latency = 3
17. Random Column Write (Page within same Bank)
    - 17.1 $\overline{CAS}$ Latency = 2
    - 17.2 $\overline{CAS}$ Latency = 3
18. Random Row Read (Interleaving Banks) with Precharge
    - 18.1 $\overline{CAS}$ Latency = 2
    - 18.2 $\overline{CAS}$ Latency = 3
19. Random Row Write (Interleaving Banks) with Precharge
    - 19.1 $\overline{CAS}$ Latency = 2
    - 19.2 $\overline{CAS}$ Latency = 3
20. Full Page Read Cycle
    - 20.1 $\overline{CAS}$ Latency = 2
    - 20.2 $\overline{CAS}$ Latency = 3
21. Full Page Write Cycle
    - 21.1 $\overline{CAS}$ Latency = 2
    - 21.2 $\overline{CAS}$ Latency = 3
22. Precharge Termination of a Burst
    - 22.1 $\overline{CAS}$ Latency = 2
    - 22.2 $\overline{CAS}$ Latency = 3

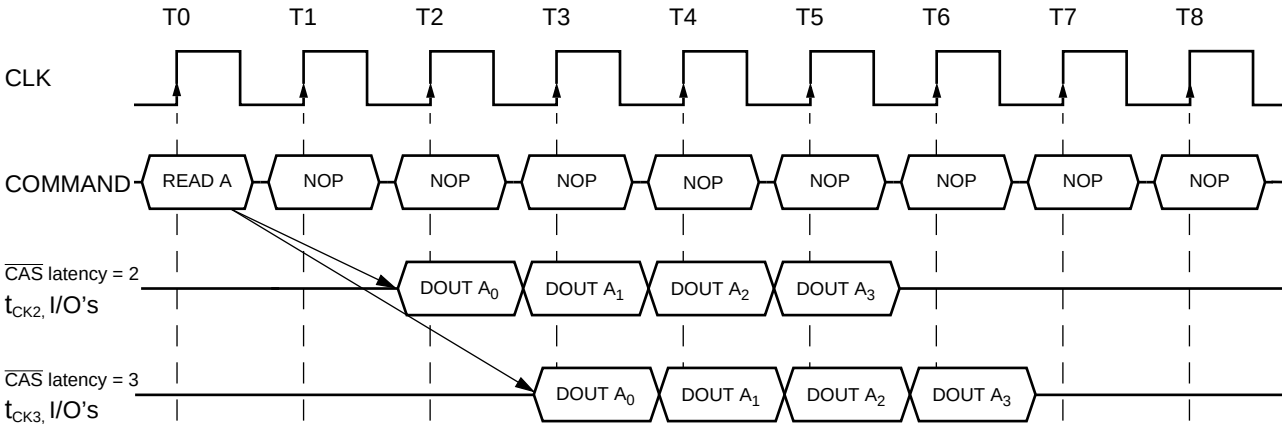
1. Bank Activate Command Cycle

(CAS latency = 3)



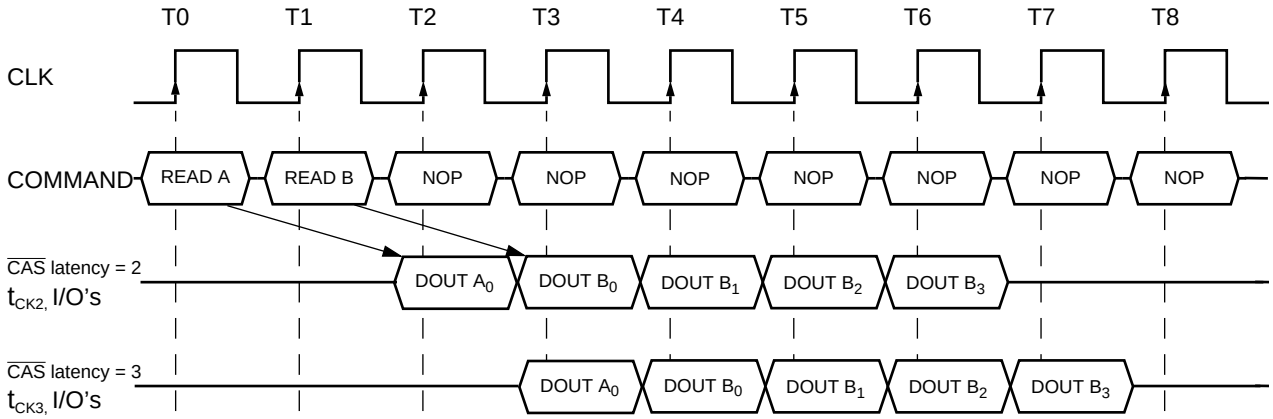
2. Burst Read Operation

(Burst Length = 4, CAS latency = 2, 3, 4)



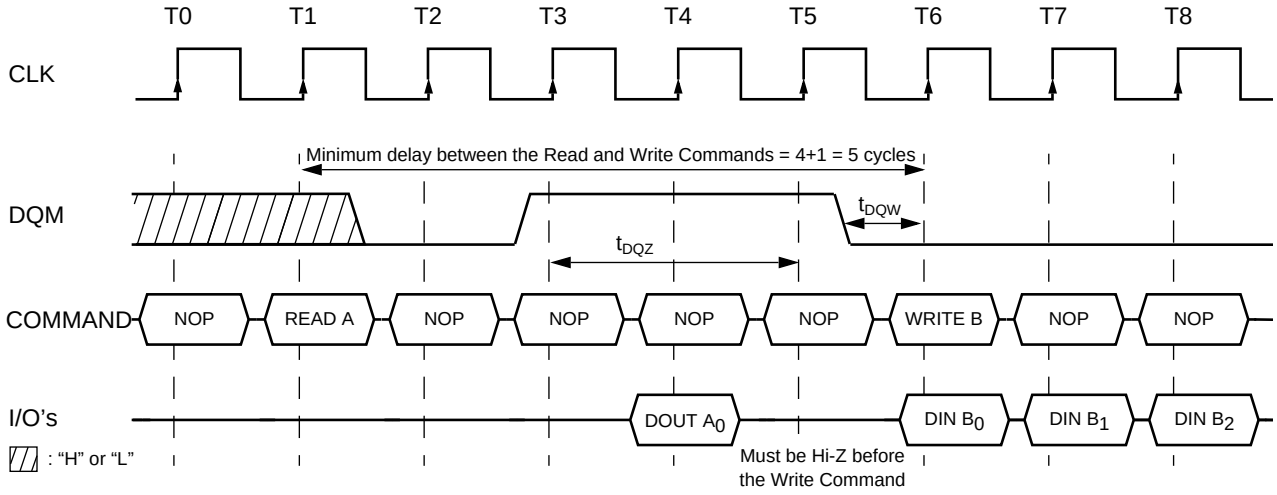
3. Read Interrupted by a Read

(Burst Length = 4, $\overline{CAS}$ latency = 2, 3)



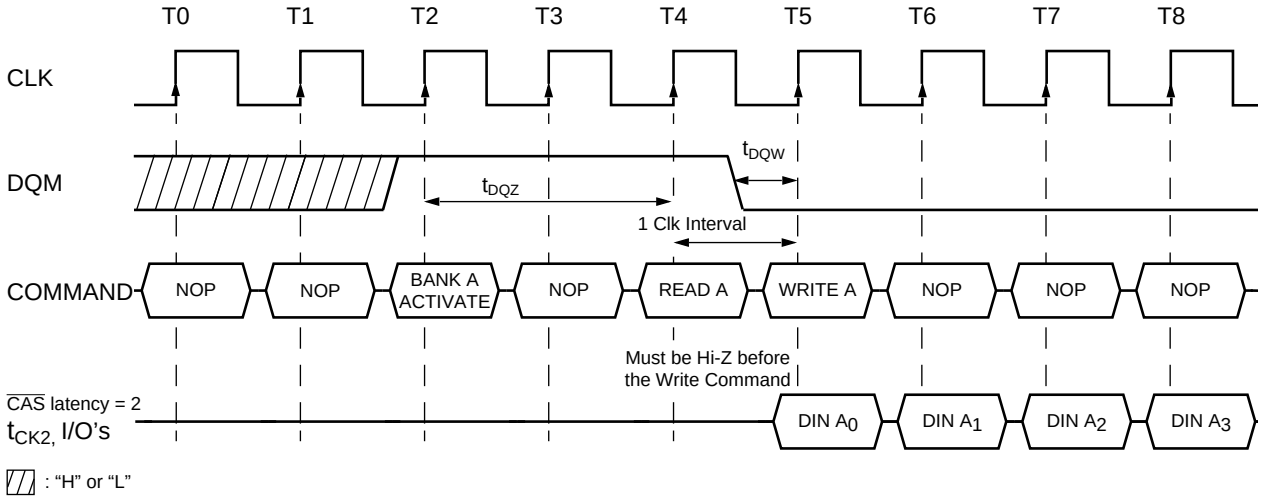
4.1 Read to Write Interval

(Burst Length = 4, $\overline{CAS}$ latency = 3)



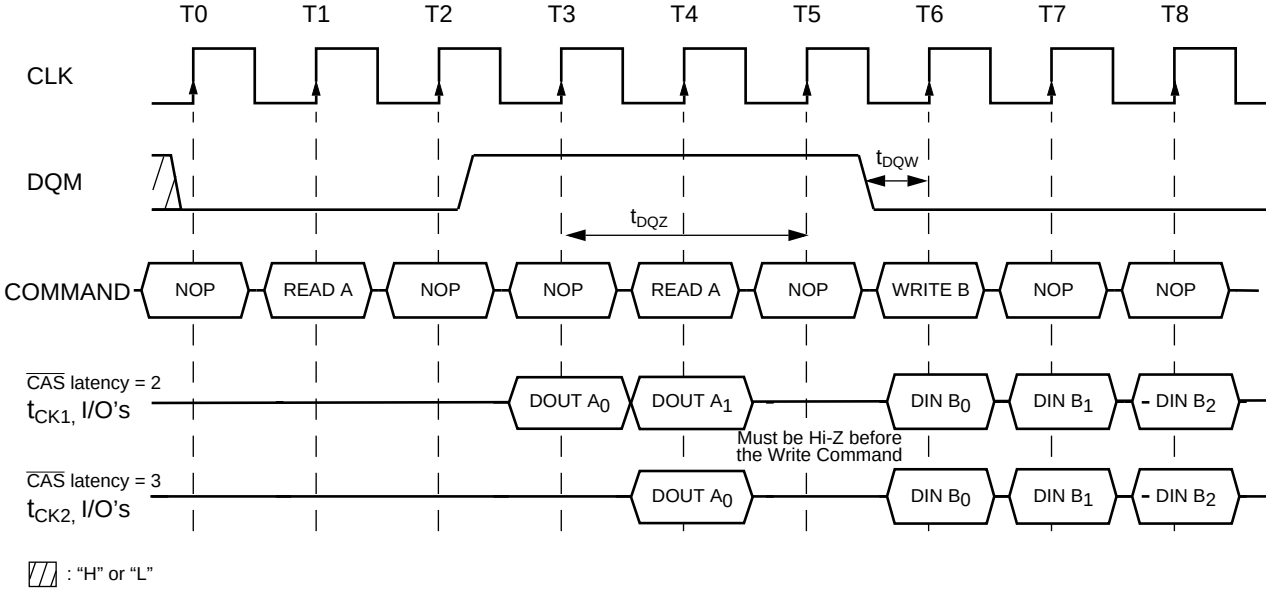
4.2 Minimum Read to Write Interval

(Burst Length = 4, $\overline{CAS}$ latency = 2)



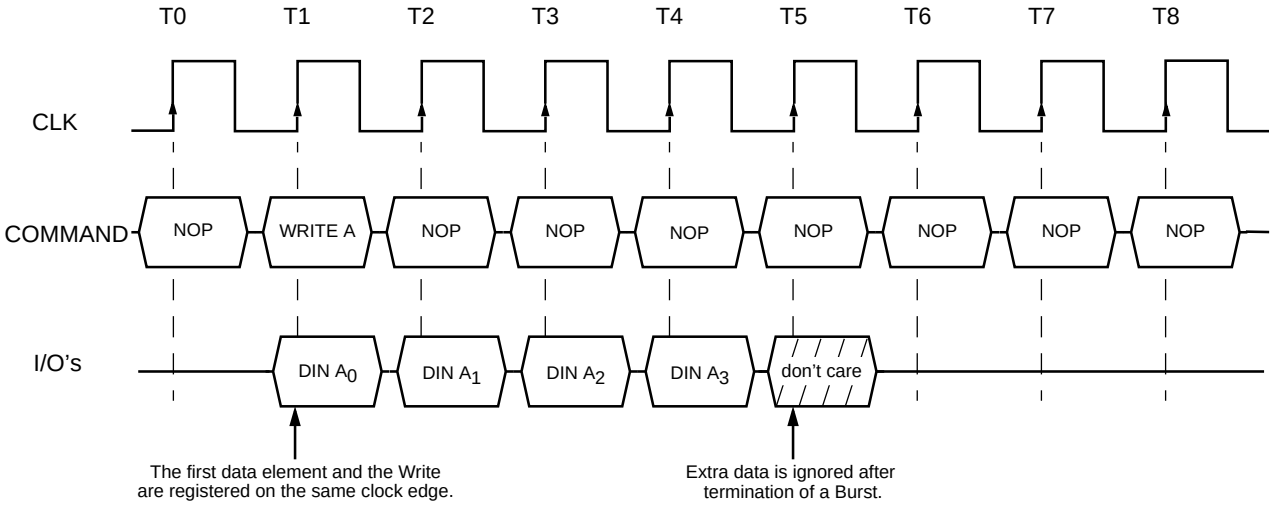
4.3 Non-Minimum Read to Write Interval

(Burst Length = 4, $\overline{CAS}$ latency = 2, 3



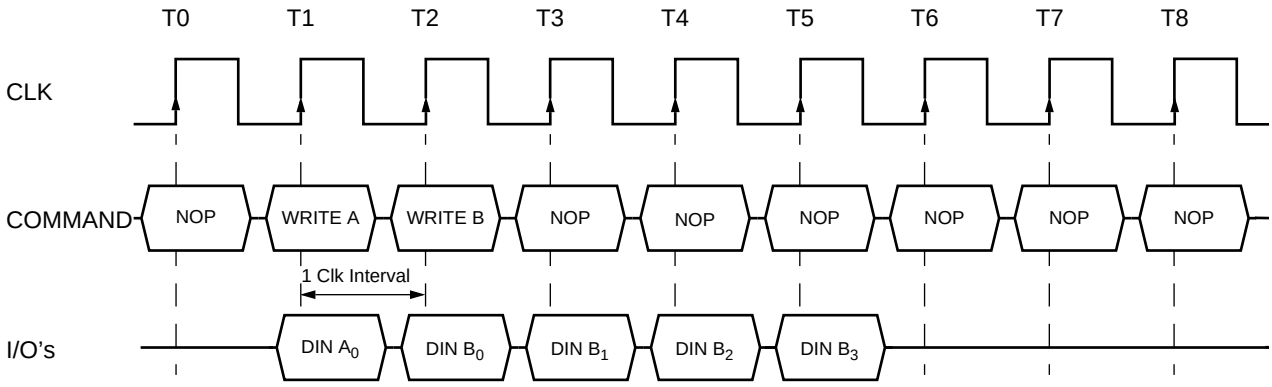
5. Burst Write Operation

(Burst Length = 4, $\overline{CAS}$ latency = 2, 3)



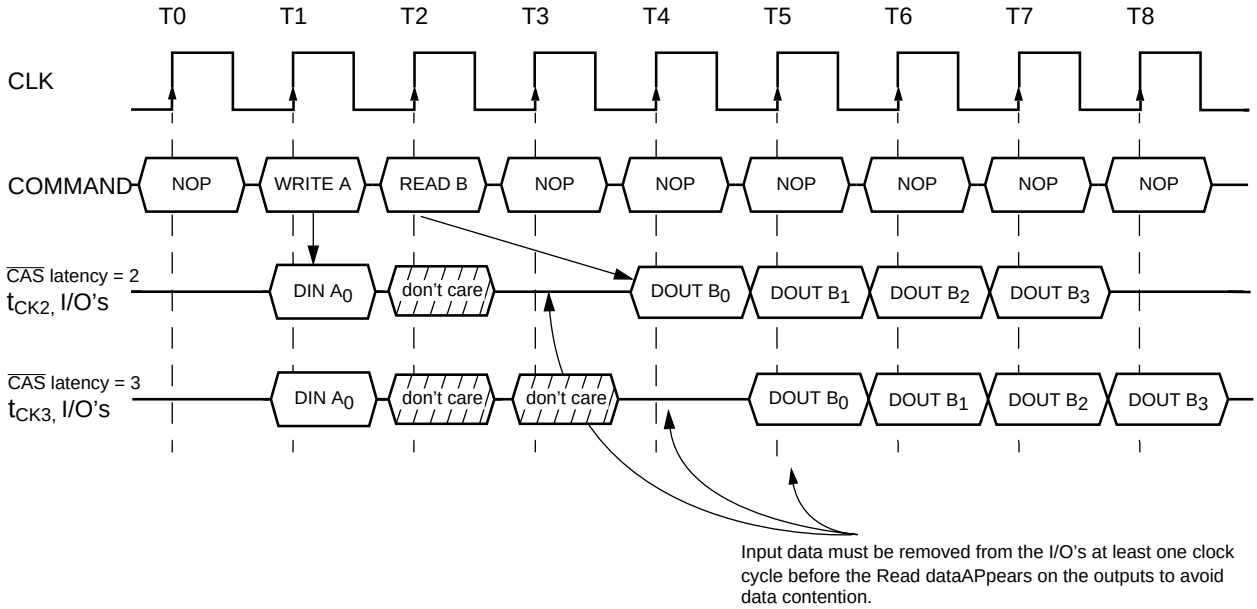
6.1 Write Interrupted by a Write

(Burst Length = 4, $\overline{CAS}$ latency = 2, 3)



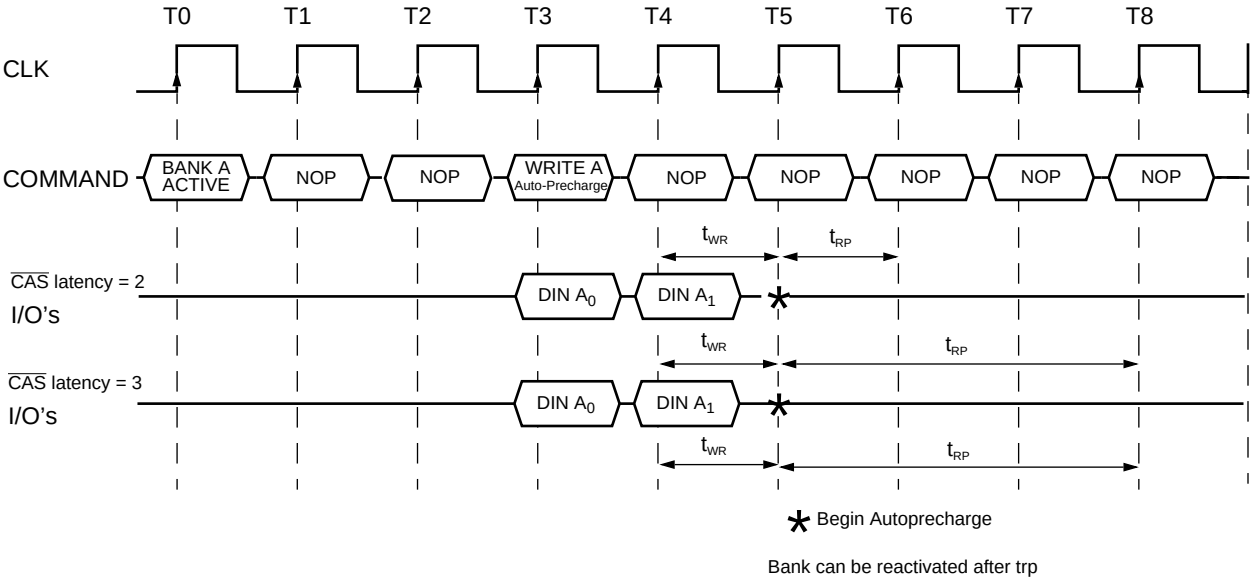
6.2 Write Interrupted by a Read

(Burst Length = 4, $\overline{CAS}$ latency = 2, 3)



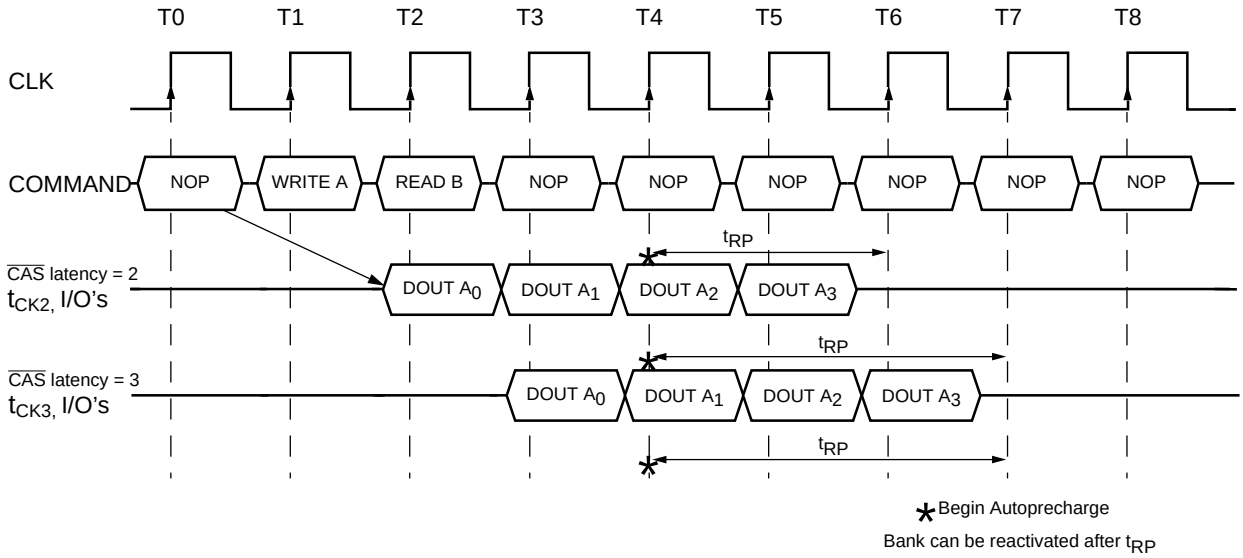
7. Burst Write with Auto-Precharge

Burst Length = 2, $\overline{CAS}$ latency = 2, 3)



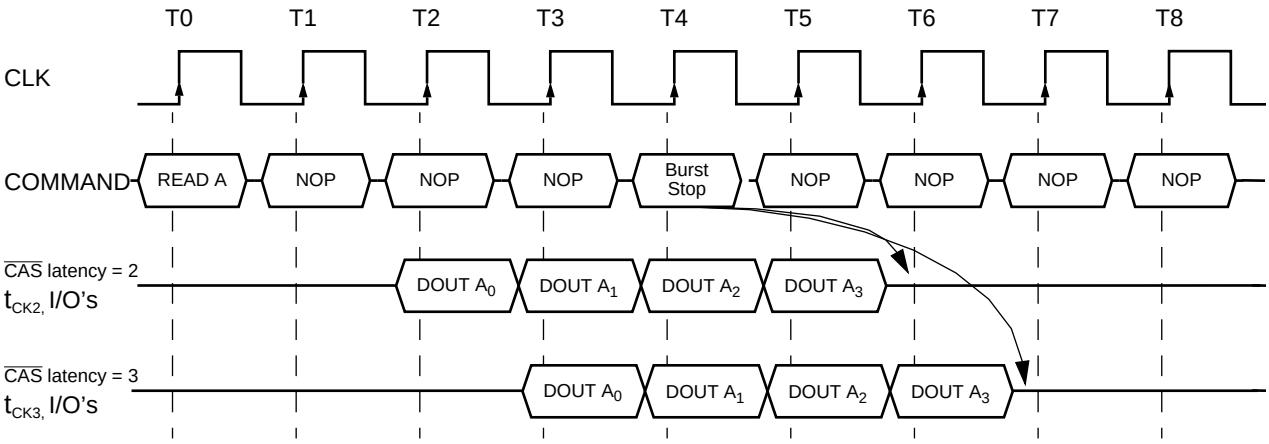
7.2 Burst Read with Auto-Precharge

Burst Length = 4, $\overline{CAS}$ latency = 1, 2, 3)



8.1 Termination of a Full Page Burst Read Operation

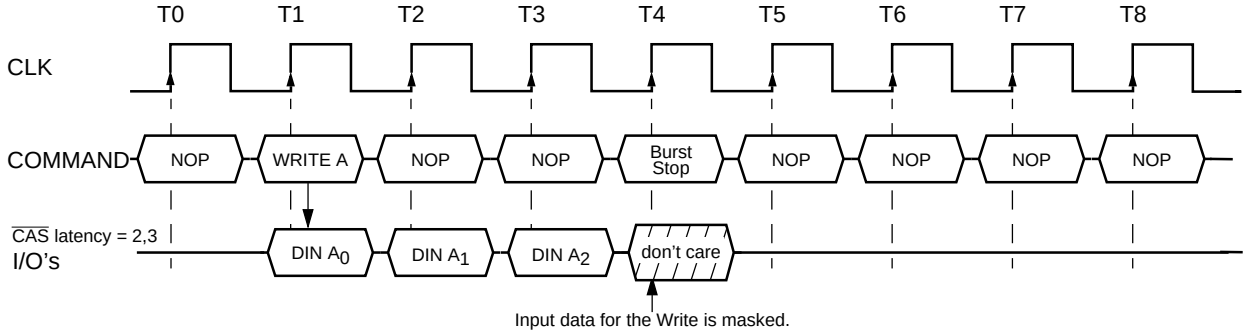
(CAS latency = 2, 3)



The burst ends after a delay equal to the CAS latency.

8.2 Termination of a Full Page Burst Write Operation

(CAS latency = 2, 3)

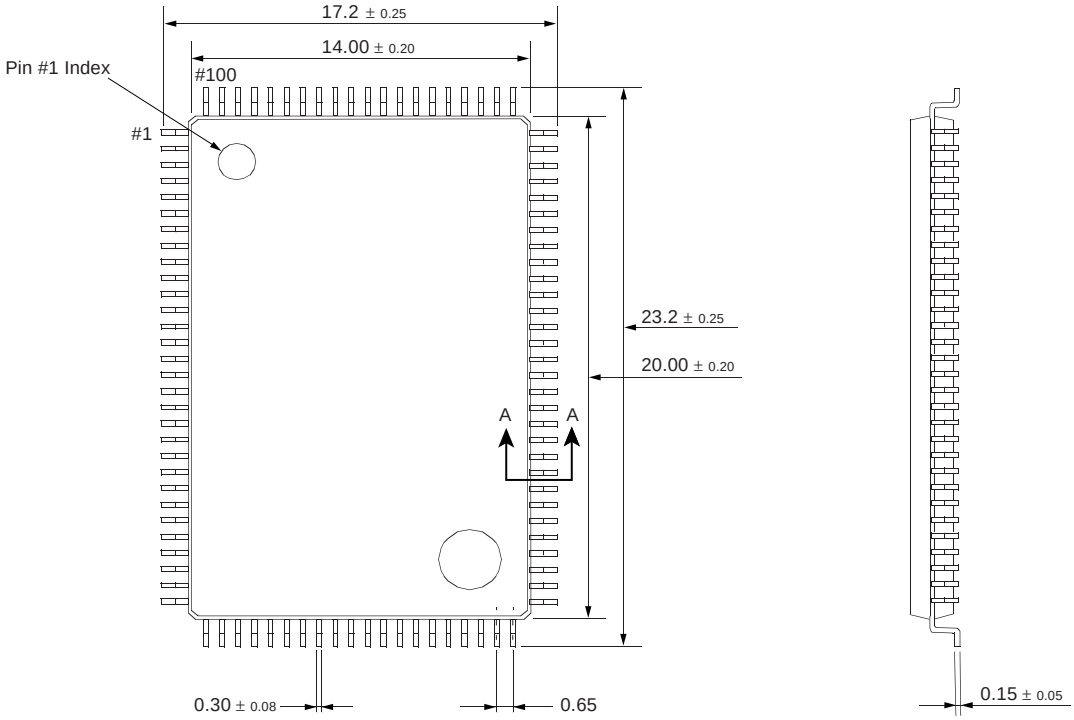


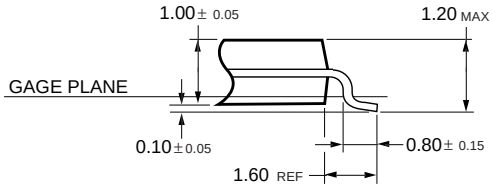
Input data for the Write is masked.

Package Diagram

100-pin TQFP

Dimensions in Millimeters





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