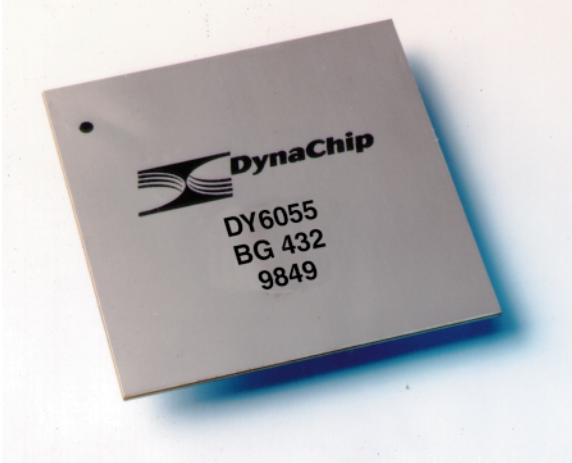
DY6000™ Family

FAST Field Programmable Gate Array™

Features

- Predictable, Fast, Patented Active Repeater™ Architecture
- I/O Data-Transfer Rates up to 200MHz
- 2.7ns I/O Clock-to-Output Time with 10pf Load; 3.2ns with 50pf Load
- 1.4ns I/O Input Register Setup Time
- 9,000 to 55,000 Usable Gates
- 32-Bit Synchronous 8ns-Access, Two-Clock, Two-Port SRAM in Every Logic Block, to Support 125MHz FIFOs
- Two PLLs for 8MHz-to-200MHz Clock Multiplication, Division, and Locking with Programmable Latency
- Ten Clock Trees with 200ps Worst-Case Clock Skew
- 150ps Worst-Case Pin-to-Pin Skew Between Registered Logic Outputs to Support Fast Buses
- In-System Reprogrammability
- Dynamic Single-Block Reconfigurability
- TTL, LV-TTL, GTL, and GTLP Interface Levels; 24mA IOL Drive for GTL, 48mA IOL Drive for GTLP
- Up to Nineteen LVDS-Compatible Input Pairs
- Up to Nineteen Differential LV-PECL Input Pairs
- 66MHz, 64-Bit, Zero-Wait-State PCI Soft Core
- 3.3V Operation with 5V-Tolerant I/O
- Hot-Swappability – no System Shutdown Required When Exchanging Circuit Boards
- JTAG (IEEE1149.1) Boundary-Scan Conformance
- Individual Slew-Rate Controls for Each Output
- Fully-Automatic Design Implementation Using DynaTool™
- 432-Pin EBGA and 240-Pin EQFP Packages



Applications Examples

- Data Communications: Gigabit Ethernet, ATM, Fibre Channel, Token Ring, SONET – Switching, Routing, CRC Functions
- Telecommunications
- High-Speed Graphics
- On-the-Fly-Reconfigurable Systems
- Servers and Supercomputers
- PCI Interfaces
- ASIC Emulation
- Semiconductor Testers
- High-Performance Instrumentation
- Medical Imaging Systems

Device	Gates	Logic Blocks	Max User SRAM Bits	Flip- flops	Clock Trees	I/O Blocks
DY6009	9,000	256	8,192	768	10	128
DY6020	20,000	576	18,432	1,536	10	192
DY6035	35,000	1,024	32,768	2,560	10	256
DY6055	55,000	1,600	51,200	3,840	10	320

Table 1: DY6000 Family

Table of Contents

Introduction

DynaChip's third generation DY6000 family of Fast Field Programmable Gate Array devices incorporate improvements in internal architecture and in I/O versatility. Fabricated using a deep-submicron CMOS process, this family of devices supports applications with system clock and I/O rates up to 200MHz – well above the rates achievable using conventional FPGAs.

All DY6000 family devices feature DynaChip's patented Active Repeater™ architecture, which provides shorter, highly-predictable internal routing path delays. Every I/O pin can be programmed to LV-TTL or GTL/GTLP interface levels as well as to standard-TTL and CMOS levels to support the fast data rates of high-performance applications.

Every logic block in DY6000 family devices contains 32 bits of synchronous two-clock two-port SRAM, with 8ns access time; an architecture particularly well suited to implementing many small, fast, distributed SRAMs or FIFOs in customer designs. In data rate matching applications, the FIFO can have completely independent read and write clocks.

High operating frequencies, on-chip distributed SRAM/FIFO, fast I/O, and PCI compatibility make DY6000 family devices ideal for high-performance data communications, telecommunications, graphics, and emulation applications.

The SRAM-based DY6000 family devices enable in-circuit configuration and reprogramming on-the-fly. Dynamic single-block reconfiguration is also possible, where a portion of the device may be reprogrammed without affecting the operation of the remaining logic. DY6000 family devices are hot-swappable, so system operation remains uninterrupted during power down for things like exchanging a circuit board.

DY6000 Enhancements

The DY6000 family incorporates numerous improvements:

- Wider functions in a single-logic level:
  - 8:1 Mux
  - 7-Input XOR
  - 2-Bit Full Adder
  - 2-Bit Identity Comparator
  - 9-Input AND Gate
  - 16-Input AND/OR Function
- Local Fast-Carry-Chain Paths:
  - Higher-Performance Full Adders
  - Higher-Performance Identity Comparators
  - Higher-Performance Parity and CRC Logic
- 125MHz Distributed Two-Clock Data-Rate-Matching FIFOs:
  - 32-Bit Two-Clock, Two-Port SRAM in Every Logic Block
  - Separate Write Clock and Read Clocks
- External Reference Voltage for I/O Blocks
  - Supports GTL and GTLP
- Higher-Current Drive:
  - 48mA I_{OL} in GTLP Mode (or 24mA I_{OL} in GTL Mode)
- Programmable PLL Latency:
  - Adjustable from -3.0ns to + 2.0ns in 150ps increments
- 19 LV-PECL/LVDS Differential Input Pairs
- Chip Power-Down Mode for ‘Green Design’

Performance Examples

All DY6000 family devices use DynaChip's patented Active Repeater™ architecture to support high-performance applications at clock rates and chip-to-chip data-transfer rates up to 200MHz. Active repeaters significantly reduce routing delays even for routing-intensive designs with high-fanout nets.

Table 2 gives the performance values of various macros implemented within a DY6055G (fastest speed grade) device over commercial voltage and temperature ranges.

Circuit	DY6055G	Logic Block Count
Fully-Synchronous Loadable Up-Counters:		
8-bit	145MHz	9
16-bit	140MHz	20
32-bit	125MHz	42
64-bit	100MHz	86
Adders:		
8-Bit, Using Carry Chain	7.5ns	5
16-Bit, Using Carry Chain	8.8ns	9
4x4 Pipelined Multiplier	145MHz	49
SRAM-Based FIFOs:		
32x32	125MHz	47
64-Bit Shift Register	160MHz	64

Table 2: Performance of Various Applications (Includes Routing Delays)

Assumptions: -G speed grade over commercial voltage and temperature range; 10pF load and fast slew-rate setting on outputs.

Notes: When measuring these performance values over industrial voltage and temperature ranges, derate the values by 5 percent.

When comparing DY6000 family FPGA performance with competing products, all values in Table 2 include all block routing delays within the same routing region.

The maximum chip-to-chip data-transfer rate is 250MHz assuming 10pF loads, GTL/GTLP interface levels, and the fastest slew rate.

High-Performance Active Repeater Technology

Active Repeater Routing, illustrated in Figure 2, is the enabling technology behind DynaChip's patented Fast Field Programmable Gate Arrays.

Conventional FPGA devices use pass gates to create programmable interconnections. When using multiple pass gates to create a net, they act like series resistors with distributed capacitance to ground, as shown in Figure 1. Nets formed as a series of these pass gates slow down dramatically as the number of programmable connections increases, resulting in long, unpredictable delays, especially for those nets which must traverse a long physical distance or drive a large number of loads.

In contrast, DynaChip DY6000-family devices use Active Repeaters to create programmable interconnections. As shown in Figure 2, these repeaters buffer the signal at every interconnection point and isolate the capacitance of the rest of the net.

The result is fast, predictable performance even for long, high-fanout nets.

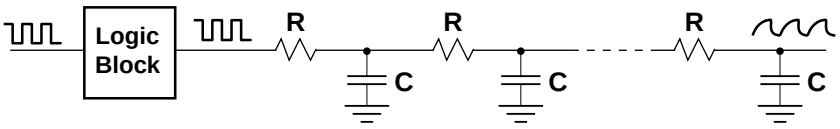


Figure 1: Pass Gates in Series Delay and Degrade Signals

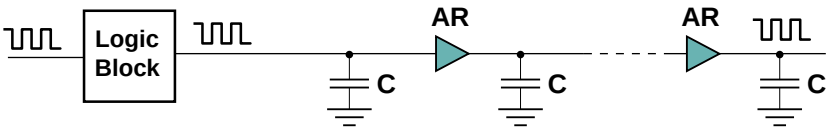


Figure 2: DynaChip's Active Repeaters Build Fast, Predictable Interconnect

Figure 3 illustrates a comparison of net delays between the two circuit technologies as the number of programmable interconnection points grow.

In FPGA devices using pass gate-based interconnect, net delays increase quadratically with the number of interconnection points, resulting in performance bottlenecks for long and/or heavily-loaded nets.

Conversely, using Active Repeater interconnect produces net delays which increase only linearly with the number of interconnection points, and are not affected by increased fanout, resulting in higher performance and superior predictability.

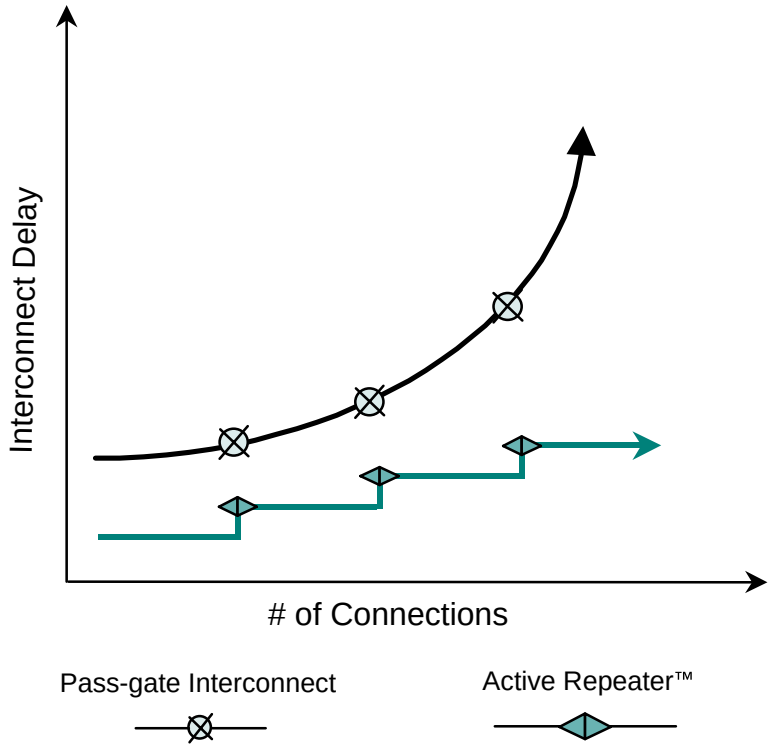


Figure 3: Active Repeater™ vs. Pass Gate Delays

Top-Level Architecture

Figure 4 illustrates the architecture common to all DY6000 family devices, but for a reduced number of blocks. A border of I/O blocks forms the outer perimeter of the device. A rectangular array of logic blocks occupies the device's interior. The spaces between these logic blocks form channels, which are filled by horizontal and vertical routing tracks.

The structure of the individual DY6000 routing tracks is entirely different from the corresponding structures in conventional FPGAs. The illustrations in Figure 1, Figure 2, and Figure 3 emphasize the effect of these differences. Using Active Repeaters eliminates the need for numerous levels of routing tracks of varying lengths, resulting in more predictable convergence to optimized solutions.

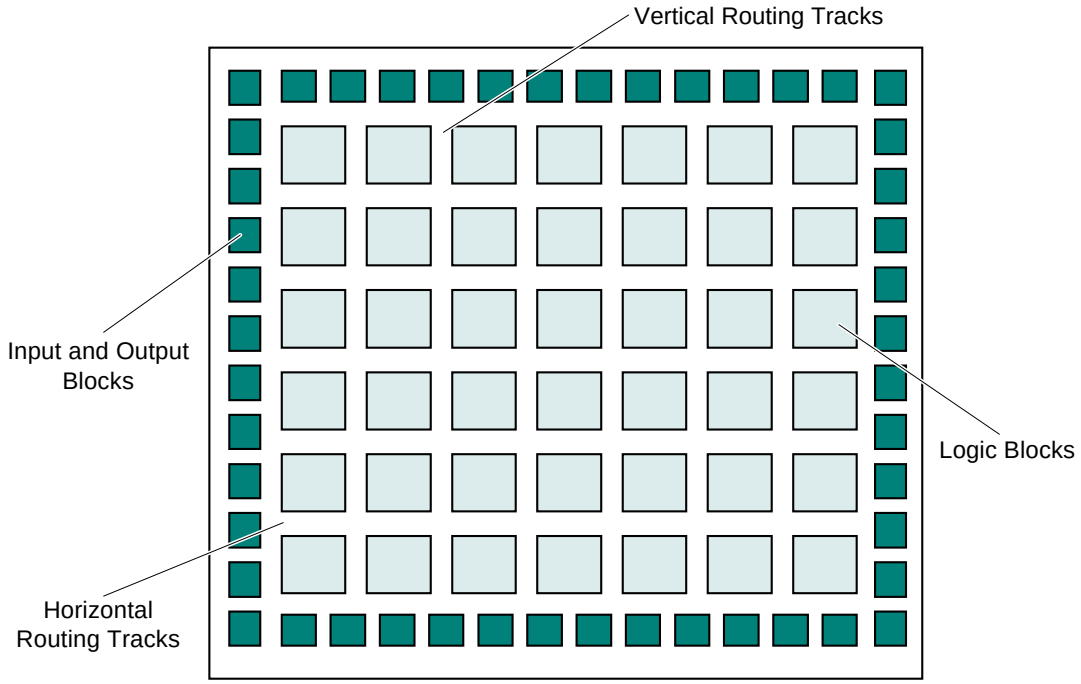


Figure 4: Overview of DY6000 Architecture

Routing Architecture

Dynachip's Active Repeater technology provides higher performance than more complex multi-level routing architectures.

As shown in Figure 5, a routing region consists of logic blocks and a set of horizontal and vertical routing tracks, interconnected by buffers controlled by programmable configuration SRAM bits. All routing is programmed by selecting which of these buffers to turn on; there are no pass gates or other passive routing types.

Active Repeater buffers drive fixed loads and are optimized for those loads. As a result, their logic delays are fixed and the performance of large complex user designs is deterministic and predictable. There are four types of Active Repeater buffers:

- Horizontal (Horizontal-to-Horizontal Bidirectional Buffers)
- Vertical (Vertical-to-Vertical Bidirectional Buffers)
- Vertical-to-Horizontal Connection Buffers
- Horizontal-to-Vertical Connection Buffers

As shown in Figure 5, each DY6000 logic block has its own nine-block local routing region; three rows high by three columns wide. The Active Repeaters are staggered so that every block has an associated routing region, which overlaps the routing regions of nearby blocks.

Routing regions are connected via bidirectional Active Repeater buffers. A signal which has passed through an Active Repeater is available throughout the next routing region.

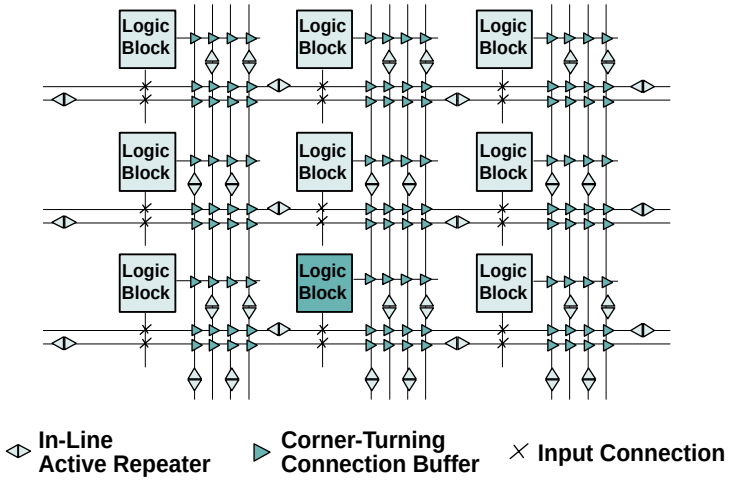


Figure 5: Routing Architecture

This architecture allows a logic block to drive all nine logic blocks in its 3x3 routing region, with no additional routing delays even for high-fanout nets, shown in Figure 6. Performance is completely deterministic within that routing region.

The DY6000 parameters presented in Table 26 allow designers to accurately estimate performance because they include all connection buffer delays and other routing delays within the logic block's 3x3 routing region. The DY6000 parameters presented in Table 27 show logic block delays without any connection buffer or routing delays and are useful for comparing the DY6000 to other FPGA technologies.

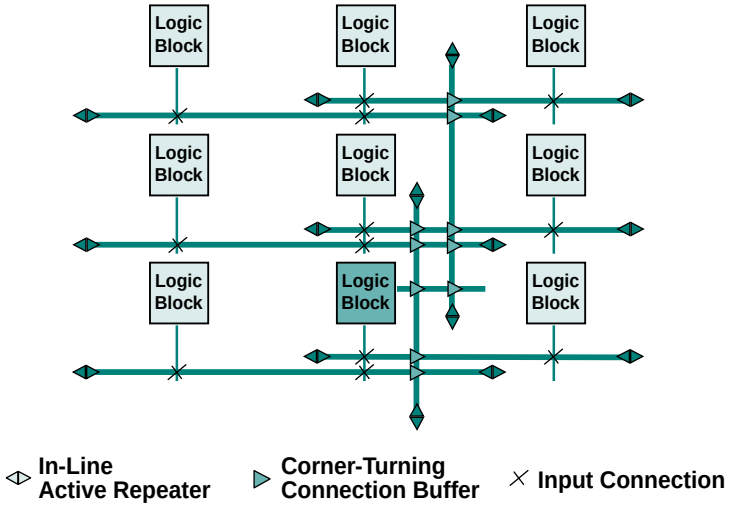


Figure 6: Routing Region With No Interconnect Delay

For a signal driving a block or blocks within the next region, the fixed delay through one Active Repeater is added to the logic block delay. Thereafter, an additional Active Repeater delay is added for every two logic blocks the signal traverses. Figure 7 shows the number of logic blocks that can be driven with 0, 1, and 2 active repeaters.

Active Repeater delays are the only routing delays in a DY6000 device. Active Repeaters performance values are given in Table 30 at the end of this data sheet.

Each logic block typically implements twenty logic gates or thirty-two SRAM bits. The total logic and memory resources which may be reached with 0, 1, or 2 Active Repeater delays are shown in Table 3, and are illustrated in Figure 7.

Active Repeater Delays	Logic Blocks	Gates	SRAM Bits
0	9	180	288
1	33	660	1,056
2	73	1,460	2,336

Table 3: Accessing Neighboring Logic Blocks

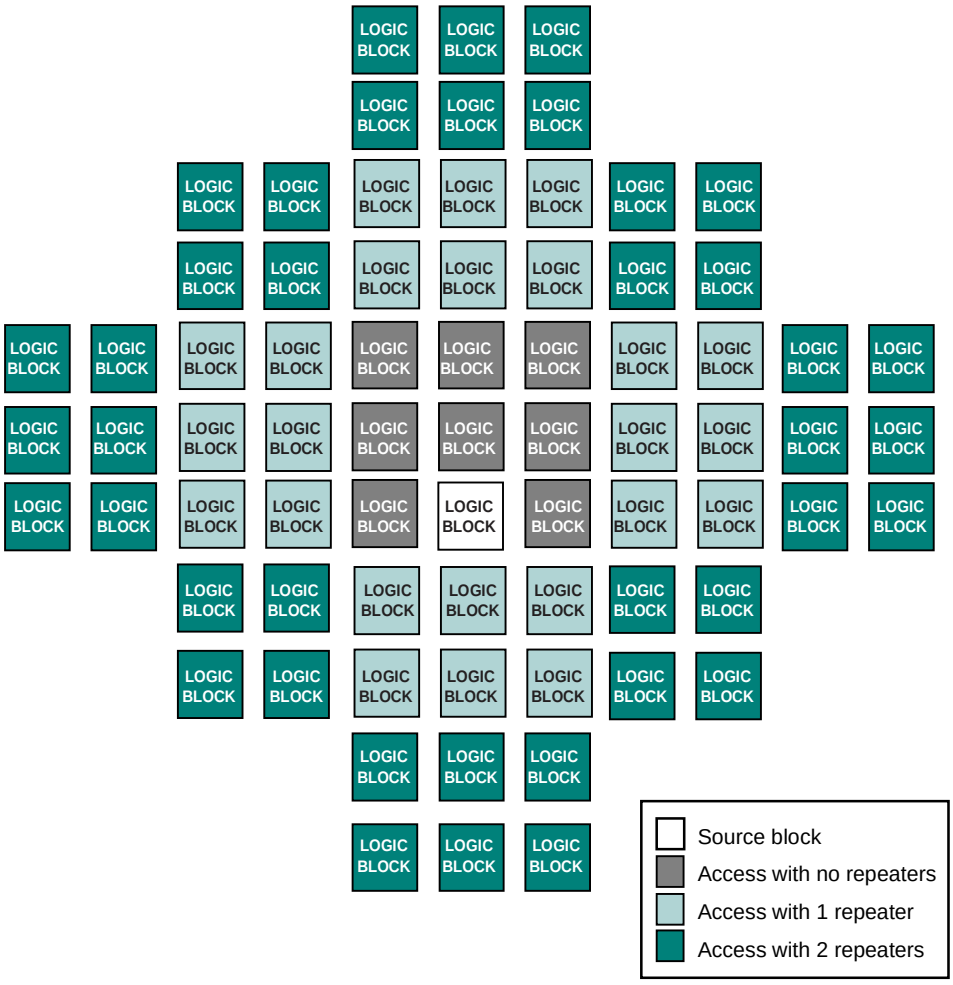


Figure 7: Logic Blocks Reachable with 0, 1, or 2 Active Repeaters

Input/Output Blocks

DY6000 I/O block structure is illustrated in Figure 8. Each I/O block includes an input flip-flop and an output flip-flop, both featuring clock enables.

Every I/O block may be set independently to accommodate either LV-TTL (5V tolerant) or GTL/GTLP interface levels. However, GTL levels and GTLP levels may not be mixed on the same physical FPGA chip.

Thirty-eight of the I/O blocks have slightly different input circuitry to accommodate LV-PECL and/or LVDS input signals as well as LV-TTL and GTL/GTLP signals. These 38 I/O can be configured as 19 differential pairs or 19 single-ended inputs. When used as LV-PECL or LVDS, these I/O can be used as inputs only. These inputs are not 5V tolerant.

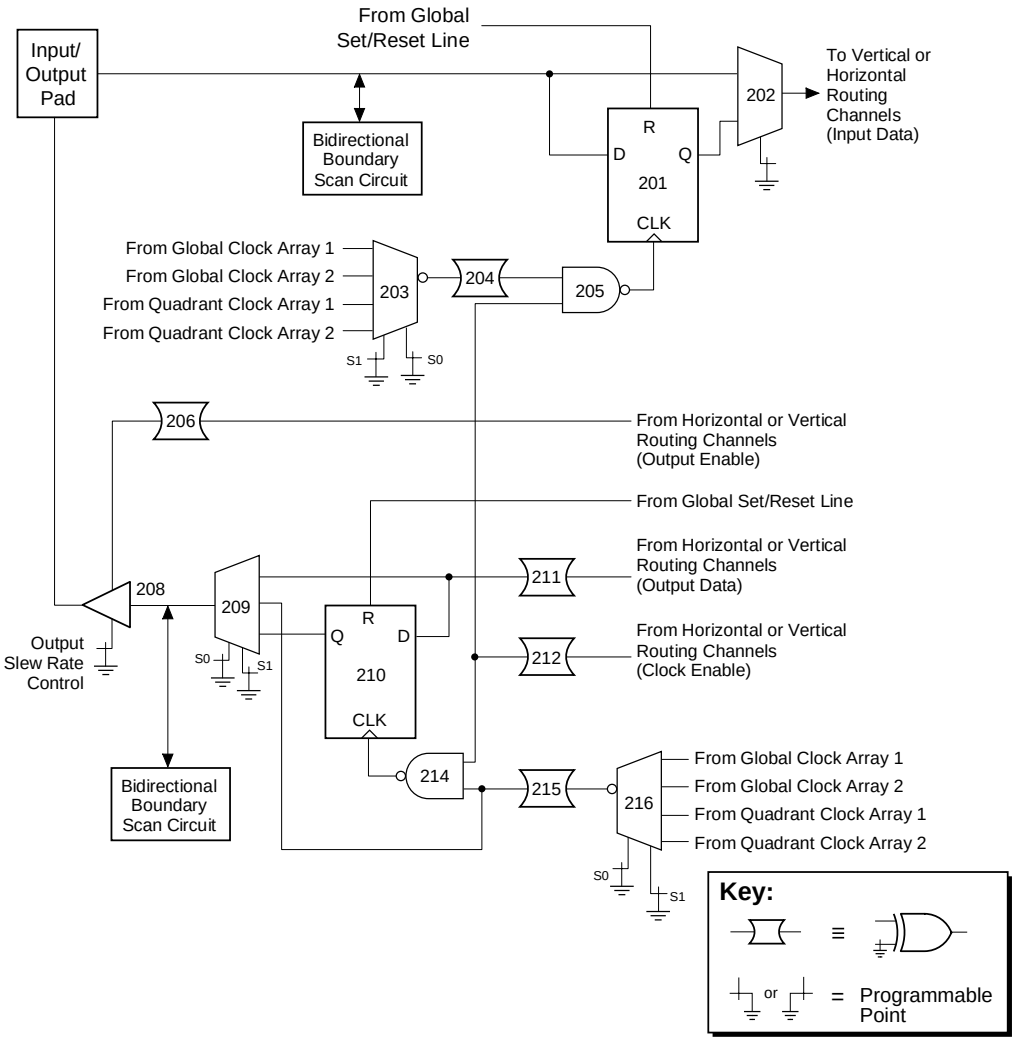


Figure 8: Input/Output Block

Note: The numbers within the logic symbols are used by DynaTool to identify particular logic elements.

Each I/O block may be configured to handle input, output, or bidirectional signals. Clock signals for either of the two flip-flops in an I/O block may come from either of the two global clocks which serve the entire chip, or from either of the two quadrant clocks which serve that particular region of the device.

Each output has its own individual slew rate control and three-state enable control. An output's slew rate may be set to be fast, medium, or slow, regardless of the settings for other outputs on the chip, unless it's GTL/GTLP-compatible.

Each output also is equipped with high-resistance, individually-programmable active pull-up and active pull-down elements. Using DynaTool, you can connect the pullup, connect the pulldown, or leave both of them unconnected so that the output can float. Connecting both the pullup and the pulldown elements simultaneously is not allowed.

With an I/O supply voltage of 3.3V, the current in a pull-up or pull-down element is limited to less than 100µA.

Each I/O block includes JTAG Boundary Scan logic, conformant to the IEEE 1149.1 (JTAG) Specification.

LVDS

Any of the 19 LV-PECL capable input pairs can interface directly to LVDS levels. To use these inputs at LVDS levels, you must place a shunt resistor between the input pairs, as illustrated in Figure 9.

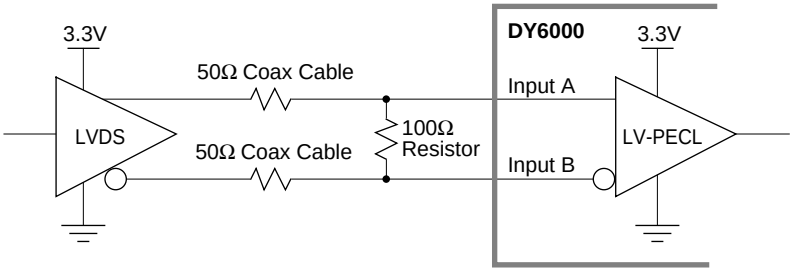


Figure 9: Interfacing LVDS to LV-PECL using Two DY6000 Inputs

External GTL/GTLP and LV-PECL Reference Voltage

The DY6000 I/O blocks can use an external reference voltage. Any I/O block may be programmed to use this externally-supplied reference voltage. Recommended voltage settings for GTL, GTLP, and LV-PECL are:

Required Compatibility	Reference Voltage
GTL	0.8V ± 5%
GTLP	1.0V ± 5%
LV-PECL	(V_{CC} - 1.3V) ± 5%

Table 4: Recommended Settings for Reference-Voltage Input

The GTL and GTLP settings are two-thirds of the recommended termination voltage VTT.

Using an external reference voltage is mandatory for GTLP and optional for GTL and LV-PECL. If the external reference voltage is not used, internal reference voltage is provided.

Logic Blocks

The DY6000 Logic Block, simplified in Figure 10, and shown fully in Figure 11, contains AND, OR, and XOR gates, flip-flops, muxes, and a 32-bit, two-clock, two-port SRAM, making this block versatile and powerful. DynaTool™ (DynaChip's development system) automatically maps logic from the designer's application into these logic block resources.

One logic block may implement a two-bit full adder or identity comparator, a nine-input AND gate, a seven-input XOR parity tree, an 8:1 multiplexer, and other logic functions of comparable complexity.

The logic block includes sixteen general purpose logic inputs, plus Clock and Set/Reset inputs. All inputs are equipped with polarity control circuits, which may be programmed to pass their signals either as noninverted (true) or as inverted (false). There are also two Global Clock Inputs, two Quadrant Clock Inputs, a Global Set/Reset Input, and 'Top' and 'Bottom' Carry Inputs.

There are three logic outputs, plus 'Top' and 'Bottom' Carry outputs. The three logic outputs may be driven by the logic blocks' combinatorial logic, its flip-flops, or its SRAM. Two of the logic outputs can be direct or registered. The third output is always direct.

The Carry inputs and outputs form two fast-carry paths through the logic block, a 'Top' path and a 'Bottom' path, providing high-speed routing to the logic blocks immediately above and below the given logic block. These fast-carry paths are useful for speeding up adders, identity comparators, and XOR functions. For adder applications, the delay of carry signals using these fast-carry paths consists of an initial delay required to access the fast-carry path, an incremental delay for each two bits in the adder, and a final delay required for exiting the fast-carry path.

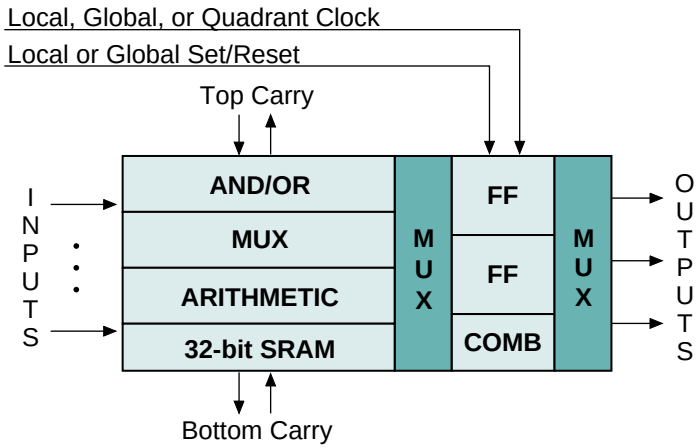
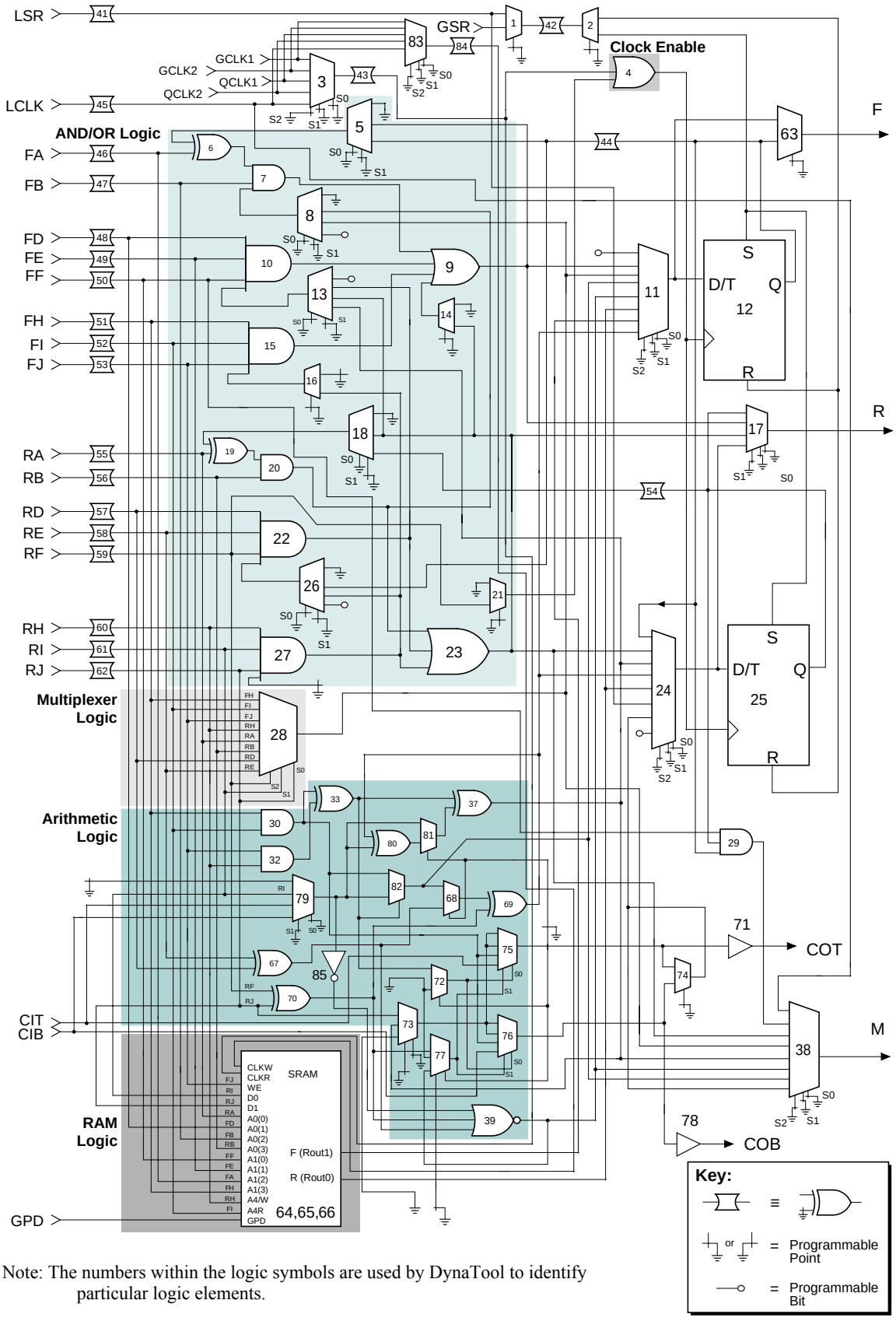


Figure 10: Conceptual Diagram of Logic Block

The functional areas shown in Figure 10 are the AND/OR logic section, multiplexer section, arithmetic logic section, and the thirty two-bit, two-clock, two-port SRAM section.

Each block includes two flip-flops that are configurable to either a D-type or T-type element. Both flip-flops are clocked from one of five sources (local clock (LCLK)), two global clocks (GCLK1 or GCLK2), or two quadrant clocks (QCLK1 or QCLK2), which serve this region. Flip-flops can be programmed to be active on either the rising or the falling clock edge.



Note: The numbers within the logic symbols are used by DynaTool to identify particular logic elements.

Figure 11: Schematic Diagram of Logic Block

The two flip-flops share a common set/reset signal from either of two sources: local interconnect (LSR), or the FPGA's global set/reset (GSR). The set/reset input has programmable polarity control. You may choose assertive-HIGH operation or assertive-LOW operation for resetting the two flip-flops, although your choice must be the same for both. Likewise, you may configure the two flip-flops together to use either a set operation or a reset operation.

SRAM

Each logic block in a DY6000-family FPGA includes 32 bits of fully-synchronous dual-port, two-clock SRAM with three configuration options:

- One 32x1 two-port SRAM.
- One 32x1 single-port SRAM.
- Two separate 16x1 single-port SRAMs.

Functional block diagrams corresponding to each of these configurations are shown in Figure 12, Figure 13, and Figure 14. All signals are one-bit except for addresses, which are five-bit for the two 32x1 configurations, and four-bit for the double-16x1 configuration.

The SRAM has separate read and write clocks. Either of these clocks may originate from any of five sources: local interconnect (LCLK), either of the FPGA's two global clocks (GCLK1 or GCLK2), or either of the FPGA's two quadrant clocks (QCLK1 or QCLK2) serving that region of the chip. For the two single-port configurations, the write clock and the read clock are automatically tied together.

For any of the three SRAM configurations, both writing and reading are synchronous operations.

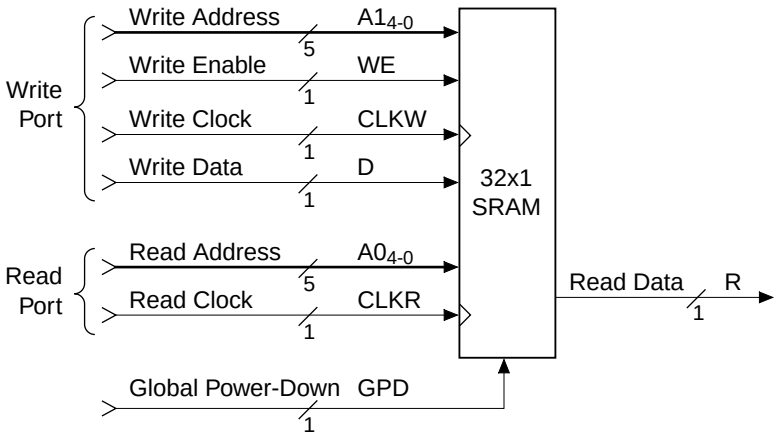


Figure 12: 32x1 Two-Port SRAM

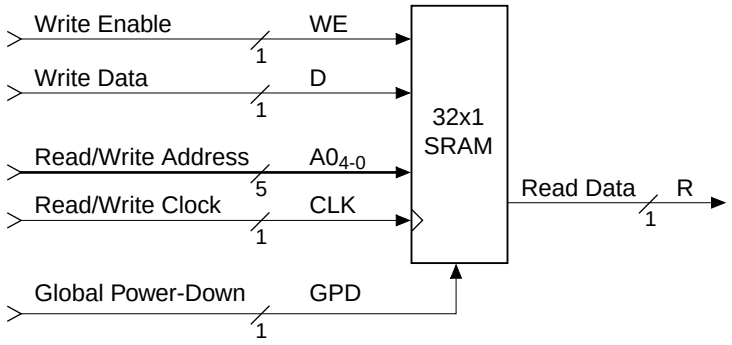


Figure 13: 32x1 Single-Port SRAM

On a rising edge (a LOW-to-HIGH transition) of the write clock, the WE, address, and data inputs are latched. If WE is HIGH, the data is written to the RAM in the same clock cycle. Writing is a single-clock operation. While a write operation is in progress, the state of the SRAM's data output(s) is indeterminate.

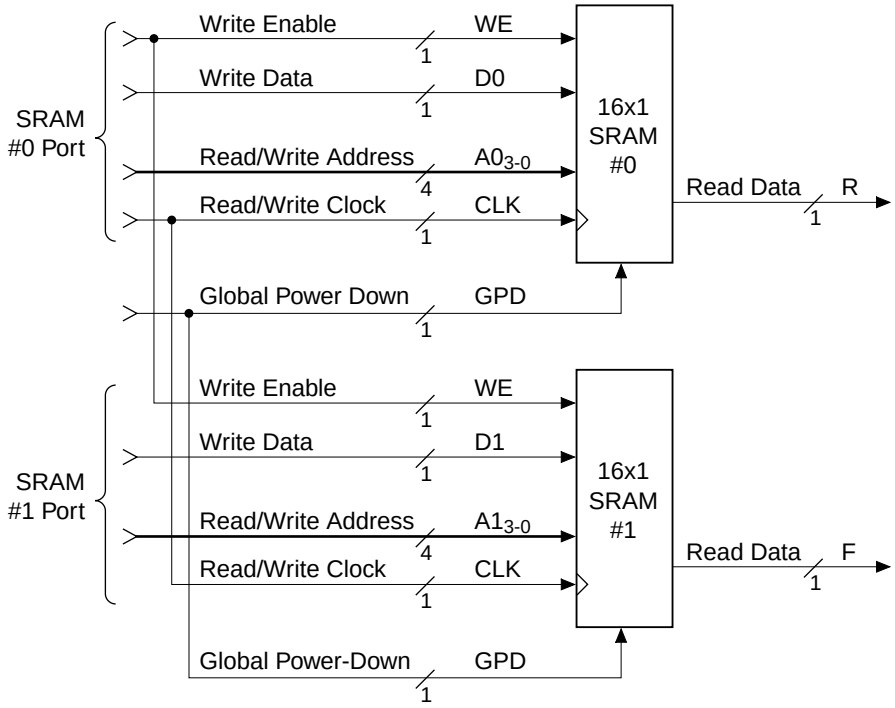


Figure 14: Two Separate 16x1 Single-Port SRAMs

On a rising edge of the read clock, the RAM outputs are latched and are available at the RAM output(s). Reading is a single-clock operation.

The two-port SRAM configuration has a separate write port and read port, with separate read address and clock signals. Single-port configurations have common read/write clocks and addresses.

For two single-port configurations, SRAM is in write mode whenever WE is asserted and in read mode whenever WE is not asserted.

For two-port configurations, the SRAM is always in read mode regardless of the state of WE, except when a read-write collision occurs; that is, when an attempt is made to read and write the same location at the same time. In this case, writing takes precedence over reading, and the data output is indeterminate.

Timing waveforms for the SRAM write and read operations are shown in Figure 15, Figure 16, and Figure 17. Figure 15 and Figure 16 apply to the 32x1 two-port configuration. Figure 15 is for the common case where the write and read addresses are not the same, and Figure 16 applies to the 'read-write collision' case where the addresses are the same. Figure 17 applies to both the 32x1 single-port configuration and the two-16x1 single-port configuration.

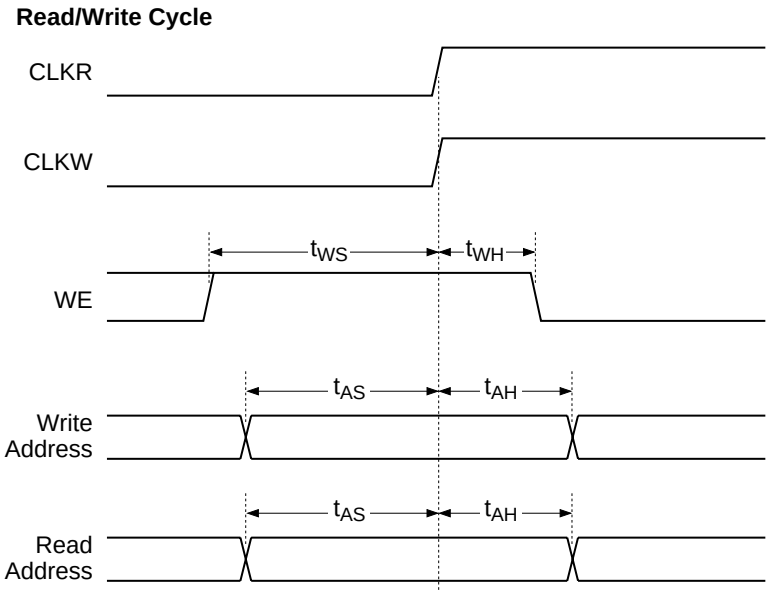


Figure 15: Two-Port SRAM Read/Write Cycle, with Differing Write and Read Addresses

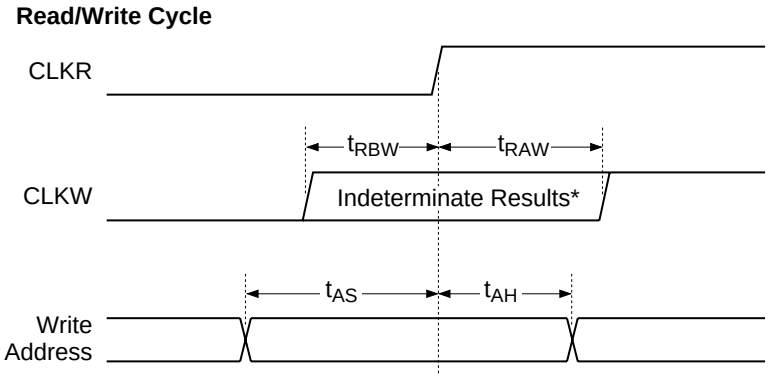


Figure 16: Two-Port SRAM Read/Write Cycle, with Identical Write and Read Addresses

* If the rising edge of CLKW occurs in this region, the output is indeterminate.

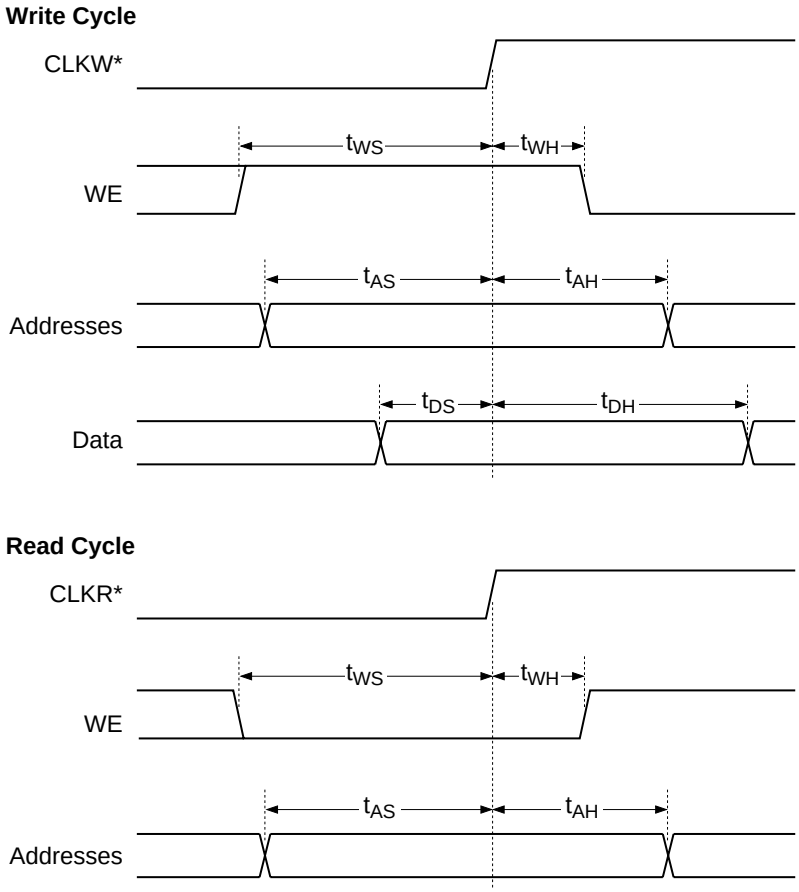


Figure 17: Read/Write Cycle Timing for Single-Port SRAM Configurations

* For single-port operation, CLKW and CLKR are automatically tied together.

The SRAM may be powered down by using the Global Power-Down (GPD) signal. This signal must meet setup-time and hold-time conditions with respect to a clock (write or read), if the entry or exit from powered-down mode is to be effective as of that clock. In powered-down mode, the SRAM bits retain their previously stored information, but cannot be written into or read from as long as the powered-down mode remains in effect, as illustrated in Figure 18.

The GPD signal (pin name IO3/PECL1_GPD) is not 5V tolerant.

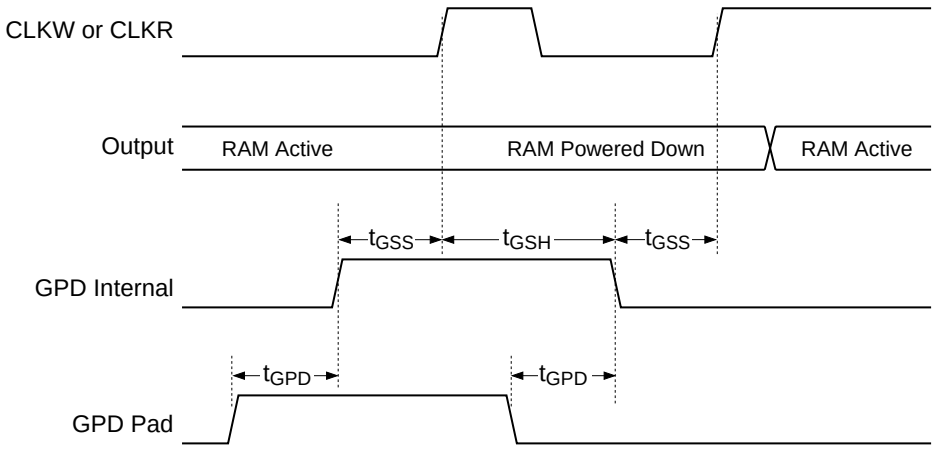


Figure 18: SRAM Power-Down Cycle

Clock Distribution

DY6000-family FPGAs have ten low-skew clock distribution networks. Two of these are global networks which access the entire device; the other eight are quadrant networks which access one quarter of the device. Each of the ten clock networks can be driven from a package pin, from the PLLs, or from signals generated within the FPGA. A signal on any of the ten clock networks can be driven off-chip through package pins.

Every logic block can use any of five clock signals:

- either of the two global clocks
- either of the two quadrant clocks in the quadrant
- local interconnect clock (LCLK) generated by the user's logic

Every I/O block can use any of four clock signals:

- either of the two global clocks
- either of the two quadrant clocks in the quadrant.

The input pins that drive the 10 clock networks are programmable to LV-TTL, GTL, GTLP, single-ended LV-PECL, differential LV-PECL, or differential LVDS interface levels.

Clock inputs are not 5V tolerant.

Phase-Locked Loops

DY6000 devices contain two PLLs for clock latency reduction, clock multiplication, and clock division.

Each of the two PLLs drive one global clock network and four quadrant-clock networks. The PLLs multiply and divide clock signals by 1, 2, 3, 4, 6, or 8.

By default, the PLL reduces clock latency to zero. The latency may be programmed in 150ps increments, over the range of -3ns to +2ns.

A filter is required for the PLL power supply. Refer to DynaChip's PLL application note for more information on the filter requirements.

External resistors can be connected to device pins PLL1REST and PLL2REST for signal optimization. For most applications, these pins should be tied to ground.

PLL1 is located in the top-left corner of the chip, and can drive GCLK1, QCLK1TL, QCLK1TR, QCLK1BL, and QCLK1BR. PLL2 is located in the top-right corner of the chip, and can drive GCLK2, QCLK2TL, QCLK2TR, QCLK2BL, and QCLK2BR.

The PLLs support a clock frequency of 8MHz to 200MHz. Table 5 shows the supported input frequency range for different multiplication factors.

Multiplier	Minimum Input Frequency	Maximum Input Frequency
1	25*	200
2	24	80
3	19	52
4	14	40
6	10	26
8	8	20

*Contact the factory for additional information on applications that require a 1x multiplier at frequencies below 25 MHz.

Table 5: PLLs' Supported Input Frequency Ranges

Figure 19 shows, in simplified form, the clock networks for the entire chip.

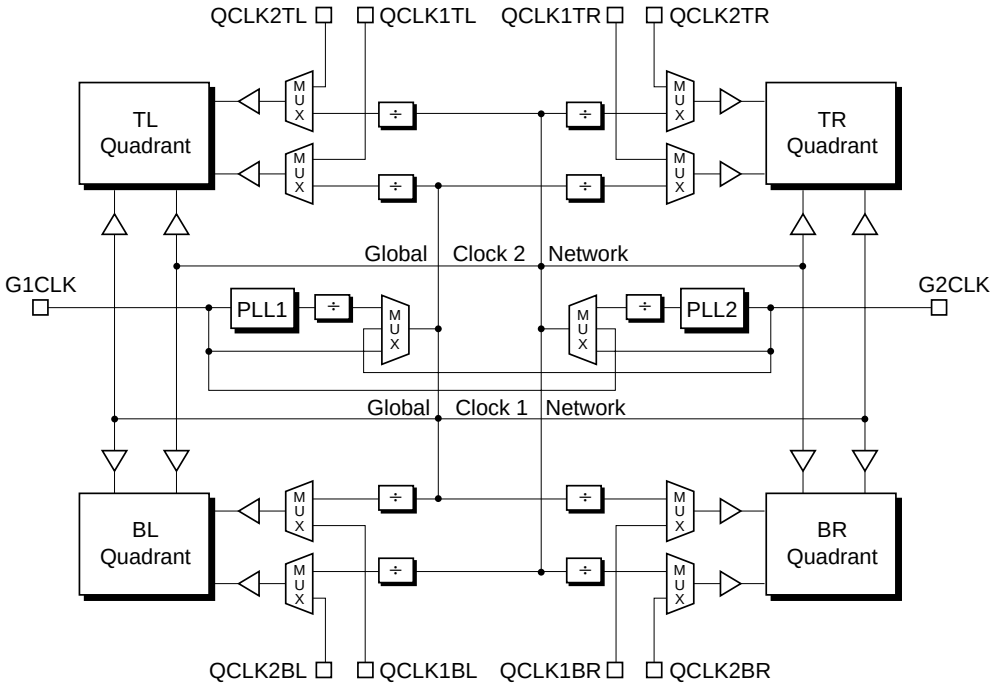


Figure 19: PLL and Clock Networks

If the jitter of the incoming clock is 100ps or less, then the jitter of the clock signal produced by the PLL is less than 350ps over commercial voltage and temperature range, or 450ps over industrial voltage and temperature range.

Power Consumption

Power consumption for a DY6000 device depends upon:

- the number of I/O logic blocks, SRAM bits, clocks, and PLLs used.
- the operating frequency.
- the operating supply voltage.
- the number of outputs used.
- the I/O interface-levels (TTL or GTL/GTLP) and the slew-rate settings.
- the speed grade of the FPGA.

In general, on-chip logic resources draw power only if programmed to do something.

Power consumption is frequency-dependent, and also depends upon the percentage of flip-flops which are switching on each clock. For power estimates, it is reasonable to assume that 25% of the flip-flops in a design are switching on each clock.

In addition, DY6000-FPGA power consumption is affected by the actual core and I/O supply voltages, which are nominally 3.3V.

Faster speed grade devices typically consume more power. The power consumption increases by approximately 10% per speed grade.

Advance Estimates

A methodology for a first-order estimate of power dissipation is provided here. DynaTool reports a more accurate power estimate. The estimation process is divided into two parts: one for the dynamic power drawn by the internal resources when they are clocked, and one for the static power being drawn by the FPGA regardless of the clock.

For the dynamic power estimate, there is a baseline typical power-dissipation value, which assumes the use of a 3.3V power supply, 100MHz operation, and a 30pf capacitive load on each active output. There are also sensitivity values for each volt of supply voltage, each 1MHz of frequency, and each pF of capacitive loading on output pins.

Two values are given for logic and I/O blocks. One value for blocks where the logic is strictly combinatorial, and the other for blocks where a flip-flop is included for registered operation.

Element	Baseline Estimate (mW)	Voltage Sensitivity (mW/V)	Frequency Sensitivity (mW/MHz)	Output-Loading Sensitivity (mW/pF)
Combinatorial Input*	2.43	0.96	0.013	0
Registered Input*	4.62	3.99	0.017	0
Combinatorial Output*	17.85	7.06	0.033	0.33
Registered Output*	18.81	5.51	0.033	0.33
Combinatorial Logic Block*	5.78	0.50	0.026	0
Registered Logic Block*	7.03	3.86	0.013	0
PLL	22.44	10.00	0.155	0
Global Clock	340.43	160.22	6.755	0
Quadrant Clock	85.11	40.06	1.690	0

*These numbers should be multiplied by the percentage of the design that is switching on each clock (Typically 12% to 25%).

Table 6: Typical Switching Power Consumption

For the static-power estimate, it's assumed that the FPGA is *idle* – that is, that no flipflops are switching, either in the logic blocks or in the I/O blocks. The most obvious method of placing the FPGA into this condition is to disable all clock networks, by some means either on-chip or off-chip.

The components of static power are:

- standby power.
- bias power.
- static PLL power.
- memory static power.

Standby power is drawn by the entire FPGA when all are flip-flops disabled from switching and when all SRAM bits are subject to Global Power-Down (GPD).

Bias power is drawn whenever any I/O blocks are programmed to GTL/GTLP or PECL interface levels. If the external-voltage-reference pin is used, the voltage present on it may affect bias power. If any I/O blocks are programmed to GTLP levels, this external-voltage-reference pin must be held to a voltage suitable for GTLP.

Static PLL power is that which is drawn by a PLL at zero frequency.

Memory static power is drawn by the 32-bit memory in logic block when the block is programmed and power down is not asserted. Here, the power drawn depends upon the memory configuration; the 32x1 two-port configuration draws twice as much static power as the single-port configurations.

For static power, there is a baseline typical value at 3.3V, and a sensitivity value for how the indicated parameter changes with voltage.

Item	Baseline Estimate in mW/Item	Voltage Sensitivity in mW/V
Standby Power (Entire Chip)	5.1	3.8
Bias Power (Entire Chip)	6.6	3.2
Static PLL Power (per PLL)	6.6	3.2
Static Single-Port Memory (per 32 Bits)*	2.6	1.2
Static Dual-Port Memory (per 32 Bits)*	5.3	2.5

Table 7: Typical Static Power Consumption

* This item becomes zero when GPD (General Power-Down) is asserted.

Configuration

Configuration memory in the DY6000 stores programming bits that control operation of all programmable elements in the device. These programming bits are called a bitstream.

The configuration memory is volatile and does not retain information when the FPGA is powered off. The configuration process must be repeated at each power up.

If only a portion of the FPGA's resources are used, the bitstream needs to include only the bits necessary to program those resources.

Table 8 gives the maximum possible number of bitstream bits for each DY6000-family FPGA.

Device	Array	Maximum Number of Programming Bits
DY6009	16x16	235,524
DY6020	24x24	304,856
DY6035	32x32	452,696
DY6055	40x40	686,776

Table 8: Maximum Number of Programming Bits

The configuration mode is controlled by the state of mode pins M2, M1, and M0. If these mode pins are left unconnected, a weak pulldown resistor holds them LOW to logic '0.' Table 9 shows the mode pin states required for each configuration mode.

Configuration Mode	M2	M1	M0
Mode 0 Serial/Internal Last	0	0	0
Mode 1 Serial/External Last	0	0	1
Mode 2 (Reserved for Future Use)	0	1	0
Mode 3 Readback	0	1	1
Mode 4 Serial/External Not Last	1	0	0
Mode 5 Parallel/External Last	1	0	1
Mode 6 Parallel/External Not Last	1	1	0
Mode 7 Full-Chip Reset	1	1	1

Table 9: Mode-Pins Settings

The Readback Mode 3 may be used to read the bitstream from a configured FPGA to determine if the bitstream has been properly loaded.

Configuration Pin Usage

There are two categories of configuration pins: dedicated and dual-purpose. Dedicated pins are always reserved for their configuration function. Dual-purpose pins have a configuration function during downloading and become user I/O after configuration.

The dedicated pins are: PCKI/PCKO, STPRGM, RESET, and SYSDONE. The dual-purpose pins are: M2, M1, M0, DONE, D7, D6, D5, D4, D3, D2, D1, D0, WE, RDY, and DOUT. In the Serial Configuration modes 0, 1, and 4, dual-purpose pins are used as follows:

- M2, M1, M0, and D0 are used for configuration during download and readback.
- DONE is used for configuration during download and readback, only if several FPGAs are 'chained.'

- DOUT is used for configuration only if readback is required.
- The remaining dual-purpose pins are not used for downloading or readback.

In the Parallel Configuration Modes 5 and 6, the dual-purpose pins are used as follows:

- M2, M1, M0, D7, D6, D5, D4, D3, D2, D1, D0, WE, and RDY are used for downloading and/or readback.
- DONE is for downloading and/or readback only when several FPGAs are chained.' Otherwise, this pin is available for I/O connections.
- DOUT is used only if readback is required. Otherwise, this pin is available for I/O connections in user designs.

DynaChip FPGAs are capable of being partially reconfigured during operation; however, the dual-purpose pins used for configuration downloading and/or readback must be reserved, and are not available as user I/O connections. Otherwise, dual purpose I/O becomes available when configuration completes.

Configuration Modes

Three Serial Configuration Modes are available, described previously in Table 9, and below in Table 10.

Serial Configuration Mode	Description
Mode 0 – Serial/Internal Last	This mode is used in two situations: 1) To program a single DY6000 device from a serial PROM. In this mode, the DY6000 device generates a clock signal to drive the serial PROM. 2) For the last DY6000 device, in a programming chain that uses a serial PROM. In this mode, the DY6000 device generates a clock signal to drive both the serial PROM and the other DynaChip devices in the chain.
Mode 4 – Serial/External Not Last	This mode is used for each DY6000 device, except for the last DY6000 device, in a programming chain that uses a serial PROM – regardless of the source of the programming clock.
Mode 1 – Serial/External Last	This mode is used in two situations: 1) To program a single DY6000 device, using a serial bitstream and a user-supplied clock. 2) For the last DY6000 device, in a programming chain that is programmed using a serial bitstream and a user-supplied clock.

Table 10: Serial Configuration Modes

Two Parallel Configuration Modes are available, described previously in Table 9, and below in Table 11.

Parallel Configuration Mode	Description
Mode 5 – Parallel/External Last	This mode is used in two situations: 1) To program a single DY6000 device from a microprocessor. 2) For the last DY6000 device, in a programming chain that uses a microprocessor.
Mode 6 – Parallel/External Not Last	This mode is used for each DY6000 device, except for the last DY6000 device, in a programming chain that uses a microprocessor.

Table 11: Parallel Configuration Modes

There are nine possible cases when reconfiguring a DY6000 FPGA, as indicated in Table 12. These cases are determined by:

- Bitstream format – bit-serial, or byte-parallel.
- Clocking source – internal FPGA, or from an external clock.
- Loading position – standalone, or chained.
- If chained, loading position within the chain – not last, or last.

One combination of these choices, byte-parallel with internal clocking from within the FPGA, is not supported by DY6000 family FPGAs.

Although there are no mode or clocking differences between the ‘Standalone FPGA’ case and the ‘Chained FPGAs – Last’ case, presented inTable 12, their wiring connections are different, as illustrated in the Figures to which each case refers.

Format and Clock	Standalone FPGA	Chained FPGAs	
	Last (Only)	Not Last	Last
Serial/Internal	Mode 0 – Serial/Internal Last ~ 2.5MHz Clock, Generated Within FPGA, Output on PCKO See Figure 20	Mode 4 – Serial/External Not Last ~ 2.5MHz Clock, From Last FPGA, Input via PCKI See Figure 21	Mode 0 – Serial/Internal Last ~ 2.5MHz Clock, Generated Within FPGA, Output on PCKO See Figure 21
Serial/External	Mode 1 – Serial/External Last ≤ 15.0MHz Clock, Supplied Externally, Input via PCKI See Figure 22	Mode 4 – Serial/External Not Last ≤ 15.0MHz Clock, Supplied Externally, Input via PCKI See Figure 23	Mode 1 – Serial/External Last ≤ 15.0MHz Clock, Supplied Externally, Input via PCKI See Figure 23
Parallel/External	Mode 5 – Parallel/External Last ≤ 2.5MHz External Handshake Signals; Input via WE, Output on RDY See Figure 24	Mode 6 – Parallel/External Not Last ≤ 2.5MHz External Handshake Signals; Input via WE, Output on RDY See Figure 25	Mode 5 – Parallel/External Last ≤ 2.5MHz External Handshake Signals; Input via WE, Output on RDY See Figure 25

Table 12: Serial and Parallel Modes and Clock Sources for Configuration

Clocking for the three main configuration methods has the properties given in Table 13.

Mode	Clock Source	Frequency	Bit Rate
Serial/Internal	Last/Only FPGA	Approximately 2.5MHz	~ 2.5Mbs
Serial/External	External System	At Most 15.0MHz	≤ 15.0Mbs
Parallel/External	External System	At Most 2.5MHz	≤ 20.0Mbs

Table 13: Configuration Clocking Ground Rules

For the Parallel/External method there is no 'clocking' per se. Rather, a handshake exchange occurs between a microprocessor and the FPGA being downloaded. The microprocessor asserts Write Enable (WE) to signal the FPGA a byte is ready to be loaded, and the FPGA responds by asserting ReaDY (RDY) when the data has been read and the device is ready for the next byte.

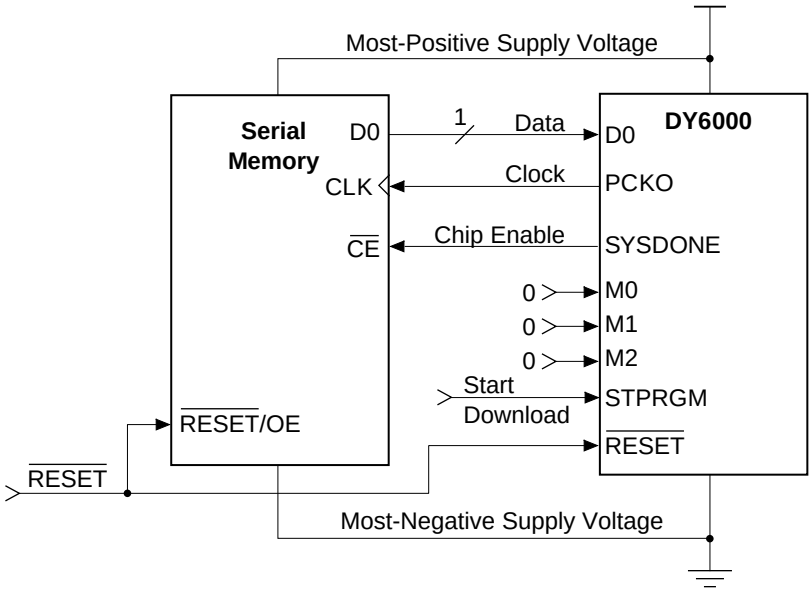


Figure 20: Serial/Internal Configuration, Standalone

The Serial/Internal method uses the fewest external resources. The Serial/External method is the fastest since you can supply a clock up to 15 MHz. The Parallel/External method is useful when a microprocessor is contained within the system.

The setup for the Serial/Internal method consists of only a serial-output Programmable Read-Only Memory (PROM) and one or more DY6000 FPGAs. With one standalone FPGA, the internal oscillator within the FPGA is the clock source both for that FPGA and for the PROM, as shown in the interconnections illustration in Figure 20. With two or more FPGAs in a chain, the last FPGA is the clock source for both the PROM and the entire chain, as shown in the interconnections illustration in Figure 21. A standalone, or last, FPGA operates in Mode 0; a not-last FPGA operates in Mode 4. The frequency of the standalone or last FPGA's internal oscillator, nominally about 2.5MHz, determines the bit-transfer rate for the PROM and the FPGA(s).

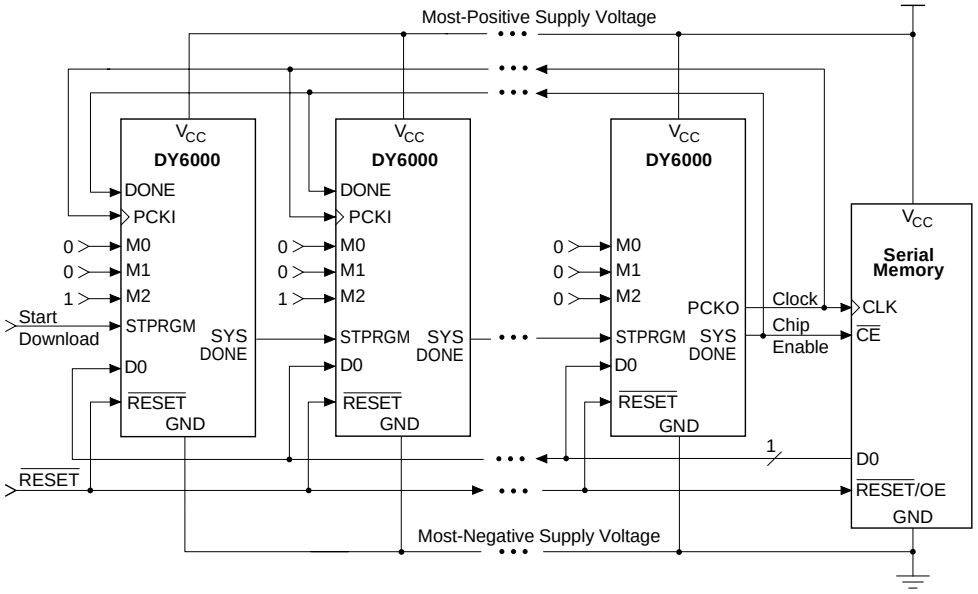


Figure 21: Serial/Internal Configuration, Chained

The setup for the Serial/External method differs from the Serial/Internal method only in that the clock comes from some an outside source. The interconnections for a standalone FPGA are shown in Figure 22, and for a chain of two or more FPGAs in Figure 23. Here, a standalone or 'Last' FPGA operates in Mode 1; a not-last FPGA operates in Mode 4. The bit transfer rate for the PROM and the FPGA(s) is determined by the frequency of the outside clock source, which may be any frequency up to 15.0MHz.

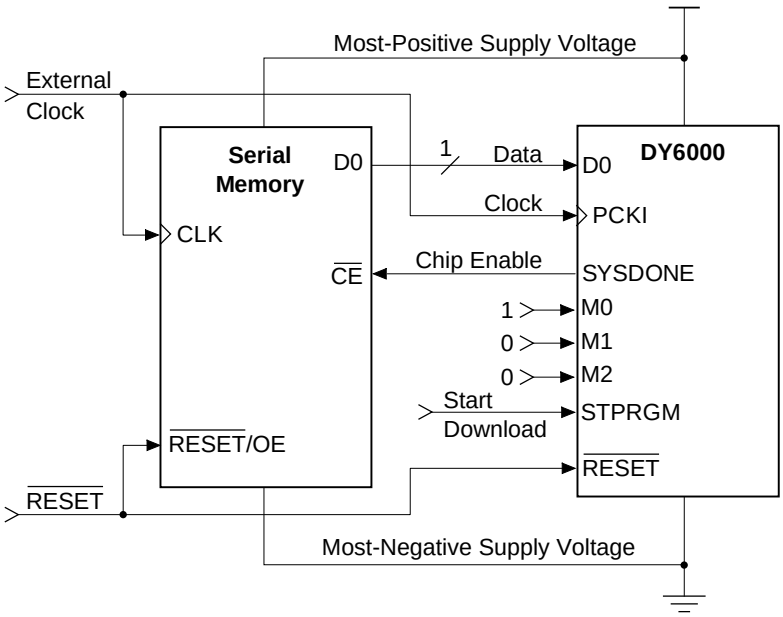


Figure 22: Serial/External Configuration, Standalone

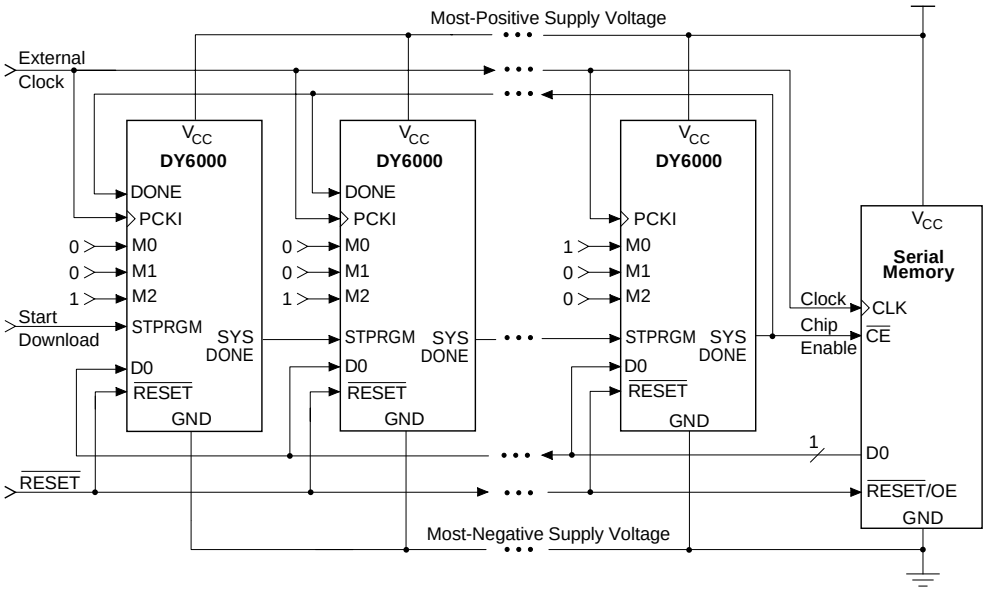


Figure 23: Serial/External Configuration, Chained

For the Parallel/External method, there is handshake signaling between the microprocessor and the FPGA. The interconnections for a standalone FPGA are shown in Figure 24, and for a chain of two or more FPGAs in Figure 25. Here, a standalone or 'Last' FPGA operates in Mode 5; a not-last FPGA operates in Mode 6. The byte transfer rate is determined by the frequency of the handshake, which should not exceed 2.5MHz. Thus, the maximum bit-transfer rate is eight times that value, which 20.0MHz.

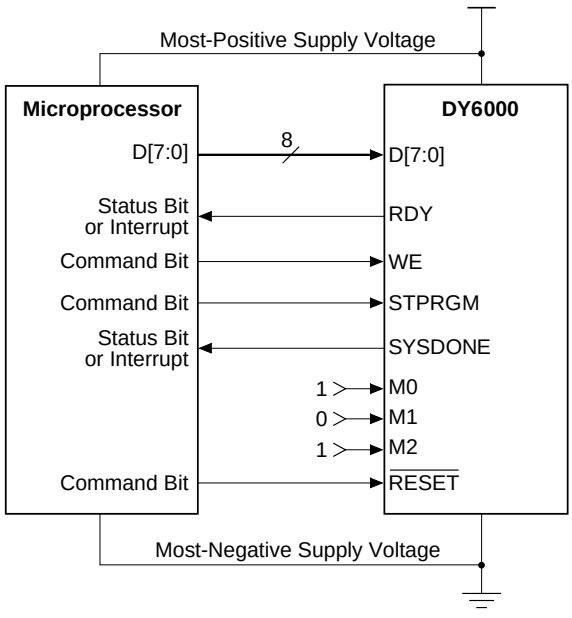


Figure 24: Parallel/External Configuration, Standalone

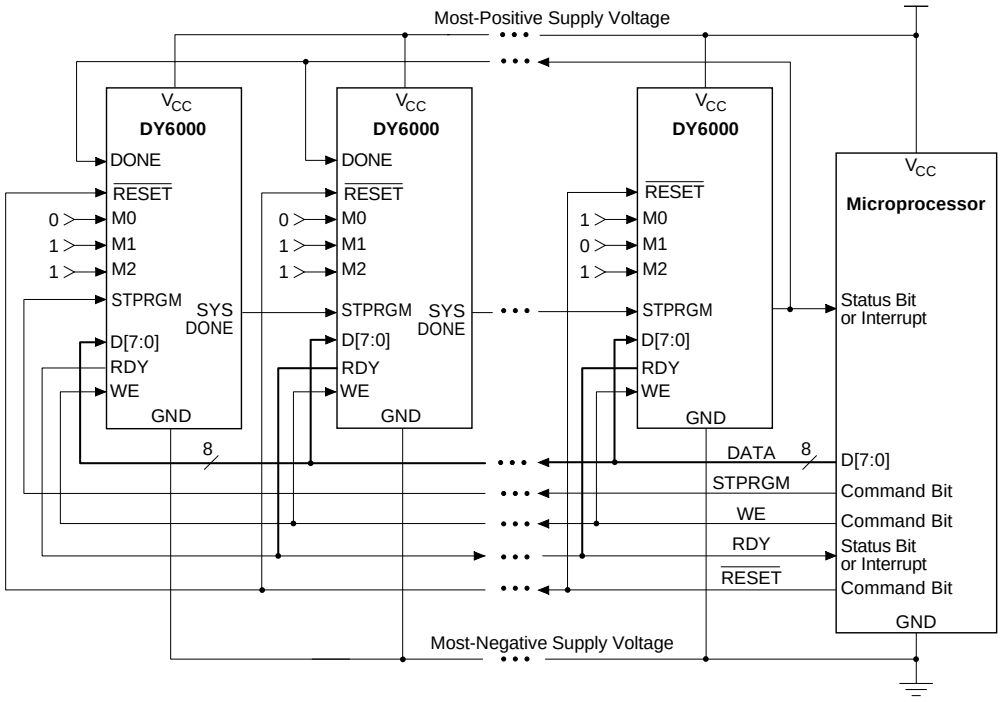


Figure 25: Parallel/External Configuration, Chained

In all configuration modes, the programming process is launched by asserting the STart PRoGraM (STPRGM) input. When that FPGA has received enough bits that its portion of the programming process is complete, it asserts its SYStem DONE (SYSDONE) output. When two or more FPGAs are chained, the SYSDONE output of the (n)th FPGA is connected to the STPRGM input of the (n+1)st FPGA.

An FPGA in one of the Serial modes treats an incoming clock on Programming ClocK Input (PCKI) as an edge-sensitive signal, and responds to the positive (rising) edge. The same is true in one of the Parallel modes for an incoming handshake signal on WE.

Reconfiguration and Resetting

The DY6000 has three different reset capabilities:

- **Full-Chip Reset**—All configuration bits, logic-block flip-flops, I/O flip-flops, and RAM bits are reset to the LOW state. Full-Chip Reset may be initiated from two different methods:
  - Automatically initiated whenever the FPGA device is powered up.
  - Initiated by the external system without shutting off power by applying the code for Mode 7 to M2, M1, and M0, then asserting the RESET input. (The pin for RESET is ‘RESETN’ in the pin list, and is an assertive-LOW input.) This is typically used for applications that reprogram the entire FPGA in system.
- **Partial Reconfiguration Reset**—All configuration bits in the region being configured are overwritten with new values, and all flip-flops and RAM bits in this region are reset. This is typically used for applications that reprogram a portion of the FPGA in system.

Logic-block flip-flops and RAM bits in regions that are not reconfigured are unaffected. Partial Reconfiguration Reset must be initiated by the external system without shutting off power by applying the code for any mode except for Mode 7 to M2, M1, and M0, then asserting the RESET input.

- **Global System Reset**—No configuration or RAM bits are affected. All logic block flip-flops are either set or reset according to their design definition, and all I/O block flip-flops are reset. Refer to the Logic Block discussion and to Figure 11. Global System Reset is initiated by the external system without shutting off power by asserting the GSR input. (The pin for GSR is 'GSR/GSR' in the pin list, and is an assertive-HIGH input.)

Reprogramming, after a Full-Chip Reset, must occur in one of Modes 0, 1, 4, 5, or 6. Figure 26 gives representative timing waveforms, for the case where Mode 1 (Serial/External Last) is to be used for reprogramming. During programming, M0 is HIGH and M1 and M2 are LOW. Figure 26 shows the minimum required timing for asserting $\overline{\text{RESET}}$ (LOW).

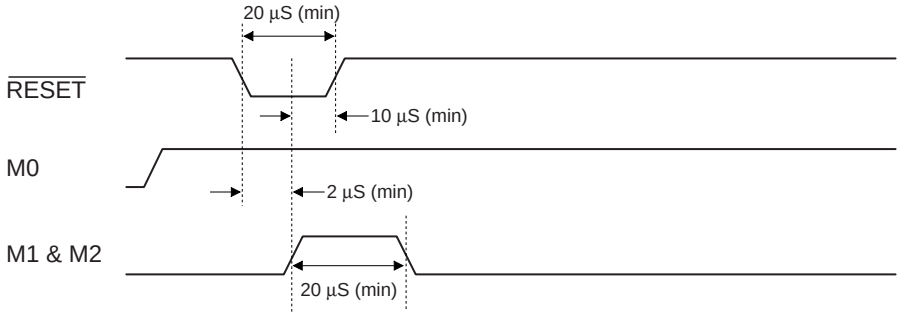


Figure 26: Full-Chip Reset in Serial/External Last Mode

Configuration-Related Pins

Two types of pins are used in the configuration process. Fixed-function pins are always dedicated for configuration usage. Dual-purpose pins have special configuration functions and become user-assignable I/O pins after device configuration.

Pin	Name	Type	Function
PCKI/PCKO	Programming Clock Input/Output	Fixed-Function	This pin has two different functions, depending on the programming mode: 1) If the device is the only device to be programmed or is last in a programming chain, and an external clock is not being used, this pin is an output that provides a master clock to all other devices and to the serial PROM. 2) If the device is in a programming chain and is not the last device, or if an external user-supplied clock controls the configuration process, this is an input pin which receives the clock from a source outside the FPGA. When the FPGA is not being programmed, the functionality of this pin defaults to that of PCKI.
STPRGM	STart PRoGraM	Fixed-Function	This pin initiates the configuration process. Depending on that FPGA's position (standalone, not last, or last) it receives an input either from the external system, or from the previous FPGA in the chain.

Table 14: Configuration-Related Pins

Pin	Name	Type	Function
RESETN	$\overline{\text{RESET}}$	Fixed-Function	This pin controls changes in the configuration memory. In Mode 7, it causes Full-Chip Reset – clearing of the entire configuration memory, to the LOW state, for all bits. In other configuration modes, it causes writing of the incoming bitstream over specified portions of the configuration memory. Figure 26 shows the timing required for proper operation of Full-Chip Reset.
SYSDONE	SYStem DONE	Fixed-Function	This output pin is dedicated for programming. It can be configured as a CMOS or an open drain output. When configured as an open drain output, an external pull-up resistor is required. Once configuration has been completed, SYSDONE goes from LOW to HIGH.It stays HIGH until either the power is turned off, or a RESET signal is applied. If the FPGA is the last or only device to be programmed, this pin signals that configuration has been completed. If the FPGA is the last one in a programming chain, this pin signals all other devices that programming has been completed, and to return to normal operation. This signal may also be used to control the enabling and disabling of an external serial PROM(s).
M2, M1, M0	Mode	Dual-Purpose	These pins are inputs during programming. They control the mode used for configuring the FPGA. The configuration-mode pins are listed in Table 9. These pins become I/Os during normal operation. If the mode pins are not connected, they are pulled down to a logic ‘0.

Table 14: Configuration-Related Pins

Pin	Name	Type	Function
DONE	DONE	Dual-Purpose	This is an input pin during programming which is used only in a chained-multiple-device configuration mode. If the device is not the last one in the chain, the DONE pin is tied to the SYS-DONE pin of the last device. A LOW-to-HIGH transition on this pin signals that programming has been completed and the device begins normal operation. This pin can be used as an I/O during normal operation.
D0	Data	Dual-Purpose	This is an input in during programming. It accepts serial data from an outside source. It can also accept the LSB (Least-Significant Bit) from a byte-wide memory or a microprocessor bus. This pin can be used as an I/O during normal operation.
D7 - D1	Data	Dual-Purpose	These are data-input pins for the parallel configuration modes. They are activated only after the $\overline{\text{RESET}}$ signal has been applied. Together with D0, they accept byte-wide data loaded from a parallel source such as a microprocessor. They can be used as I/Os during normal operation.
WE	Write Enable	Dual-Purpose	This is an input pin for the parallel configuration modes. It is activated only after the RESET signal has been applied. This pin is used by the microprocessor to signal the DY6000 that an eight-bit byte has been placed on the D[7:0] inputs. This pin becomes an I/O during normal operation.

Table 14: Configuration-Related Pins

Pin	Name	Type	Function
RDY	ReaDY	Dual-Purpose	This is an output pin for the parallel configuration modes. It signals an external microprocessor that one eight-bit byte has been loaded, and that the device is ready to receive the next byte. Together with RDY, it provides 'handshake signaling' to coordinate the data-transfer process. This pin can be used as an I/O during normal operation.
DOUT	Data OUT	Dual-Purpose	This output pin supplies the bitstream during readback. This pin can be used as an I/O during normal operation.

Table 14: Configuration-Related Pins

JTAG

All devices in the DY6000 family provide JTAG (Joint Test Action Group) Boundary Scan, conformant to the IEEE1149.1 specification. This feature simplifies the testing of boards incorporating devices in surface-mount packages, or in packages with closely-spaced pins.

Four JTAG instructions are supported, as shown in Table 15.

JTAG Instruction	Register	Opcode
SAMPL/PRE	BSC	`1000`
EXTEST	BSC	`0000`
BYPASS	BYPASS	`1111`
IDCODE	ID	`1101`

Table 15: JTAG Instructions

The JTAG ID register is read when the DY6000 device is reset, and when the `1101` opcode is loaded. Upon power-up, the opcode defaults to `1101`. Internal pullup resistors are provided on the TDI and TMS pins.

The DY6000 JTAG ID number is:
`0000.0110.0000.0101.0101.000.1011.1001.1`
(hexadecimal 06055, followed by 0B91 in irregularly-spaced fields).

Product Specifications

Maximum Ratings

Symbol	Description	Value	Unit
V_{CC}	V_{CC} Pin Potential to GND Lead	-0.5 to +5.0	V
V_{IN}	Input Voltage Normal Pins Low-Voltage Pins	 -0.5 to V_{CC} + 0.5 -0.5 to +3.6	 V V
V_{TS}	Voltage Applied to 3-State Output Normal Pins Low-Voltage Pins	 -0.5 to V_{CC} + 0.5 -0.5 to +3.6	 V V
T_{VCC}	Supply Voltage Rise Time, 1V to 3V	500	ms
T_{STORE}	Storage Temperature (Ambient)	-65 to +150	°C
T_J	Junction Temperature Ceramic Plastic	 +150 +125	 °C °C
T_{SOL} (3)	Soldering Temperature	+260	°C

Table 16: Absolute Maximum Rating

Notes:

(1) Permanent damage to the device may occur if the Absolute Maximum ratings are exceeded.

These are stress ratings only. Functional operation of the device at these or any other conditions, other than those listed under the Recommended Operating Conditions, is not implied.

(2) Exposure to Absolute Maximum Ratings conditions for extended periods of time may degrade device reliability.

(3) T_{SOL} should occur for no more than 10 seconds. (EBGA package only.)

Recommended Operating Conditions

Symbol	Description	Min	Max	Unit
V_{CC}	Supply Voltage Relative to GND: Commercial: 0° C to 85° C Junction Industrial: –40° C to 100° C Junction	 3.14 3.0	 3.47 3.6	 V V
$V_{TT\ (GTL)}$	GTL Terminating Voltage Relative to GND: Commercial: 0° C to 85° C Junction Industrial: –40° C to 100° C Junction	 1.14 1.08	 1.26 1.32	 V V
$V_{TT\ (GTLP)}$	GTLP Terminating Voltage Relative to GND: Commercial: 0° C to 85° C Junction Industrial: –40° C to 100° C Junction	 1.43 1.35	 1.58 1.65	 V V
V_{REF} (2)	GTL/GTLP Reference Voltage Relative to GND (3) LV-PECL Reference Voltage	2/3 V_{TT} - 5% V_{CC} - 1.36	2/3 V_{TT} + 5% V_{CC} - 1.24	V V
T_{IN}	Input Signal Rise or Fall Time	-	250	ns

Table 17: Recommended Operating Conditions

Notes:

(1) All junction temperatures above those listed as Recommended Operating Conditions are unsafe, and may destroy the device.

(2) This voltage should be applied to the V_{REF} pin on DY6000-family devices.

Symbol	Parameter	Min	Max	Units	Test Conditions
V_{IMAX} (4)	Max. Voltage Applied to Input	-	5.5	V	
V_{CMAX} (5)	Max. Voltage Applied to Clock and Low-Voltage Inputs	-	3.6	V	
$V_{IH(TTL)}$	HIGH-Level Input Voltage	2.0	V_{CC} + 0.3	V	
$V_{IL(TTL)}$	LOW-Level Input Voltage	0.0	0.8	V	
$V_{IH(CMOS)}$	HIGH-Level Input Voltage	$0.7V_{CC}$	V_{CC}	V	
$V_{IL(CMOS)}$	LOW-Level Input Voltage	0.0	$0.3V_{CC}$	V	
$V_{IH(GTL\ or\ GTLP)}$	HIGH-Level Input Voltage	V_{REF} + 0.2	V_{TT}	V	
$V_{IL(GTL\ or\ GTLP)}$	LOW-Level Input Voltage	0.0	V_{REF} - 0.2	V	
$V_{IH(LVPECL)}$	HIGH-Level Input Voltage	2.135	2.420	V	V_{CC} = 3.3V
$V_{IL(LVPECL)}$	LOW-Level Input Voltage	1.490	1.825	V	V_{CC} = 3.3V
$V_{OH\ (TTL)}$	HIGH Level Output Voltage	2.4		V	V_{CC} Min. See Note 1 for I_{OH}
$V_{OL(TTL)}$	LOW Level Output Voltage (1)	-	0.4	V	V_{CC} Min. See Note 1 for I_{OL}
$V_{OH(GTL)}$	HIGH Level Output Voltage (2,3)	-	V_{TT}	V	
$V_{OL(GTL)}$	LOW Level Output Voltage (2)	-	0.4	V	I_{OL} = 20mA, V_{TT} Max
$V_{OH(GTLP)}$	HIGH Level Output Voltage (2,3)	-	V_{TT}	V	
$V_{OL(GTLP)}$	LOW Level Output Voltage (2)	-	0.55	V	I_{OL} = 40mA, V_{TT} Max
V_{DR} (8)	Data-Retention Voltage	2.5	-	V	
I_{DDQ}	Quiescent Current (9)	-	10	mA	V_{CC} = Max; All I/Os Open
I_{IL}	Leakage Current	-10	+10	µA	
I_{PU}	Pad Pullup Current (When Selected)	-	-150	µA	V_{IN} = 0V V_{CCO} = 3.3V
I_{PD}	Pad Pulldown Current (When Selected)	-	-200	µA	V_{IN} = 5.5V
C_{IN}	Input Capacitance	-	10.0	pF	EBGA Package

Table 18: DC Electrical Characteristics over Operating Conditions

Notes:

(1) Sink/Source current in TTL mode varies with slew-rate setting. For V_{CC} = Min, it is

Fast Slew Rate: 16mA
Medium Slew Rate: 11mA
Slow Slew Rate: 5mA

(2) Sink current in GTL mode = 20mA. Sink current in GTLP mode = 40mA. Source current is provided by an external pullup resistor.

(3) V_{REF} = 2/3 V_{TT} ±5%.

(4) All I/O pins except the 38 low-voltage input leads are 5-volt-tolerant.

(5) The maximum voltage applied to the 38 low-voltage input pins should not exceed this value, even if they are used as single-ended I/O.

(6) All GTL outputs should be terminated to V_{TT} through a 50Ω resistor.

(7) ALL GTLP outputs should be terminated to V_{TT} through a 25Ω termination, configured as a pair of 50Ω resistors, one at each end of the net.

(8) Below this voltage, configuration data may be lost.

(9) Refer to Table 7.

Clock and Set/Reset Buffer Switching Characteristics

Description	Symbol	Speed Grade			Units
		-E	-F	-G	
		Max	Max	Max	
Global Clock Delay with PLL		Programmable from -3.0ns to +2ns in 150ps increments			
Global Clock Delay without PLL(1, 2)	T_{GCKD}	7.7	7.0	6.3	ns
Global Clock Skew	T_{GCKS}	0.2	0.2	0.2	ns
Quadrant Clock Delay with PLL		Programmable from -3.0ns to +2ns in 150ps increments			
Quadrant Clock Delay(1, 2)	T_{QCKD}	6.1	5.5	5.0	ns
Quadrant Clock Skew	T_{QCKS}	0.2	0.2	0.2	ns
Clock Min Pulse Width HIGH	T_{MPH}	2.4	2.2	2.0	ns
Clock Min Pulse Width LOW	T_{MPL}	2.4	2.2	2.0	ns
Global Set/Reset Delay	T_{GSR}	18.7	17.0	15.3	ns

Table 19: Clock and Set/Reset Buffer AC Characteristics (Input Set to TTL)

Notes:

(1) Global and quadrant clock delays are measured from the input pin on the device to the flip-flop clock input.

(2) Default programming of the PLL offsets actual clock delays, forcing them to 0.0ns.

(3) All delays are specified over commercial voltage and temperature range. For industrial voltage and temperature range, add 5%.

(4) Clock delays are also referred to as latency.

Description	Symbol	Speed Grade			Units
		-E	-F	-G	
		Max	Max	Max	
Global Clock Delay with PLL		Programmable from -3.0ns to +2ns in 150ps increments			
Global Clock Delay without PLL(1, 2)	T_{GCKD}	8.8	8.0	7.2	ns
Global Clock Skew	T_{GCKS}	0.2	0.2	0.2	ns
Quadrant Clock Delay with PLL		Programmable from -3.0ns to +2ns in 150ps increments			
Quadrant Clock Delay(1, 2)	T_{QCKD}	7.2	6.5	5.9	ns
Quadrant Clock Skew	T_{QCKS}	0.2	0.2	0.2	ns
Clock Min Pulse Width HIGH	T_{MPH}	2.4	2.2	2.0	ns
Clock Min Pulse Width LOW	T_{MPL}	2.4	2.2	2.0	ns
Global Set/Reset Delay	T_{GSR}	19.6	17.9	16.2	ns

Table 20: Clock and Set/Reset Buffer AC Characteristics (Input Set to GTL, GTLP, PECL, or LVDS)

Notes:

(1) Global and quadrant clock delays are measured from the input pin on the device to the flip-flop clock input.

(2) Default programming of the PLL offsets actual clock delays, forcing them to 0.0ns.

(3) All delays are specified over commercial voltage and temperature range. For industrial voltage and temperature range, add 5%.

(4) Clock delays are also referred to as latency.

I/O Block Switching Characteristics

Description	Symbol	Speed Grade			Units
		-E	-F	-G	
		Max	Max	Max	
Input Buffer Combinatorial Delay	T_{INPD}	3.7	3.2	2.9	ns
Input Flip-flop Setup Time (Global Clock)	T_{INIS1}	1.9	1.6	1.4	ns
Input Flip-flop Hold Time (Global Clock)	T_{INIH1}	0.0	0.0	0.0	ns
Input Flip-flop Clock to Output (Global Clock)	T_{INCO1}	3.0	2.6	2.3	ns
Output Buffer Combinatorial Delay (No Load)(2,3)	T_{OUTIS1}	5.2	4.3	3.8	ns
Output Flip-flop Setup Time (Global Clock)	T_{OUTIS2}	3.5	2.3	2.0	ns
Output Flip-flop Hold Time (Global Clock)	T_{OUTIH1}	0.0	0.0	0.0	ns
Output Flip-flop Clock to Output (Global Clock, No Load) (2,3)	T_{OUTCO1}	3.6	2.9	2.6	ns
I/O Flip-flop Clock Enable Setup Time	T_{CES1}	2.4	2.0	1.6	ns
I/O Flip-flop Clock Enable Hold Time	T_{CEH1}	0.0	0.0	0.0	ns
Input Flip-flop GSR Set/Reset Delays	T_{GSRI}	3.0	2.6	2.3	ns
Output Flip-flop GSR Set/Reset Delays	T_{GSRO}	3.5	3.0	2.7	ns
Input Flip-flop GSR Set/Reset Setup Time	T_{GSRIS1}	0.5	0.4	0.3	ns
Output Flip-flop GSR Set/Reset Setup Time	T_{GSROS1}	0.5	0.4	0.3	ns

Table 21: Input and Output Buffer Parameters (I/O Set to TTL)

Notes:

(1) All delays are specified over commercial voltage and temperature range. For industrial voltage and temperature range, add 5%.

(2) Output delays are specified with no load. Add the following delays to adjust for loading.

Fast Slew Rate: 12ps/pF
Medium Slew Rate: 25ps/pF
Slow Slew Rate: 55ps/pF

(3) The maximum loading for outputs switching at the same time in the same direction is shown below. One power/ground pin pair is provided for each eight I/O blocks on the device.

Fast Slew Rate: 200pf between each power/ground pair
Medium Slew Rate: 300pf between each power/ground pair
Slow Slew Rate: 400pf between each power/ground pair

(4) Each output pin has individual slew-rate control.

Description	Symbol	Speed Grade			Units
		-E	-F	-G	
		Max	Max	Max	
OE to Pad Active (No Load)(2,3)	T_{3SOE}	4.5	3.7	3.3	ns
OE to Pad Hi-Z (No Load) (2,3)	T_{3SOD}	4.5	3.7	3.3	ns

Table 22: Three-state Buffer Delays (I/O Set to TTL)

Notes:

(1) All delays are specified over commercial voltage and temperature range. For industrial voltage and temperature range, add 5%.

(2) Output delays are specified with no load. Add the following delays to adjust for loading:

Fast Slew Rate: 12ps/pF
Medium Slew Rate: 25ps/pF
Slow Slew Rate: 55ps/pF

(3) Each output pin has individual slew-rate control.

(4) Should be measured with output held at V_{OL} + 0.5V.

Description	Symbol	Speed Grade			Units
		-E	-F	-G	
		Max	Max	Max	
Input Buffer Combinatorial Delay	T_{INPD}	4.7	4.0	3.6	ns
Input Flip-flop Setup Time (Global Clock)	T_{INIS1}	3.0	2.4	2.2	ns
Input Flip-flop Hold Time (Global Clock)	T_{INIH1}	0.0	0.0	0.0	ns
Input Flip-flop Clock to Output (Global Clock)	T_{INCO1}	4.0	2.6	2.3	ns
Output Buffer Combinatorial Delay (No Load)(2)	T_{OUTIS1}	4.5	3.6	3.2	ns
Output Flip-flop Setup Time (Global Clock)	T_{OUTIS2}	3.5	2.3	2.0	ns
Output Flip-flop Hold Time (Global Clock)	T_{OUTIH1}	0.0	0.0	0.0	ns
Output Flip-flop Clock to Output (Global Clock, No Load) (2)	T_{OUTCO1}	2.8	2.3	2.1	ns
I/O Flip-flop Clock Enable Setup Time	T_{CES1}	2.4	2.0	1.6	ns
I/O Flip-flop Clock Enable Hold Time	T_{CEH1}	0.0	0.0	0.0	ns
Input Flip-flop GSR Set/Reset Delays	T_{GSRI}	3.0	2.6	2.3	ns
Output Flip-flop GSR Set/Reset Delays	T_{GSRO}	2.9	2.4	2.2	ns
Input Flip-flop GSR Set/Reset Setup Time	T_{GSRIS1}	0.5	0.4	0.3	ns
Output Flip-flop GSR Set/Reset Setup Time	T_{GSROS1}	0.5	0.4	0.3	ns

Table 23: Input and Output Buffer Parameters (I/O Set to GTL or GTLP)

Notes:

(1) All delays are specified over commercial voltage and temperature range. For industrial voltage and temperature range, add 5%.

(2) Output delays are specified with no load. Add the following delays to adjust for loading:
GTL: 7ps/pF
GTLP: 4ps/pF

Description	Symbol	Speed Grade			Units
		-E	-F	-G	
		Max	Max	Max	
OE to Pad Active (No Load)(2)	T_{3SOE}	4.5	3.7	3.3	ns
OE to Pad Hi-Z (No Load) (2)	T_{3SOD}	4.5	3.7	3.3	ns

Table 24: Three-state Buffer Delays (I/O Set to GTL or GTLP)

Notes:

(1) All delays are specified over commercial voltage and temperature range. For industrial voltage and temperature range, add 5%.

(2) Output delays are specified with no load. Add the following delays to adjust for loading:
GTL: 7ps/pF
GTLP: 4ps/pF

(3) Should be measured with output held at V_{OL} + 0.5V.

Description	Symbol	Speed Grade			Units
		-E	-F	-G	
		Max	Max	Max	
Input Buffer Combinatorial Delay	T_{INPD}	4.7	4.0	3.6	ns
Input Flip-flop Setup Time (Global Clock)	T_{INIS1}	3.0	2.4	2.2	ns
Input Flip-flop Hold Time (Global Clock)	T_{INIH1}	0.0	0.0	0.0	ns
Input Flip-flop Clock to Output (Global Clock)	T_{INCO1}	4.0	2.6	2.3	ns
I/O Flip-flop Clock Enable Setup Time	T_{CES1}	2.4	2.0	1.6	ns
I/O Flip-flop Clock Enable Hold Time	T_{CEH1}	0.0	0.0	0.0	ns
Input Flip-flop GSR Set/Reset Delays	T_{GSRI}	3.0	2.6	2.3	ns
Input Flip-flop GSR Set/Reset Setup Time	T_{GSRIS1}	0.5	0.4	0.3	ns

Table 25: Input Buffer Parameters (I/O Set to LV-PECL or LVDS)

Note:

All delays are specified over commercial voltage and temperature range. For industrial voltage and temperature range, add 5%.

Logic Block Switching Characteristics

Description	Symbol	Speed Grade			Units
		-E	-F	-G	
		Max	Max	Max	
3-Input AND/OR to Flip-flop Delay	T_{ANDR3}	2.7	2.4	2.2	ns
6-Input AND/OR to Flip-flop Delay	T_{ANDR6}	3.3	3.0	2.7	ns
9-Input AND/OR to Flip-flop Delay	T_{ANDR9}	3.9	3.5	3.2	ns
7-Input XOR to Flip-flop Delay	T_{XORR7}	4.0	3.6	3.3	ns
8:1 Multiplexer Data to Flip-flop	T_{MUXR8}	3.0	2.8	2.5	ns
8:1 Multiplexer Select to Flip-flop	T_{MUXSR8}	3.1	2.9	2.6	ns
2-Bit-Adder/Multiplier to Flip-flop (Sum)	T_{ADDCR}	4.0	3.6	3.3	ns
3-Input AND/OR Combinatorial Delay	T_{ANDC3}	3.0	2.8	2.5	ns
6-Input AND/OR Combinatorial Delay	T_{ANDC6}	3.9	3.5	3.2	ns
9-Input AND/OR Combinatorial Delay	T_{ANDC9}	4.5	4.1	3.7	ns
7-Input XOR Combinatorial Delay	T_{XORC7}	4.6	4.2	3.8	ns
2-Bit-Adder/Multiplier Delay (Sum)	T_{ADDC}	4.4	4.0	3.6	ns
8:1 Multiplexer Data Combinatorial Delay	T_{MUXC8}	3.4	3.1	2.8	ns
8:1 Multiplexer Select Combinatorial Delay	T_{MUXS8}	3.5	3.2	2.9	ns
Carry Chain Initial Delay	T_{CRYI}	3.1	2.9	2.6	ns
Carry Chain Delay Per 2 Bits	T_{CRY}	0.4	0.4	0.35	ns
Carry Chain Final Delay	T_{CRYF}	2.5	2.3	2.1	ns
D-Flip-flop Setup Time	T_{SU}	0.5	0.4	0.4	ns
D-Flip-flop Hold Time	T_{HD}	0.0	0.0	0.0	ns
T-Flip-flop Setup Time	T_{SUT}	0.7	0.7	0.6	ns
T-Flip-flop Hold Time	T_{THD}	0.0	0.0	0.0	ns
Flip-flop Clock to Out (GCLK or QCLK)	T_{COG}	1.5	1.3	1.2	ns
Flip-flop Clock to Out (LCLK)	T_{COL}	2.7	2.4	2.2	ns
GSR Set/Reset Delay	T_{GSR}	2.9	2.6	2.4	ns
LSR Set/Reset Delay	T_{LSR}	4.2	3.9	3.5	ns
Logic Block Pass-Through	T_{LBPT}	2.4	2.2	2.0	ns

Table 26: Logic Block Switching Parameters

(Includes All Routing Delays Within Routing Region(5))

Notes:

(1) All delays are specified over commercial voltage and temperature range. For industrial voltage and temperature range, add 5%.

(2) Refer to Figure 11 for a schematic of the logic paths described in Table 26.

(3) The AND/OR combinatorial delay, XOR combinatorial delay, comparator combinatorial delay, adder/multiplier delay, multiplexer combinatorial delay, and carry chain final delay include the complete path through the logic block from inputs through outputs, connection buffers, and routing to the next logic block or Active Repeater.

(4) The AND/OR-to-flip-flop delay, XOR-to-flip-flop delay, and multiplexer-to-flip-flop delay include all elements from inputs to the D/T input of either flip-flop.

(5) Logic block delays shown in Table 26 include all connection buffer and routing delays within a nine-block routing region. Additional delays are incurred only when a net must go through an Active Repeater to reach a block in another routing region.

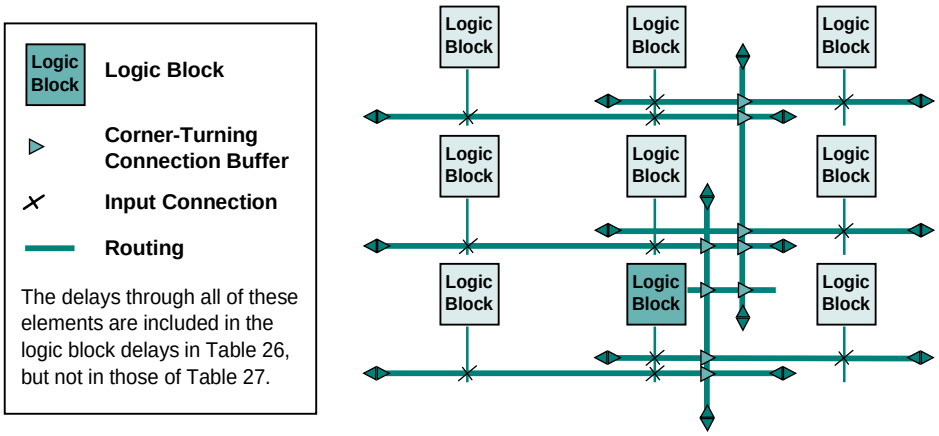


Figure 27: Logic Block Delays Includes Routing Within a Region

Description	Symbol	Speed Grade			Units
		-E	-F	-G	
		Max	Max	Max	
3-Input AND/OR Combinatorial Delay	T_{ANDR3}	0.82	0.75	0.68	ns
6-Input AND/OR Combinatorial Delay	T_{ANDR6}	1.43	1.30	1.18	ns
9-Input AND/OR Combinatorial Delay	T_{ANDR9}	1.41	1.29	1.17	ns
7-Input XOR Combinatorial Delay	T_{XORR7}	3.19	2.90	2.64	ns
8:1 Multiplexer Data Combinatorial Delay	T_{MUXR8}	1.17	1.07	0.97	ns
8:1 Multiplexer Select Combinatorial Delay	T_{MUXSR8}	1.28	1.17	1.06	ns
Flip-flop Clock-to-Out (GCLK or QCLK)	T_{COG}	0.67	0.61	0.55	ns

Table 27: Logic Block Switching Parameters

(Excludes All Routing Delays Within Routing Region(5))

Notes:

(1) All delays are specified over commercial voltage and temperature range. For industrial voltage and temperature range, add 5%.

(2) Refer to Figure 11 for a schematic of the logic paths described in the above table.

Description	Symbol	Speed Grade			Units
		-E	-F	-G	
Read/Write Operation		Max	Max	Max	
Address Setup Time Before Clock	T_{AS}	4.0	3.5	3.0	ns
Address Hold Time After Clock	T_{AH}	0.0	0.0	0.0	ns
WE Setup Time Before Clock	T_{WS}	4.0	3.5	3.0	ns
WE Hold Time After Clock	T_{WH}	0.0	0.0	0.0	ns
D_{IN} Setup Time Before Clock	T_{DS}	4.0	3.5	3.0	ns
D_{IN} Hold Time After Clock	T_{DH}	0.0	0.0	0.0	ns
Clock Min Pulse Width HIGH (2)	T_{MPH}	5.0	5.0	5.0	ns
Read Cycle		Min	Min	Min	
Output Data Valid After Clock	T_{ROS}	10.0	9.0	8.0	ns
RAM Enable/Disable		Min	Min	Min	
SRAM Enable/Disable Buffer Delay	T_{GPD}	6.0	5.5	5.0	ns
SRAM Enable Setup with Read/Write Clock	T_{GSS}	4.0	3.5	3.0	ns
SRAM Enable/Disable Hold Time with Read/Write Clock	T_{GSH}	0.0	0.0	0.0	ns
Two Clock Operation		Min	Min	Min	
Read After Write to Same Location	T_{RAW}	7.0	6.5	6.0	ns
Read Before Write to Same Location	T_{RBW}	7.0	6.5	6.0	ns

Table 28: RAM Switching Parameters – Two-Port Mode

Note:

All delays are specified over commercial voltage and temperature range. For industrial voltage and temperature range, add 5%.

Description	Symbol	Speed Grade			Units
		-E	-F	-G	
Read/Write Operation		Max	Max	Max	
Address Setup Time Before Clock	T_{AS}	4.0	3.5	3.0	ns
Address Hold Time After Clock	T_{AH}	0.0	0.0	0.0	ns
WE Setup Time Before Clock	T_{WS}	4.0	3.5	3.0	ns
WE Hold Time After Clock	T_{WH}	0.0	0.0	0.0	ns
DIN Setup Time Before Clock	T_{DS}	4.0	3.5	3.0	ns
DIN Hold Time After Clock	T_{DH}	0.0	0.0	0.0	ns
Read Cycle		Min	Min	Min	
Output Data Valid After Clock	T_{ROS}	0.0	0.0	0.0	ns

Table 29: RAM Switching Parameters – Single-Port Mode

Note:

All delays are specified over commercial voltage and temperature range. For industrial voltage and temperature range, add 5%.

Description	Symbol	Speed Grade			Units
		-E	-F	-G	
		Max	Max	Max	
Horizontal Active Repeater Delay	T_{HRPT}	0.9	0.8	0.7	ns
Vertical Active Repeater Delay	T_{VRPT}	0.6	0.6	0.5	ns
Vertical to Horizontal Active Repeater Delay	T_{VHRPT}	0.9	0.8	0.7	ns
Horizontal to Vertical Active Repeater Delay	T_{HVRPT}	0.9	0.8	0.7	ns

Table 30: Active Repeater Switching Parameters

Note:

All delays are specified over commercial voltage and temperature range. For industrial voltage and temperature range, add 5%.

Pin Description

432-Pin EBGA

Pin Description		DY6009 Ball	DY6020 Ball	DY6035 Ball	DY6055 Ball
GTL_REF_EXTERNAL		AE4	AE4	AE4	AE4
LVPECL_REF_EXTERNAL		AG4	AG4	AG4	AG4
PCKI_PCKO		AJ25	AJ25	AJ25	AJ25
PLL1REST		D26	D26	D26	D26
PLL2REST		D6	D6	D6	D6
RESETN		AG28	AG28	AG28	AG28
STRPRG		AH27	AH27	AH27	AH27
SYSDONE		AH7	AH7	AH7	AH7
IO_1		NC	F29	F29	F29
IO_2/PECL1N	L-V	F28	F28	F28	F28
IO_3/PECL1_GPD	L-V	G28	G28	G28	G28
IO_4		NC	NC	G29	G29
IO_5		NC	NC	NC	G30
IO_6		NC	G31	G31	G31
IO_7		H28	H28	H28	H28
IO_8		NC	NC	H29	H29
IO_9		NC	NC	NC	H30
IO_10		NC	H31	H31	H31
IO_11		J28	J28	J28	J28
IO_12		NC	NC	J31	J31
IO_13		NC	NC	NC	J30
IO_14/QCLK1TLN	L-V	J29	J29	J29	J29
IO_15/QCLK1TL	L-V	K29	K29	K29	K29
IO_16		NC	NC	K28	K28
IO_17		NC	NC	NC	K30
IO18/QCLK2TLN	L-V	L29	L29	L29	L29
IO_19/QCLK2TL	L-V	L28	L28	L28	L28
IO_20		NC	NC	L30	L30
IO_21		NC	K31	K31	K31
IO_22		NC	L31	L31	L31
IO_23		NC	NC	M31	M31
IO_24		M28	M28	M28	M28
IO_25		NC	NC	NC	M29
IO_26		NC	M30	M30	M30
IO_27		NC	N31	N31	N31
IO_28		NC	NC	N30	N30
IO_29		NC	NC	NC	N28
IO_30/ GCLK1N	L-V	N29	N29	N29	N29
IO_31/GCLK1	L-V	P29	P29	P29	P29
IO_32		P30	P30	P30	P30
IO_33		NC	NC	NC	P28
IO_34/PECL2N	L-V	P31	P31	P31	P31
IO_35/PECL2	L-V	R31	R31	R31	R31
Pin Description		DY6009 Ball	DY6020 Ball	DY6035 Ball	DY6055 Ball

Table 31: 432-Pin EBGA Package Information

Pin Description		DY6009 Ball	DY6020 Ball	DY6035 Ball	DY6055 Ball
IO_36		NC	NC	R29	R29
IO_37		NC	NC	NC	R30
IO_38/PECL3N	L-V	R28	R28	R28	R28
IO_39/PECL3	L-V	T28	T28	T28	T28
IO_40		NC	T31	T31	T31
IO_41		NC	T30	T30	T30
IO_42/PECL4N	L-V	NC	T29	T29	T29
IO_43/PECL4	L-V	NC	U29	U29	U29
IO_44		NC	NC	U28	U28
IO_45		NC	NC	NC	U30
IO_46/PECL5N	L-V	NC	V29	V29	V29
IO_47/PECL5	L-V	V28	V28	V28	V28
IO_48		NC	NC	U31	U31
IO_49		NC	NC	NC	V30
IO_50		NC	V31	V31	V31
IO_51		NC	W29	W29	W29
IO_52		NC	NC	W28	W28
IO_53/WE		W30	W30	W30	W30
IO_54		NC	NC	NC	W31
IO_55/RDY		Y30	Y30	Y30	Y30
IO_56		NC	NC	Y29	Y29
IO_57/D7		Y28	Y28	Y28	Y28
IO_58		NC	NC	NC	Y31
IO_59/D6		AA31	AA31	AA31	AA31
IO_60		NC	AB31	AB31	AB31
IO_61		NC	NC	NC	AA30
IO_62/QCLK1BLN	L-V	AA28	AA28	AA28	AA28
IO_63/QCLK1BL	L-V	AA29	AA29	AA29	AA29
IO_64		NC	NC	AC31	AC31
IO_65/D5		AB30	AB30	AB30	AB30
IO_66/QCLK2BLN	L-V	AB28	AB28	AB28	AB28
IO_67/QCLK2BL	L-V	AB29	AB29	AB29	AB29
IO_68		NC	NC	NC	AC30
IO_69/D4		AC29	AC29	AC29	AC29
IO_70		NC	NC	AC28	AC28
IO_71/D3		AD31	AD31	AD31	AD31
IO_72		NC	NC	NC	AD30
IO_73/D2		AD29	AD29	AD29	AD29
IO_74		NC	NC	AE30	AE30
IO_75/D1		AD28	AD28	AD28	AD28
IO_76		NC	NC	NC	AE29
IO_77/D0		AE28	AE28	AE28	AE28
IO_78/TDO		AE31	AE31	AE31	AE31
IO_79		NC	AF29	AF29	AF29
IO_80		NC	NC	AF28	AF28
IO_81		NC	AH26	AH26	AH26
IO_82		NC	NC	AJ26	AJ26
IO_83/M0		AK26	AK26	AK26	AK26
IO_84		AH25	AH25	AH25	AH25
IO_85		NC	NC	NC	AK25
Pin Description		**DY6009 Ball**	**DY6020 Ball**	**DY6035 Ball**	**DY6055 Ball**

Table 31: 432-Pin EBGA Package Information

Pin Description	DY6009 Ball	DY6020 Ball	DY6035 Ball	DY6055 Ball
IO_86/M1	AL25	AL25	AL25	AL25
IO_87	NC	NC	NC	AH24
IO_88/M2	AJ24	AJ24	AJ24	AJ24
IO_89	NC	AK24	AK24	AK24
IO_90/DONE	AL24	AL24	AL24	AL24
IO_91	NC	NC	NC	AH23
IO_92/DOUT	AJ23	AJ23	AJ23	AJ23
IO_93	NC	NC	AK23	AK23
IO_94	NC	AL23	AL23	AL23
IO_95	AH22	AH22	AH22	AH22
IO_96	NC	NC	AJ22	AJ22
IO_97	NC	NC	NC	AK22
IO_98	AL22	AL22	AL22	AL22
IO_99	AH21	AH21	AH21	AH21
IO_100	NC	AJ21	AJ21	AJ21
IO_101	NC	NC	NC	AK21
IO_102	NC	AL21	AL21	AL21
IO_103	AH20	AH20	AH20	AH20
IO_104	NC	NC	AJ20	AJ20
IO_105	NC	NC	NC	AK20
IO_106	AL20	AL20	AL20	AL20
IO_107	AH19	AH19	AH19	AH19
IO_108	NC	NC	AJ19	AJ19
IO_109	NC	NC	NC	AK19
IO_110	NC	AL19	AL19	AL19
IO_111	AH18	AH18	AH18	AH18
IO_112	NC	NC	AJ18	AJ18
IO_113	NC	NC	NC	AK18
IO_114	AL18	AL18	AL18	AL18
IO_115	AH17	AH17	AH17	AH17
IO_116	NC	NC	AJ17	AJ17
IO_117	NC	NC	AK17	AK17
IO_118	NC	AL17	AL17	AL17
IO_119	AK16	AK16	AK16	AK16
IO_120	NC	AH16	AH16	AH16
IO_121	NC	AJ16	AJ16	AJ16
IO_122	AL16	AL16	AL16	AL16
IO_123	AL15	AL15	AL15	AL15
IO_124	NC	NC	NC	AK15
IO_125	NC	NC	AH15	AH15
IO_126	NC	AJ15	AJ15	AJ15
IO_127	AL14	AL14	AL14	AL14
IO_128	NC	NC	AK14	AK14
IO_129	NC	NC	AH14	AH14
IO_130	AJ14	AJ14	AJ14	AJ14
IO_131	AL13	AL13	AL13	AL13
IO_132	NC	NC	NC	AK13
IO_133	NC	NC	AH13	AH13
IO_134	NC	AJ13	AJ13	AJ13
IO_135	AL12	AL12	AL12	AL12
Pin Description	DY6009 Ball	DY6020 Ball	DY6035 Ball	DY6055 Ball

Table 31: 432-Pin EBGA Package Information

Pin Description		DY6009 Ball	DY6020 Ball	DY6035 Ball	DY6055 Ball
IO_136		NC	NC	NC	AK12
IO_137		NC	NC	AH12	AH12
IO_138		AJ12	AJ12	AJ12	AJ12
IO_139		AL11	AL11	AL11	AL11
IO_140		NC	NC	NC	AK11
IO_141		NC	AH11	AH11	AH11
IO_142		NC	AJ11	AJ11	AJ11
IO_143		AL10	AL10	AL10	AL10
IO_144		NC	NC	NC	AK10
IO_145		NC	AH10	AH10	AH10
IO_146		AJ10	AJ10	AJ10	AJ10
IO_147		AL9	AL9	AL9	AL9
IO_148		NC	NC	AK9	AK9
IO_149		NC	NC	NC	AH9
IO_150		NC	AJ9	AJ9	AJ9
IO_151		AL8	AL8	AL8	AL8
IO_152		NC	NC	AK8	AK8
IO_153		NC	NC	NC	AH8
IO_154		AJ8	AJ8	AJ8	AJ8
IO_155		AL7	AL7	AL7	AL7
IO_156		NC	NC	AK7	AK7
IO_157		NC	NC	NC	AJ7
IO_158		NC	AJ6	AJ6	AJ6
IO_159/TMS		AH6	AH6	AH6	AH6
IO_160/TCK		AH5	AH5	AH5	AH5
IO_161/TDI		AG3	AG3	AG3	AG3
IO_162		NC	AF4	AF4	AF4
IO_163		AF3	AF3	AF3	AF3
IO_164		NC	NC	AF2	AF2
IO_165		NC	NC	NC	AE3
IO_166		NC	AE2	AE2	AE2
IO_167		AD4	AD4	AD4	AD4
IO_168		NC	NC	AE1	AE1
IO_169		NC	NC	NC	AD3
IO_170		AD2	AD2	AD2	AD2
IO_171		AC4	AC4	AC4	AC4
IO_172		NC	NC	AD1	AD1
IO_173		NC	NC	AC3	AC3
IO_174		NC	AC2	AC2	AC2
IO_175		NC	NC	NC	AC1
IO_176/QCLK2BR	L-V	AB4	AB4	AB4	AB4
IO_177/QCLK2BRN	L-V	AB3	AB3	AB3	AB3
IO_178		NC	NC	AB2	AB2
IO_179		NC	AB1	AB1	AB1
IO_180/QCLK1BR	L-V	AA4	AA4	AA4	AA4
IO_181/QCLK1BRN	L-V	AA3	AA3	AA3	AA3
IO_182		NC	NC	NC	AA2
IO_183		AA1	AA1	AA1	AA1
IO_184		NC	NC	Y4	Y4
IO_185		NC	NC	NC	Y3
Pin Description		**DY6009 Ball**	**DY6020 Ball**	**DY6035 Ball**	**DY6055 Ball**

Table 31: 432-Pin EBGA Package Information

Pin Description		DY6009 Ball	DY6020 Ball	DY6035 Ball	DY6055 Ball
IO_186		Y2	Y2	Y2	Y2
IO_187		Y1	Y1	Y1	Y1
IO_188		NC	NC	W4	W4
IO_189		NC	NC	NC	W3
IO_190		NC	W2	W2	W2
IO_191		NC	NC	NC	W1
IO_192/GSR		V2	V2	V2	V2
IO_193		NC	NC	V4	V4
IO_194		NC	V3	V3	V3
IO_195		NC	V1	V1	V1
IO_196/PECL6	L-V	U1	U1	U1	U1
IO_197/PECL6N	L-V	U2	U2	U2	U2
IO_198		NC	NC	NC	U4
IO_199		NC	U3	U3	U3
IO_200/PECL7	L-V	T1	T1	T1	T1
IO_201/PECL7N	L-V	T2	T2	T2	T2
IO_202		NC	T4	T4	T4
IO_203		NC	NC	T3	T3
IO_204/PECL8	L-V	R3	R3	R3	R3
IO_205/PECL8N	L-V	R4	R4	R4	R4
IO_206		NC	NC	R2	R2
IO_207		NC	NC	NC	R1
IO_208/PECL9	L-V	P3	P3	P3	P3
IO_209/PECL9N	L-V	P4	P4	P4	P4
IO_210		NC	P2	P2	P2
IO_211		NC	NC	NC	P1
IO_212/GCLK2	L-V	N3	N3	N3	N3
IO_213/GCLK2N	L-V	N4	N4	N4	N4
IO_214		NC	NC	NC	N2
IO_215		NC	N1	N1	N1
IO_216		NC	NC	NC	M2
IO_217		NC	NC	M3	M3
IO_218		M4	M4	M4	M4
IO_219		M1	M1	M1	M1
IO_220		NC	NC	L1	L1
IO_221		NC	NC	L2	L2
IO_222		NC	L4	L4	L4
IO_223		NC	NC	NC	L3
IO_224/QCLK2TR	L-V	K3	K3	K3	K3
IO_225/QCLK2TRN	L-V	K4	K4	K4	K4
IO_226		NC	NC	NC	K2
IO_227		NC	K1	K1	K1
IO_228/QCLK1TR	L-V	J3	J3	J3	J3
IO_229/QCLK1TRN	L-V	J4	J4	J4	J4
IO_230		NC	NC	J2	J2
IO_231		J1	J1	J1	J1
IO_232		NC	NC	H1	H1
IO_233		NC	NC	NC	H4
IO_234		NC	H3	H3	H3
IO_235		H2	H2	H2	H2
Pin Description		**DY6009 Ball**	**DY6020 Ball**	**DY6035 Ball**	**DY6055 Ball**

Table 31: 432-Pin EBGA Package Information

Pin Description	DY6009 Ball	DY6020 Ball	DY6035 Ball	DY6055 Ball
IO_236	NC	NC	G1	G1
IO_237	NC	NC	NC	G4
IO_238	NC	G3	G3	G3
IO_239	G2	G2	G2	G2
IO_240	NC	F4	F4	F4
IO_241	C5	C5	C5	C5
IO_242	C6	C6	C6	C6
IO_243	NC	NC	B5	B5
IO_244	NC	D7	D7	D7
IO_245	NC	NC	NC	C7
IO_246	B6	B6	B6	B6
IO_247	NC	A6	A6	A6
IO_248	NC	D8	D8	D8
IO_249	NC	NC	NC	C8
IO_250	B7	B7	B7	B7
IO_251	B8	B8	B8	B8
IO_252	NC	NC	NC	A7
IO_253	NC	NC	D9	D9
IO_254	C9	C9	C9	C9
IO_255	NC	B9	B9	B9
IO_256	NC	NC	NC	A8
IO_257	NC	NC	A9	A9
IO_258	D10	D10	D10	D10
IO_259	C10	C10	C10	C10
IO_260	NC	NC	NC	B10
IO_261	NC	NC	A10	A10
IO_262	B11	B11	B11	B11
IO_263	NC	NC	D11	D11
IO_264	NC	NC	C11	C11
IO_265	NC	NC	NC	A11
IO_266	B12	B12	B12	B12
IO_267	C12	C12	C12	C12
IO_268	NC	NC	D12	D12
IO_269	NC	NC	NC	A12
IO_270	A13	A13	A13	A13
IO_271	NC	NC	B13	B13
IO_272	NC	NC	NC	A14
IO_273	NC	D13	D13	D13
IO_274	C13	C13	C13	C13
IO_275	D14	D14	D14	D14
IO_276	NC	C14	C14	C14
IO_277	NC	B14	B14	B14
IO_278	C15	C15	C15	C15
IO_279	NC	B15	B15	B15
IO_280	C16	C16	C16	C16
IO_281	B16	B16	B16	B16
IO_282	B17	B17	B17	B17
IO_283	C17	C17	C17	C17
IO_284	NC	B18	B18	B18
IO_285	NC	C18	C18	C18
Pin Description	**DY6009 Ball**	**DY6020 Ball**	**DY6035 Ball**	**DY6055 Ball**

Table 31: 432-Pin EBGA Package Information

Pin Description	DY6009 Ball	DY6020 Ball	DY6035 Ball	DY6055 Ball
IO_286	D18	D18	D18	D18
IO_287	NC	C19	C19	C19
IO_288	NC	D19	D19	D19
IO_289	NC	NC	NC	A18
IO_290	B19	B19	B19	B19
IO_291	A19	A19	A19	A19
IO_292	NC	NC	A20	A20
IO_293	NC	NC	NC	D20
IO_294	C20	C20	C20	C20
IO_295	NC	NC	B20	B20
IO_296	NC	A21	A21	A21
IO_297	NC	NC	C21	C21
IO_298	D21	D21	D21	D21
IO_299	B21	B21	B21	B21
IO_300	NC	NC	A22	A22
IO_301	NC	NC	NC	B22
IO_302	C22	C22	C22	C22
IO_303	NC	NC	D22	D22
IO_304	NC	A23	A23	A23
IO_305	NC	NC	NC	A24
IO_306	B23	B23	B23	B23
IO_307	C23	C23	C23	C23
IO_308	NC	NC	D23	D23
IO_309	NC	NC	NC	A25
IO_310	B24	B24	B24	B24
IO_311	NC	NC	NC	B25
IO_312	NC	C24	C24	C24
IO_313	NC	NC	D24	D24
IO_314	A26	A26	A26	A26
IO_315	B26	B26	B26	B26
IO_316	NC	NC	C25	C25
IO_317	NC	NC	NC	D25
IO_318	B27	B27	B27	B27
IO_319	NC	NC	C26	C26
IO_320	NC	C27	C27	C27
Pin Description	**DY6009 Ball**	**DY6020 Ball**	**DY6035 Ball**	**DY6055 Ball**

Table 31: 432-Pin EBGA Package Information

432-Pin EBGA - Internal V_{CC} and Ground Connections

V_{CC}_Int Balls	GND_Int Balls	V_{CC}_I/O Balls	GND_I/O Balls	V_{CC}_PLL
C3	B3	A1	A2	E4
D2	C2	A3	A4	E28
D4	C4	A5	B1	GND_PLL
E3	D3	B2	D1	D5
F2	E2	C1	F1	D27
AH2	F3	E1	AG1	
AH4	AG2	AF1	AJ1	
AJ3	AH3	AH1	AK2	
AJ5	AJ2	AK1	AK6	
AK4	AJ4	AL2	AL1	
AK28	AK3	AL4	AL3	
AJ27	AK5	AL6	AL5	
AJ29	AK27	AL27	AL26	
AH28	AK29	AL29	AL28	
AH30	AJ28	AL31	AL30	
AG29	AJ30	AK30	AK31	
AF30	AH29	AJ31	AH31	
F30	AG30	AG31	AF31	
E29	E30	E31	F31	
D28	D29	C31	D31	
D30	C28	B30	B31	
C29	C30	A31	A30	
B28	B29	A29	A28	
D16	D17	A27	A17	
B4	D15	A16	A15	
V_{CC}_Int Balls	GND_Int Balls	V_{CC}_I/O Balls	GND_I/O Balls	

Table 32: 432-Pin EBGA - Internal V_{CC} and Ground Connections

Notes:
(1) NC means No Connect.
(2) Both PLL1rest and PLL2rest should be tied to ground.
(3) GTL_REF_EXTERNAL should be tied to ground when not used.
(4) LVPECL_REF_EXTERNAL should be tied to VCC when not used.
(5) LV designates low voltage pins, which are not 5V tolerant.

240-Pin EQFP

Pin Description		DY6009 Pin ID	DY6020, DY6035, DY6055 Pin ID
GTL_REF_EXTERNAL		55	55
LVPECL_REF_EXTERNAL		58	58
PCKI_PCKO		114	114
PLL1REST		183	183
PLL2REST		239	239
RESETN		123	123
STRPRG		118	118
SYSDONE		65	65
IO_2/PECL1N	L-V	177	177
IO_3/PECL1_GPD	L-V	176	176
IO_6		NC	175
IO_7		174	174
IO_10		NC	173
IO_11		172	172
IO_14/QCLK1TLN	L-V	170	170
IO_15/QCLK1TL	L-V	169	169
IO_18/QCLK2TLN	L-V	167	167
IO_19QCLK2TL	L-V	166	166
IO_22		NC	165
IO_24		164	164
IO_26		NC	163
IO_27		NC	161
IO_30/GCLK1N	L-V	160	160
IO_31/GCLK1	L-V	159	159
IO_32		158	158
IO_34/PECL2N	L-V	157	157
IO_35/PECL2	L-V	156	156
IO_38/PECL3N	L-V	155	155
IO_39/PECL3	L-V	154	154
IO_42/PECL4N	L-V	NC	151
IO_43/PECL4	L-V	NC	149
IO_46/PECL5N	L-V	NC	148
IO_47/PECL5	L-V	146	146
IO_50		NC	145
IO_51		NC	144
IO_53/WE		143	143
IO_55/RDY		141	141
IO_57/D7		140	140
IO_59/D6		138	138
IO_62/QCLK1BLN	L-V	137	137
IO_63/QCLK1BL	L-V	135	135
IO_65/D5		134	134
IO_66/QCLK2BLN	L-V	133	133
IO_67/QCLK2BL	L-V	131	131
IO_69/D4		130	130
IO_71/D3		129	129
IO_73/D2		128	128
IO_75/D1		127	127
IO_77/D0		126	126
Pin Description		DY6009 Pin ID	DY6020, DY6035, DY6055 Pin ID

Table 33: 240-Pin EQFP Package Information

Pin Description	DY6009 Pin ID	DY6020, DY6035, DY6055 Pin ID
IO_78/TDO	125	125
IO_79	NC	124
IO_81	NC	117
IO_83/M0	116	116
IO_84	115	115
IO_86/M1	113	113
IO_88/M2	112	112
IO_89	NC	110
IO_90/DONE	109	109
IO_92/DOUT	107	107
IO_94	NC	106
IO_95	105	105
IO_98	104	104
IO_99	102	102
IO_102	NC	101
IO_103	99	99
IO_106	98	98
IO_107	97	97
IO_110	NC	96
IO_111	95	95
IO_114	94	94
IO_115	93	93
IO_118	NC	91
IO_119	90	90
IO_122	88	88
IO_123	86	86
IO_126	NC	84
IO_127	83	83
IO_130	82	82
IO_131	81	81
IO_134	NC	80
IO_135	79	79
IO_138	78	78
IO_139	76	76
IO_142	NC	75
IO_143	73	73
IO_146	72	72
IO_147	71	71
IO_150	NC	70
IO_151	69	69
IO_154	68	68
IO_155	66	66
IO_159/TMS	64	64
IO_160/TCK	63	63
IO_161/TDI	57	57
IO_163	56	56
IO_166	NC	54
IO_167	53	53
IO_170	52	52
IO_171	51	51
IO_174	NC	50
IO_176/QCLK2BR L-V	49	49
Pin Description	**DY6009 Pin ID**	**DY6020, DY6035, DY6055 Pin ID**

Table 33: 240-Pin EQFP Package Information

Pin Description		DY6009 Pin ID	DY6020, DY6035, DY6055 Pin ID
IO_177/QCLK2BRN	L-V	47	47
IO_180/QCLK1BR	L-V	46	46
IO_181/QCLK1BRN	L-V	44	44
IO_183		43	43
IO_186		42	42
IO_187		41	41
IO_190		NC	40
IO_192/GSR		39	39
IO_194		NC	38
IO_195		NC	36
IO_196/PECL6	L-V	35	35
IO_197/PECL6N	L-V	33	33
IO_200/PECL7	L-V	32	32
IO_201/PECL7N	L-V	29	29
IO_204/PECL8	L-V	27	27
IO_205/PECL8N	L-V	26	26
IO_208/PECL9	L-V	25	25
IO_209/PECL9N	L-V	24	24
IO_212/GCLK2	L-V	23	23
IO_213/GCLK2N	L-V	21	21
IO_215		NC	20
IO_218		18	18
IO_219		17	17
IO_222		NC	16
IO_224/QCLK2TR	L-V	15	15
IO_225/QCLK2TRN	L-V	13	13
IO_228/QCLK1TR	L-V	12	12
IO_229/QCLK1TRN	L-V	10	10
IO_231		9	9
IO_234		NC	8
IO_235		7	7
IO_238		NC	6
IO_239		5	5
IO_240		NC	4
IO_241		238	238
IO_242		237	237
IO_246		235	235
IO_250		233	233
IO_251		232	232
IO_254		230	230
IO_255		NC	228
IO_258		227	227
IO_259		226	226
IO_262		225	225
IO_266		223	223
IO_267		221	221
IO_270		220	220
IO_273		NC	219
IO_274		218	218
IO_275		217	217
IO_276		NC	216
IO_277		NC	214
Pin Description		**DY6009 Pin ID**	**DY6020, DY6035, DY6055 Pin ID**

Table 33: 240-Pin EQFP Package Information

Pin Description	DY6009 Pin ID	DY6020, DY6035, DY6055 Pin ID
IO_278	213	213
IO_279	NC	212
IO_280	211	211
IO_281	208	208
IO_282	207	207
IO_283	206	206
IO_284	NC	205
IO_285	NC	203
IO_286	202	202
IO_287	NC	200
IO_288	NC	199
IO_290	198	198
IO_291	197	197
IO_294	196	196
IO_298	194	194
IO_299	193	193
IO_302	192	192
IO_306	190	190
IO_307	189	189
IO_310	188	188
IO_314	187	187
IO_315	186	186
IO_318	185	185
Pin Description	**DY6009 Lead ID**	**DY6020, DY6035, DY6055 Lead ID**

Table 33: 240-Pin EQFP Package Information

240-Pin EQFP - Internal V_{CC} and Ground Connections

V_{CC} Pins	Ground Pins	V_{CC} PLL	Ground PLL
3	2	1	181
11	14	180	240
22	19		
30	28		
34	31		
45	37		
59	48		
61	60		
74	62		
85	67		
89	77		
100	87		
111	92		
119	103		
121	108		
136	120		
142	122		
147	132		
153	139		
168	150		
178	152		
184	162		
191	171		
201	179		
210	182		
224	195		
229	204		
234	209		
	215		
	222		
	231		
	236		

Table 34: 240-Pin EQFP - Internal V_{CC} and Ground Connections

Notes:
(1) NC means No Connect.
(2) Both PLL1rest and PLL2rest should be tied to ground.
(3) GTL_REF_EXTERNAL should be tied to ground when not used.
(4) LVPECL_REF_EXTERNAL should be tied to VCC when not used.
(5) LV designates low voltage pins, which are not 5V tolerant.

Package Drawings

432-Pin EBGA

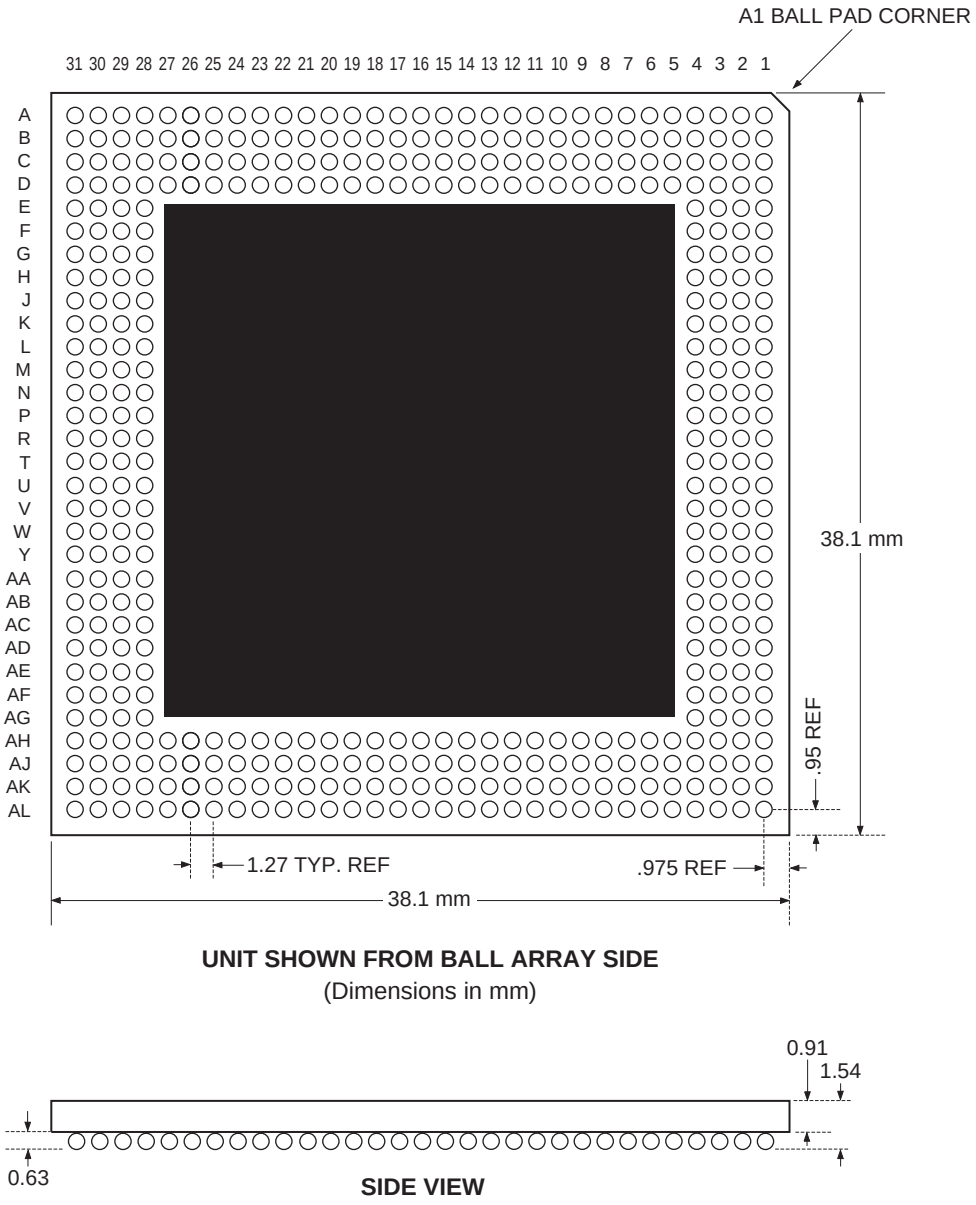


Figure 28: Package Drawing of 432-pin EBGA

240-Pin Thermal Enhanced EQFP

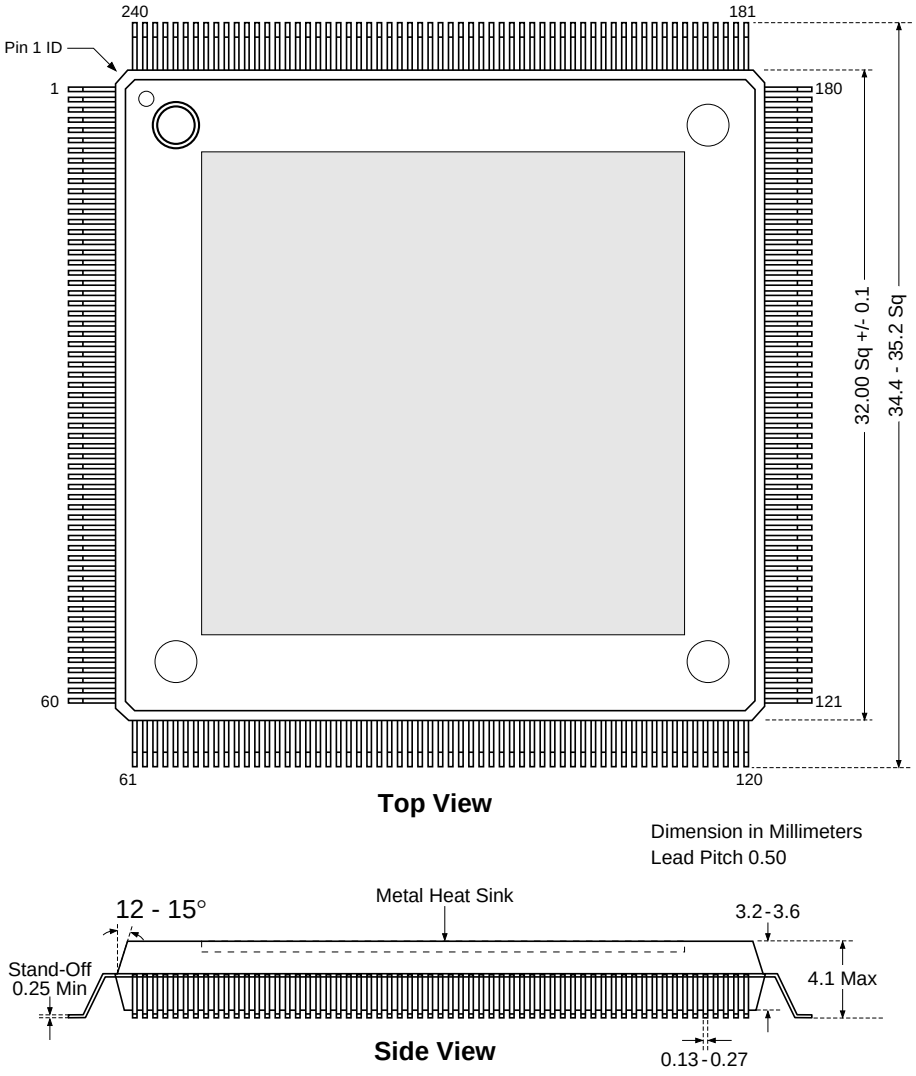
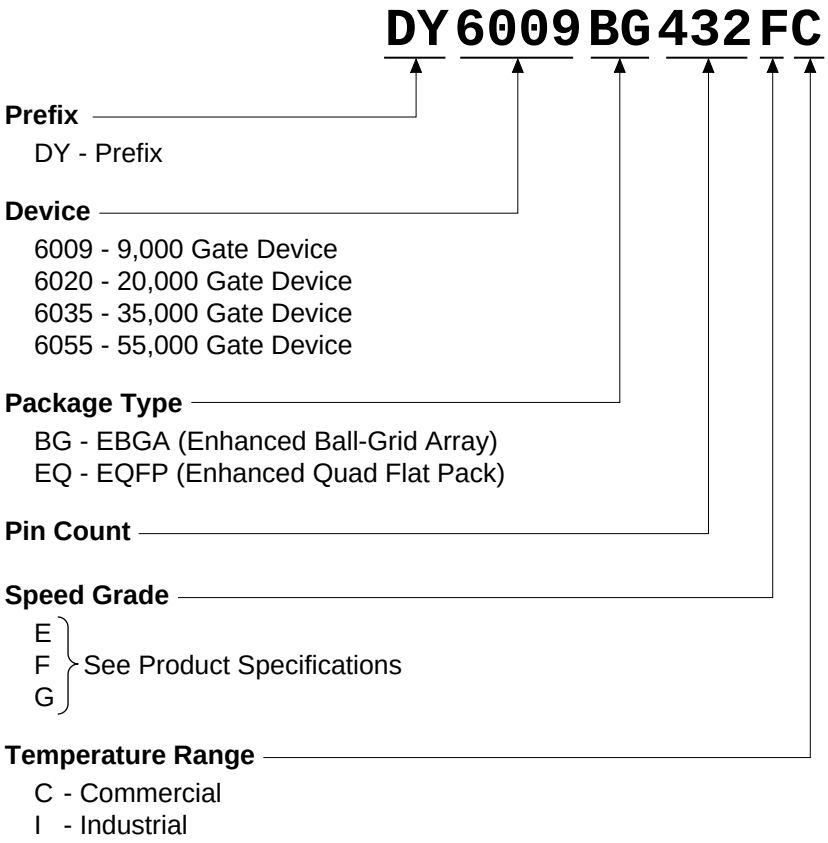


Figure 29: Package Drawing of 240-pin EQFP

Ordering Information

Order codes are shown below.



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