



3.3V CMOS 16-BIT UNIVERSAL BUS DRIVER WITH 3-STATE OUTPUTS AND BUS-HOLD

IDT74ALVCH162334

FEATURES:

- 0.5 MICRON CMOS Technology
- Typical $t_{sk(0)}$ (Output Skew) < 250ps
- ESD > 2000V per MIL-STD-883, Method 3015;
> 200V using machine model (C = 200pF, R = 0)
- 0.635mm pitch SSOP, 0.50mm pitch TSSOP,
and 0.40mm pitch TVSOP packages
- Extended commercial range of - 40°C to + 85°C
- $V_{cc} = 3.3V \pm 0.3V$, Normal Range
- $V_{cc} = 2.7V$ to 3.6V, Extended Range
- $V_{cc} = 2.5V \pm 0.2V$
- CMOS power levels (0.4 μ W typ. static)
- Rail-to-Rail output swing for increased noise margin

Drive Features for ALVCH162334:

- Balanced Output Drivers: $\pm 12mA$
- Low switching noise

APPLICATIONS:

- SDRAM Modules
- PC Motherboards
- Workstations

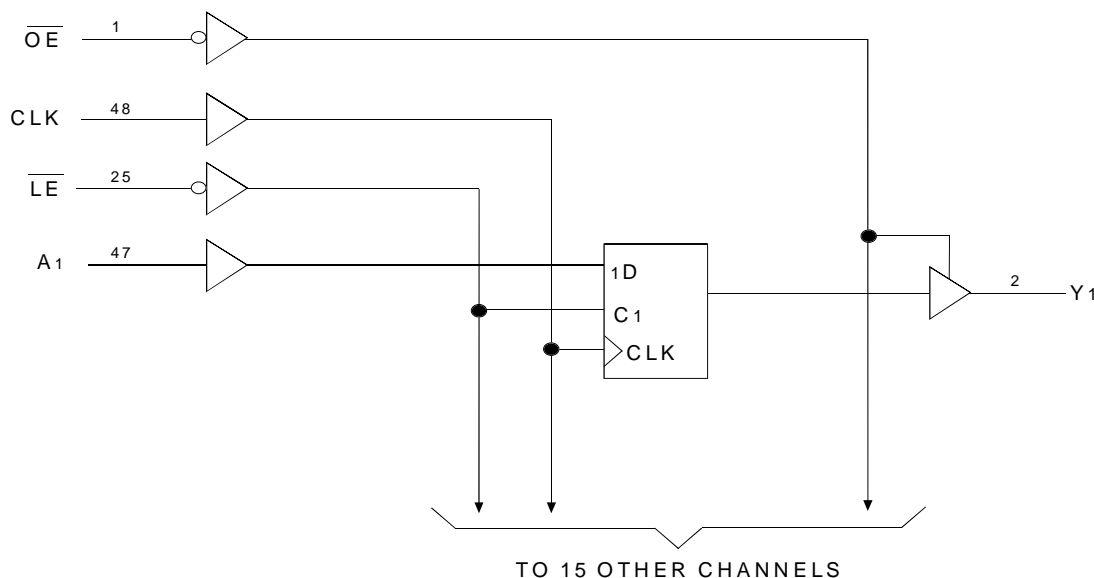
DESCRIPTION:

This 16-bit universal bus driver is built using advanced dual metal CMOS technology. Data flow from A to Y is controlled by the output-enable (\overline{OE}) input. The device operates in the transparent mode when the latch-enable (\overline{LE}) input is low. When \overline{LE} is high, the A data is latched if the clock (CLK) input is held at a high or low logic level. If \overline{LE} is high, the A data is stored in the latch/flip-flop on the low-to-high transition of CLK. When \overline{OE} is high, the outputs are in the high-impedance state.

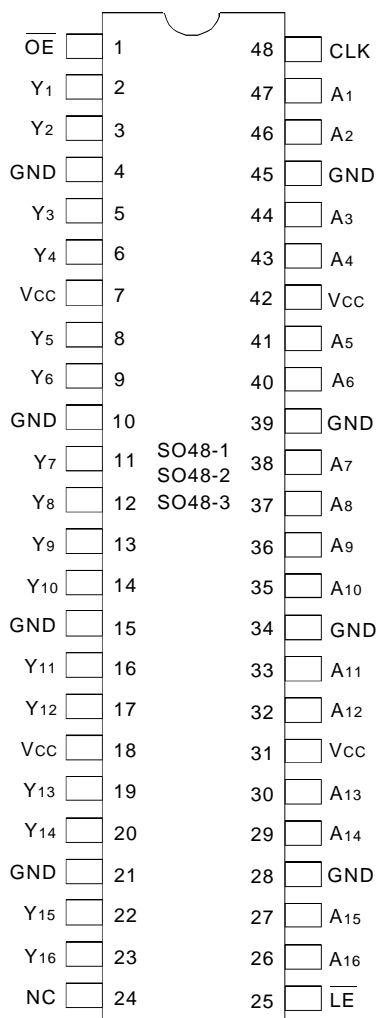
The ALVCH162334 has series resistors in the device output structure which will significantly reduce line noise when used with light loads. This driver has been designed to drive $\pm 12mA$ at the designated threshold levels.

The ALVCH162334 has "bus-hold" which retains the inputs' last state whenever the input bus goes to a high impedance. This prevents floating inputs and eliminates the need for pull-up/down resistors.

Functional Block Diagram



PIN CONFIGURATION



SSOP/
TSSOP/TVSOP
TOP VIEW

PIN DESCRIPTION

Pin Names	Description
\overline{OE}	3-State Output Enable Inputs (Active LOW)
CLK	Register Input Clock
\overline{LE}	Latch Enable (Transparent LOW)
Ax	Data Inputs ⁽¹⁾
Yx	3-State Outputs
NC	No Internal Connection

NOTE:

1. These pins have "Bus-Hold." All other pins are standard inputs, outputs, or I/Os.

ABSOLUTE MAXIMUM RATING (1)

Symbol	Description	Max.	Unit
VTERM ⁽²⁾	Terminal Voltage with Respect to GND	- 0.5 to + 4.6	V
VTERM ⁽³⁾	Terminal Voltage with Respect to GND	- 0.5 to Vcc + 0.5	V
TSTG	Storage Temperature	- 65 to + 150	°C
IOUT	DC Output Current	- 50 to + 50	mA
I _{IK}	Continuous Clamp Current, V _I < 0 or V _I > Vcc	± 50	mA
I _{OK}	Continuous Clamp Current, V _O < 0	- 50	mA
I _{CC}	Continuous Current through each Vcc or GND	± 100	mA

NEW16link

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Vcc terminals.
3. All terminals except Vcc.

CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	5	7	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	7	9	pF
C _{I/O}	I/O Port Capacitance	V _{IN} = 0V	7	9	pF

NEW16link

NOTE:

1. As applicable to the device type.

FUNCTION TABLE (1)

Inputs				Outputs
\overline{OE}	\overline{LE}	CLK	Ax	Yx
H	X	X	X	Z
L	L	X	L	L
L	L	X	H	H
L	H	↑	L	L
L	H	↑	H	H
L	H	L or H	X	Y ₀ ⁽²⁾

NOTES:

1. H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High-Impedance
↑ = LOW-to-HIGH Transition
2. Output level before the indicated steady-state input conditions were established.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Condition: TA = -40°C to +85°C

Symbol	Parameter	Test Conditions		Min.	Typ. ⁽¹⁾	Max.	Unit
VIH	Input HIGH Voltage Level	VCC = 2.3V to 2.7V		1.7	—	—	V
		VCC = 2.7V to 3.6V		2	—	—	
VIL	Input LOW Voltage Level	VCC = 2.3V to 2.7V		—	—	0.7	V
		VCC = 2.7V to 3.6V		—	—	0.8	
I _{IH}	Input HIGH Current	VCC = 3.6V	V _I = VCC	—	—	± 5	μA
I _{IL}	Input LOW Current	VCC = 3.6V	V _I = GND	—	—	± 5	
I _{OZH}	High Impedance Output Current (3-State Output pins)	VCC = 3.6V	V _O = VCC	—	—	± 10	μA
I _{OZL}			V _O = GND	—	—	± 10	μA
V _{IK}	Clamp Diode Voltage	VCC = 2.3V, I _{IN} = -18mA		—	-0.7	-1.2	V
V _H	Input Hysteresis	VCC = 3.3V		—	100	—	mV
I _{CCL}	Quiescent Power Supply Current	VCC = 3.6V		—	0.1	40	μA
I _{CCH}		V _{IN} = GND or VCC					
I _{CCZ}							
ΔI _{CC}	Quiescent Power Supply Current Variation	One input at VCC - 0.6V, other inputs at VCC or GND		—	—	750	μA

NEW16link

NOTE:

1. Typical values are at VCC = 3.3V, +25°C ambient.

BUS-HOLD CHARACTERISTICS

Symbol	Parameter ⁽¹⁾	Test Conditions		Min.	Typ. ⁽²⁾	Max.	Unit
I _{BHH}	Bus-Hold Input Sustain Current	VCC = 3.0V	V _I = 2.0V	-75	—	—	μA
			V _I = 0.8V	75	—	—	
I _{BHL}	Bus-Hold Input Sustain Current	VCC = 2.3V	V _I = 1.7V	-45	—	—	μA
			V _I = 0.7V	45	—	—	
I _{BHHO}	Bus-Hold Input Overdrive Current	VCC = 3.6V	V _I = 0 to 3.6V	—	—	± 500	μA
I _{BHLO}							

NEW16link

NOTES:

1. Pins with Bus-hold are identified in the pin description.
2. Typical values are at VCC = 3.3V, +25°C ambient.

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Max.	Unit
VOH	Output HIGH Voltage	V _{CC} = 2.3V to 3.6V	I _{OH} = - 0.1mA	V _{CC} - 0.2	—	V
		V _{CC} = 2.3V	I _{OH} = - 4mA	1.9	—	
			I _{OH} = - 6mA	1.7	—	
		V _{CC} = 2.7V	I _{OH} = - 4mA	2.2	—	
			I _{OH} = - 8mA	2	—	
		V _{CC} = 3.0V	I _{OH} = - 6mA	2.4	—	
I _{OH} = - 12mA	2		—			
VOL	Output LOW Voltage	V _{CC} = 2.3V to 3.6V	I _{OL} = 0.1mA	—	0.2	V
		V _{CC} = 2.3V	I _{OL} = 4mA	—	0.4	
			I _{OL} = 6mA	—	0.55	
		V _{CC} = 2.7V	I _{OL} = 4mA	—	0.4	
			I _{OL} = 8mA	—	0.6	
		V _{CC} = 3.0V	I _{OL} = 6mA	—	0.55	
I _{OL} = 12mA	—		0.8			

NEW16link

NOTE:

- V_{IH} and V_{IL} must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate V_{CC} range. T_A = - 40°C to + 85°C.

OPERATING CHARACTERISTICS, T_A = 25°C

Symbol	Parameter	Test Conditions	V _{CC} = 2.5V ± 0.2V	V _{CC} = 3.3V ± 0.3V	Unit
			Typical	Typical	
CPD	Power Dissipation Capacitance Outputs enabled	C _L = 0pF, f = 10Mhz	32	37	pF
CPD	Power Dissipation Capacitance Outputs disabled		7	11.5	pF

SWITCHING CHARACTERISTICS (1)

Symbol	Parameter	V _{CC} = 2.5V ± 0.2V		V _{CC} = 2.7V		V _{CC} = 3.3V ± 0.3V		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
f _{MAX}		150	—	150	—	150	—	MHz
t _{PLH} t _{PHL}	Propagation Delay A _x to Y _x	1	4.4	—	4.5	1.1	3.9	ns
t _{PLH} t _{PHL}	Propagation Delay $\overline{\text{LE}}$ to Y _x	1	5.8	—	6	1.3	5	ns
t _{PLH} t _{PHL}	Propagation Delay CLK to Y _x	1	5.2	—	5.4	1	4.9	ns
t _{PZH} t _{PZL}	Output Enable Time $\overline{\text{OE}}$ to Y _x	1	6.4	—	6.4	1.1	5.4	ns
t _{PHZ} t _{PLZ}	Output Disable Time $\overline{\text{OE}}$ to Y _x	1	4.7	—	5.1	1.7	5	ns
t _w	Pulse Duration, $\overline{\text{LE}}$ LOW	3.3	—	3.3	—	3.3	—	ns
t _w	Pulse Duration, CLK HIGH or LOW	3.3	—	3.3	—	3.3	—	ns
t _{su}	Setup Time, data before CLK \uparrow	1.4	—	1.7	—	1.5	—	ns
t _{su}	Setup Time, data before $\overline{\text{LE}}\uparrow$, CLK HIGH	1.2	—	1.6	—	1.3	—	ns
t _{su}	Setup Time, data before $\overline{\text{LE}}\uparrow$, CLK LOW	1.4	—	1.5	—	1.2	—	ns
t _h	Hold Time, data after CLK \uparrow	0.9	—	0.9	—	0.9	—	ns
t _h	Hold Time, data after $\overline{\text{LE}}\uparrow$, CLK HIGH or LOW	1.2	—	1.1	—	1.1	—	ns
tsk(o)	Output Skew ⁽²⁾	—	—	—	—	—	500	ps

NOTES:

1. See test circuits and waveforms. T_A = -40°C to +85°C.
2. Skew between any two outputs of the same package and switching in the same direction.

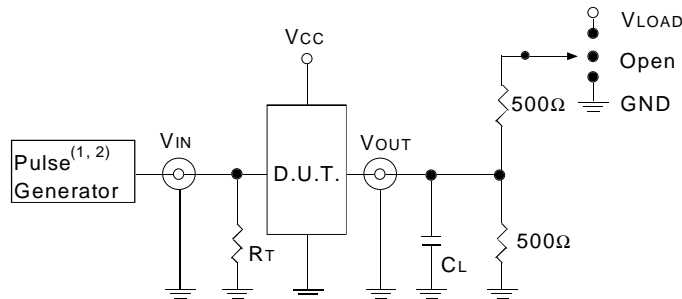
TEST CIRCUITS AND WAVEFORMS

TEST CONDITIONS

Symbol	V _{CC} (1)= 3.3V±0.3V	V _{CC} (1)= 2.7V	V _{CC} (2)= 2.5V±0.2V	Unit
V _{LOAD}	6	6	2 x V _{CC}	V
V _{IH}	2.7	2.7	V _{CC}	V
V _T	1.5	1.5	V _{CC} / 2	V
V _{LZ}	300	300	150	mV
V _{HZ}	300	300	150	mV
C _L	50	50	30	pF

NEW16link

TEST CIRCUITS FOR ALL OUTPUTS



ALVC Link

DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

NOTES:

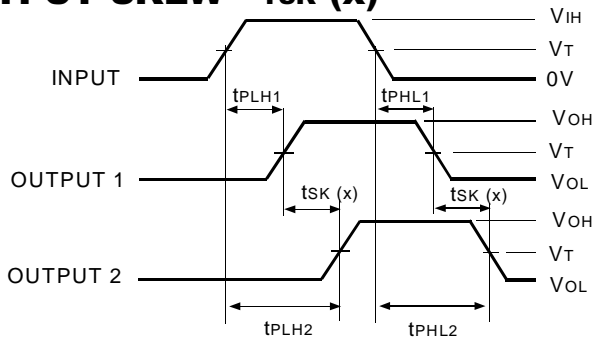
1. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns.
2. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_F ≤ 2ns; t_R ≤ 2ns.

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	V _{LOAD}
Disable High Enable High	GND
All Other tests	Open

NEW16link

OUTPUT SKEW - t_{SK}(x)



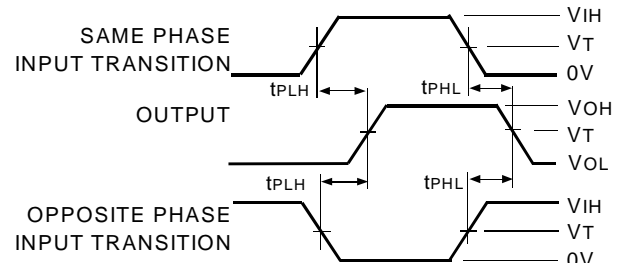
$$t_{SK}(x) = |t_{PLH2} - t_{PLH1}| \text{ or } |t_{PHL2} - t_{PHL1}|$$

ALVC Link

NOTES:

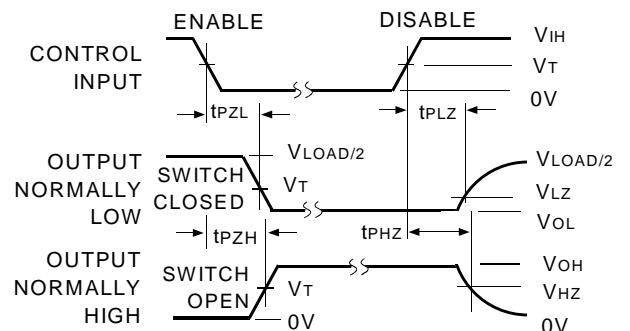
1. For t_{SK}(o) OUTPUT1 and OUTPUT2 are any two outputs.
2. For t_{SK}(b) OUTPUT1 and OUTPUT2 are in the same bank.

PROPAGATION DELAY



ALVC Link

ENABLE AND DISABLE TIMES

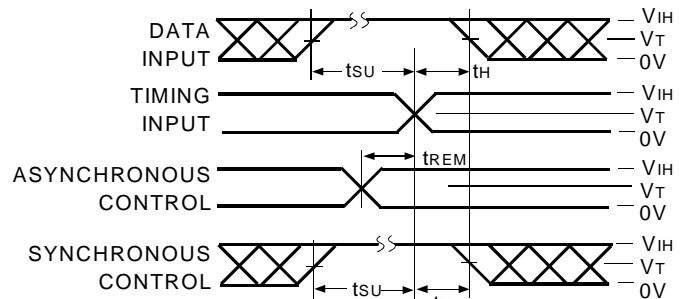


ALVC Link

NOTE:

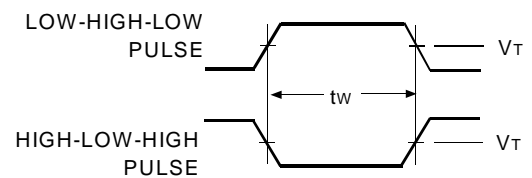
1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

SET-UP, HOLD, AND RELEASE TIMES



ALVC Link

PULSE WIDTH



ALVC Link

