KMM332F400CS-L & KMM332F410CS-L Fast Page with EDO Mode

4M x 32 DRAM SODIMM Using 4MX4, 4K & 2K Ref., 3.3V, Low power/Self-Refresh

GENERAL DESCRIPTION

The Samsung KMM332F40(1)0CS is a 4Mx32bits Dynamic RAM high density memory module. The Samsung KMM332F40(1)0CS consists of eight CMOS 4Mx4bits DRAMs in 24-pinTSOPII packages mounted on a 72-pin six layer zig-zag glass-epoxy substrate. A 0.1 or 0.22uF decoupling capacitor is mounted on the printed circuit board for each DRAM. The KMM332F40(1)0CS is a Small Out-line Dual In-line Memory Module with edge connections and is intended for mounting into 72-pin dual readout zigzag edge connector sockets.

PERFORMANCE RANGE

Speed	t_{RAC}	t_{CAC}	t_{RC}	t_{HPC}
-L5	50ns	13ns	90ns	25ns
-L6	60ns	15ns	110ns	30ns

FEATURES

- Part Identification
  - KMM332F400CS-L5/L6
    (4096 cycles/128ms Ref, TSOP, Low Power, 50/60ns)
  - KMM332F410CS-L5/L6
    (2048 cycles/128ms Ref, TSOP, Low Power, 50/60ns)
- Fast Page with EDO Mode Operation
- $\overline{CAS}$-before-$\overline{RAS}$ Refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- Self refresh capability
- LVTTL compatible inputs and outputs
- Single +3.3V±0.3V power supply
- JEDEC standard PDPin & pinout (72pin)
- PCB : Height(1000mil), double sided component

PIN CONFIGURATIONS

Pin	Symbol	Pin	Symbol
1	V_{SS}	37	DQ18
2	DQ0	38	DQ19
3	DQ1	39	V_{SS}
4	DQ2	40	$\overline{CAS0}$
5	DQ3	41	$\overline{CAS2}$
6	DQ4	42	$\overline{CAS3}$
7	DQ5	43	$\overline{CAS1}$
8	DQ6	44	$\overline{RAS0}$
9	DQ7	45	NC
10	V_{CC}	46	NC
11	PD1	47	$\overline{W}$
12	A0	48	NC
13	A1	49	DQ20
14	A2	50	DQ21
15	A3	51	DQ22
16	A4	52	DQ23
17	A5	53	DQ24
18	A6	54	DQ25
19	A10	55	NC
20	NC	56	DQ27
21	DQ9	57	DQ28
22	DQ10	58	DQ29
23	DQ11	59	DQ31
24	DQ12	60	DQ30
25	DQ13	61	V_{CC}
26	DQ14	62	DQ32
27	DQ15	63	DQ33
28	A7	64	DQ34
29	A11	65	NC
30	V_{CC}	66	PD2
31	A8	67	PD3
32	A9	68	PD4
33	NC	69	PD5
34	$\overline{RAS2}$	70	PD6
35	DQ16	71	PD7
36	NC	72	V_{SS}

PIN NAMES

Pin Name	Function
A0 - A11	Address Inputs (4K ref)
A0 - A10	Address Inputs (2K ref)
DQ(0 -7,9-16, 18-25,27-34)	Data In/Out
$\overline{W}$	Read/Write Enable
$\overline{RAS0}$, $\overline{RAS2}$	Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS3}$	Column Address Strobe
PD1 -PD7	Presence Detect
V_{CC}	Power(+3.3V)
V_{SS}	Ground
NC	No Connection

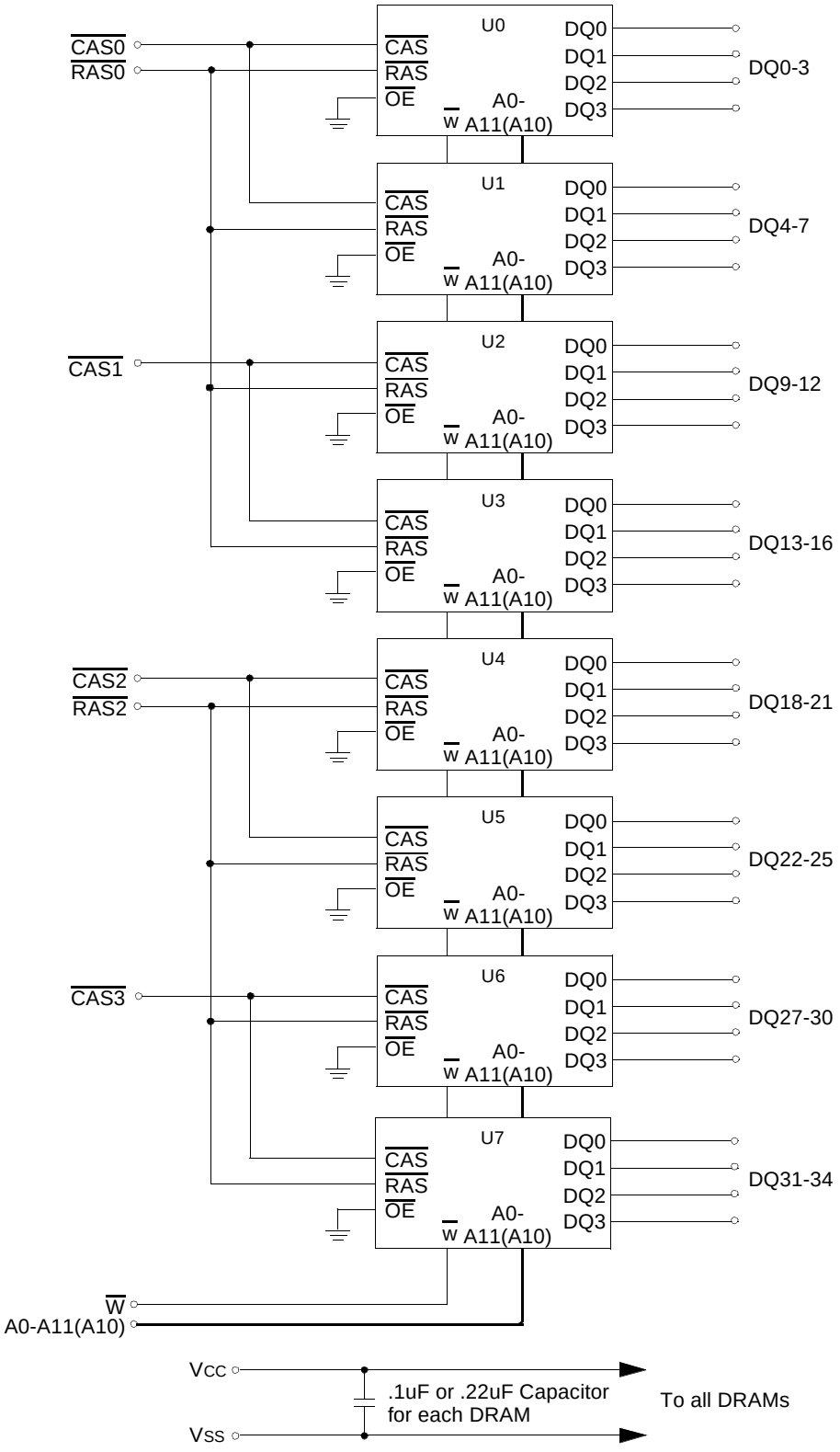
PRESENCE DETECT PINS (Optional)

Pin	50NS	60NS
PD1	NC	NC
PD2	NC	NC
PD3	V_{SS}	V_{SS}
PD4	NC	NC
PD5	V_{SS}	NC
PD6	V_{SS}	NC
PD7	NC	NC

* Pin Connection Charging Available

NOTE : A11 is used for only KMM332F400CS (4K ref.)

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on any pin relative V_{SS}	V_{IN}, V_{OUT}	-0.5 to +4.6	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	-0.5 to +4.6	V
Storage Temperature	T_{stg}	-55 to +150	°C
Power Dissipation	P_D	8	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for intended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	3.0	3.3	3.6	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.0	-	V_{CC}+0.3*1	V
Input Low Voltage	V_{IL}	-0.3*2	-	0.8	V

*1 : V_{CC}+1.3V/15ns, Pulse width is measured at V_{CC}.
*2 : -1.3V/15ns, Pulse width is measured at V_{SS}.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Symbol	Speed	KMM332F400CS		KMM332F410CS		Unit
		Min	Max	Min	Max	
I_{CC1}	-L5	-	720	-	880	mA
	-L6	-	640	-	800	mA
I_{CC2}	Don't care	-	8	-	8	mA
I_{CC3}	-L5	-	720	-	880	mA
	-L6	-	640	-	800	mA
I_{CC4}	-L5	-	640	-	720	mA
	-L6	-	560	-	640	mA
I_{CC5}	Don't care	-	1.6	-	1.6	mA
I_{CC6}	-L5	-	720	-	880	mA
	-L6	-	640	-	800	mA
I_{CC7}	Don't care	-	2000	-	2000	uA
I_{CCS}	Don't care	-	1600	-	1600	uA
$I_{I(L)}$	Don't care	-40	40	-40	40	uA
$I_{O(L)}$		-5	5	-5	5	uA
V_{OH}	Don't care	2.4	-	2.4	-	V
V_{OL}		-	0.4	-	0.4	V

I_{CC1} : Operating Current * ($\overline{RAS}$, $\overline{CAS}$, Address cycling @t_{RC}=min)
I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})
I_{CC3} : $\overline{RAS}$ Only Refresh Current * ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ cycling @t_{RC}=min)
I_{CC4} : EDO Mode Current * ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling : t_{HPC}=min)
I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{CC}-0.2V)
I_{CC6} : $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current * ($\overline{RAS}$ and $\overline{CAS}$ cycling @t_{RC}=min)
I_{CC7} : Battery back-up current, Average power supply current, Battery back-up mode
Input high voltage(V_{IH})=V_{CC}-0.2V, Input low voltage(V_{IL})=0.2V, $\overline{CAS}$=0.2V)
DQ0-31=Don't care, t_{RC}=31.25us (4K Ref.),62.5us (2K Ref.) , t_{RAS}=t_{RAS}min~300ns
I_{CCS} : Self Refresh Current ($\overline{RAS}$=$\overline{CAS}$-V_{IL} , $\overline{W}$=$\overline{OE}$=A0-A11=V_{CC}-0.2V or 0.2V, DQ0-DQ31=V_{CC}-0.2V,0.2V or OPEN)
$I_{I(L)}$: Input Leakage Current (Any input 0≤V_{IN}≤V_{CC}+0.3V, all other pins not under test=0 V)
$I_{O(L)}$: Output Leakage Current(Data Out is disabled, 0V≤V_{OUT}≤V_{CC})
V_{OH} : Output High Voltage Level (I_{OH} = -2mA)
V_{OL} : Output Low Voltage Level (I_{OL} = 2mA)

* NOTE : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one EDO mode cycle, t_{HPC}.

CAPACITANCE (T_A = 25°C, Vcc=3.3V, f = 1MHz)

Item	Symbol	Min	Max	Unit
Input capacitance[A0-A11(A10)]	C_{IN1}	-	60	pF
Input capacitance[$\overline{W}$]	C_{IN2}	-	75	pF
Input capacitance[$\overline{RAS0}$, $\overline{RAS2}$]	C_{IN3}	-	45	pF
Input capacitance[$\overline{CAS0}$ - $\overline{CAS3}$]	C_{IN4}	-	30	pF
Input/Output capacitance[DQ0-7,9-16,18-25,27-34]	C_{DQ}	-	20	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, V_{CC}=3.3V±0.3V See notes 1,2.)

Test condition : V_{ih}/V_{il}=2.0/0.8V, V_{oh}/V_{ol}=2.0/0.8V, output loading CL=100pF

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	90		110		ns	
Access time from $\overline{RAS}$	t_{RAC}		50		60	ns	3,4,10
Access time from $\overline{CAS}$	t_{CAC}		13		15	ns	3,4,5
Access time from column address	t_{AA}		25		30	ns	3,10
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	3		3		ns	3
Output buffer turn-off delay from $\overline{CAS}$	t_{CEZ}	3	13	3	15	ns	6,11,12
Transition time(rise and fall)	t_T	2	50	2	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	30		40		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10K	60	10K	ns	
$\overline{RAS}$ hold time	t_{RSH}	13		15		ns	
$\overline{CAS}$ hold time	t_{CSH}	43		50		ns	
$\overline{CAS}$ pulse width	t_{CAS}	8	10K	10	10K	ns	13
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	37	20	45	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	25	15	30	ns	10
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		ns	
Row address set-up time	t_{ASR}	0		0		ns	
Row address hold time	t_{RAH}	10		10		ns	
Column address set-up time	t_{ASC}	0		0		ns	
Column address hold time	t_{CAH}	8		10		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	25		30		ns	
Read command set-up time	t_{RCS}	0		0		ns	
Read command hold referenced to $\overline{CAS}$	t_{RCH}	0		0		ns	8
Read command hold referenced to $\overline{RAS}$	t_{RRH}	0		0		ns	8
Write command hold time	t_{WCH}	10		10		ns	
Write command pulse width	t_{WP}	10		10		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	13		15		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	8		10		ns	
Data set-up time	t_{DS}	0		0		ns	8
Data hold time	t_{DH}	8		10		ns	8
Refresh period	t_{REF}		128		128	ms	
Write command set-up time	t_{WCS}	0		0		ns	7
$\overline{CAS}$ setup time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	5		5		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	5		5		ns	
$\overline{CAS}$ precharge time (CBR counter test cycle)	t_{CPT}	20		20		ns	

AC CHARACTERISTICS (Countinued)

Test condition : V_{ih}/V_{il}=2.0/0.8V, V_{oh}/V_{ol}=2.0/0.8V, output loading CL=100pF

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Access time from $\overline{CAS}$ precharge	t_{CPA}		28		35	ns	3
Hyper page mode cycle time	t_{HPC}	25		30		ns	13
$\overline{CAS}$ precharge time (Hyper page cycle)	t_{CP}	8		10		ns	
$\overline{RAS}$ pulse width (Hyper page cycle)	t_{RASP}	50	200K	60	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	30		35		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{WRP}	10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{WRH}	10		10		ns	
Output data hold time	t_{DOH}	5		5		ns	
Output buffer turn off delay from $\overline{RAS}$	t_{REZ}	3	13	3	15	ns	
Output buffer turn off delay from $\overline{W}$	t_{WEZ}	3	13	3	15	ns	
$\overline{W}$ to data delay	t_{WED}	15		15		ns	6,11,12
$\overline{W}$ pulse width	t_{WPE}	5		5		ns	6,11
$\overline{RAS}$ pulse width (C-B-R self refresh)	t_{RASS}	100		100		us	
$\overline{RAS}$ precharge time (C-B-R self refresh)	t_{RPS}	90		110		ns	
$\overline{CAS}$ hold time (C-B-R self refresh)	t_{CHS}	-50		-50		ns	

NOTES

1. An initial pause of 200us is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.

2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.

3. Measured with a load equivalent to 1 TTL loads and 100pF.

4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.

5. Assumes that $t_{RCD} \geq t_{RCD}$(max).

6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.

7. t_{WCS} is non restrictive operating parameter.
   It is included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle.

8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.

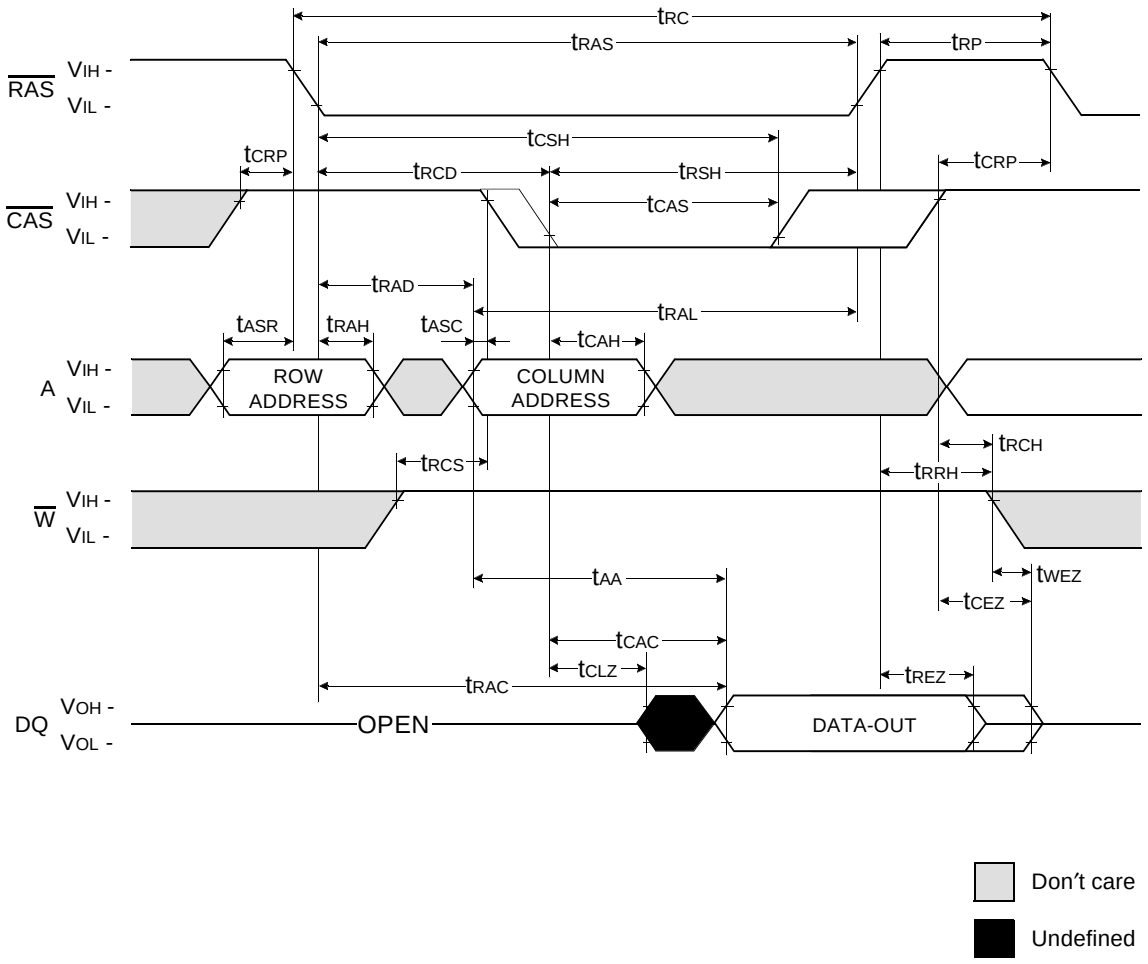
10. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit access time is controlled by t_{AA}.

11. t_{CEZ}(max), t_{REZ}(max), t_{WEZ}(max) and t_{OEZ}(max) define the timeat which the output achieves the open circuit condition and are not referenced to output voltage level.

12. If $\overline{RAS}$ goes to high before $\overline{CAS}$ high going, the open circuit condition of the output is achieved by $\overline{CAS}$ high going. If $\overline{CAS}$ goes to high before $\overline{RAS}$ high going , the open circuit condition of the output is achieved by $\overline{RAS}$ going.

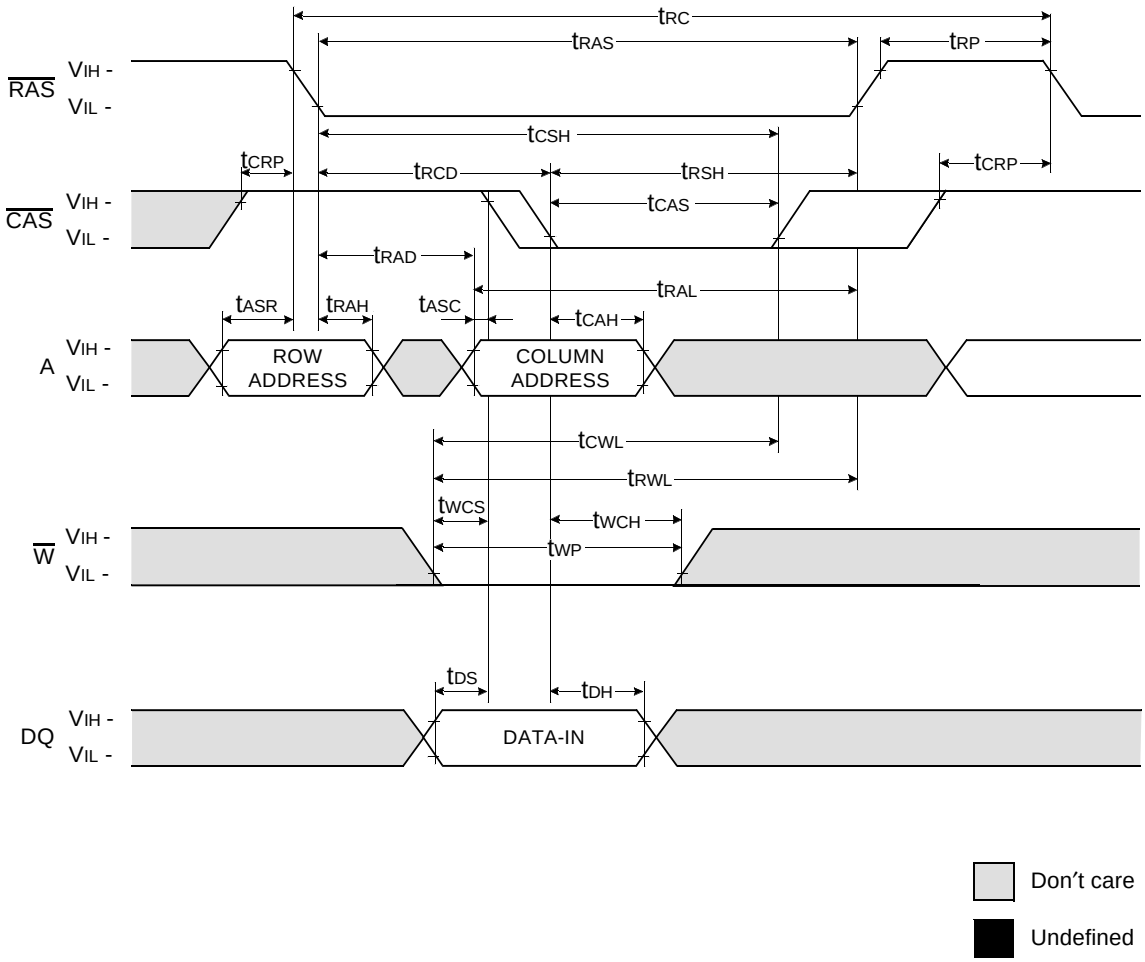
13. $t_{ASC} \geq t_{CP}$ min

READ CYCLE

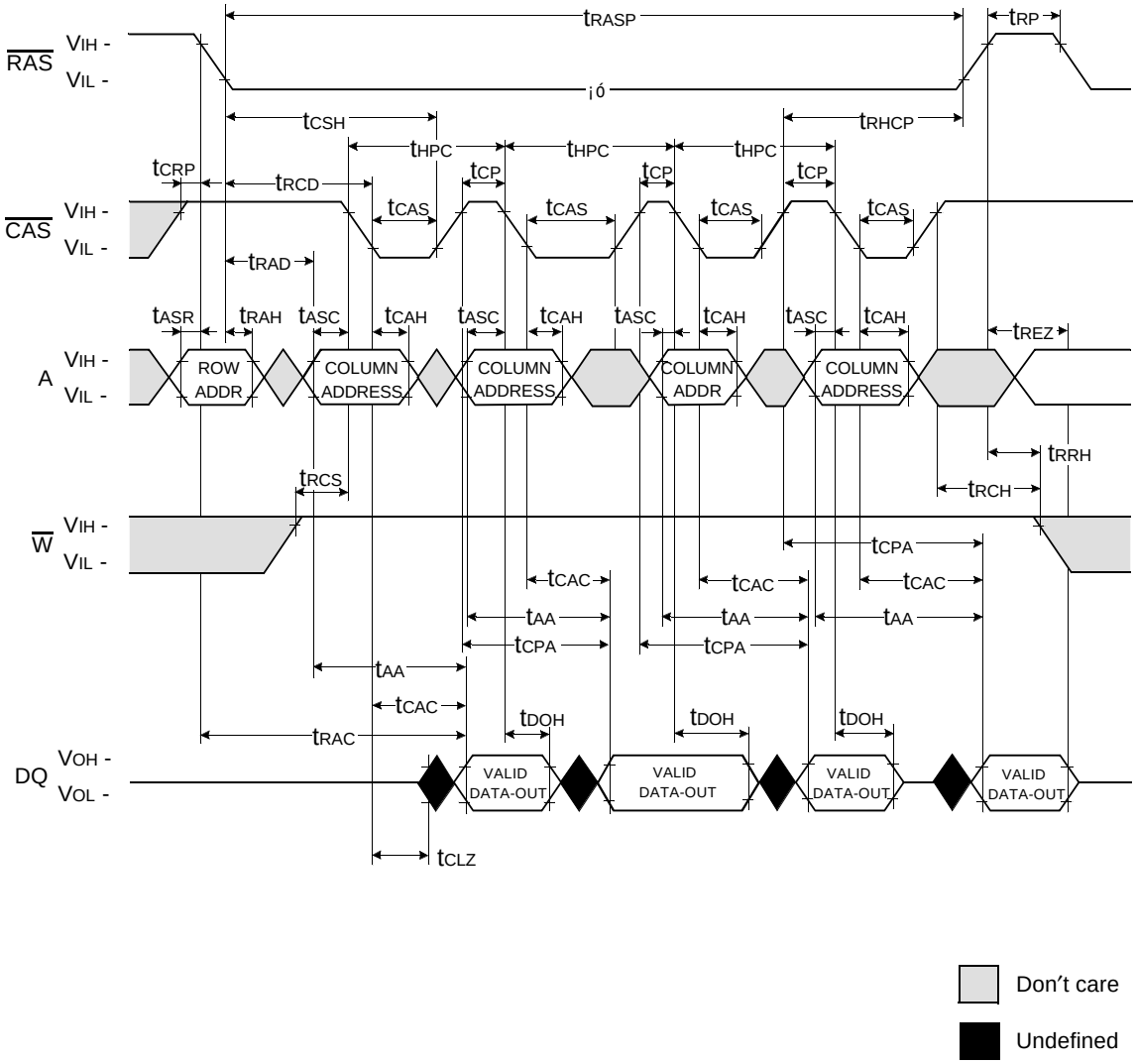

tRC
tRAS
tRP
RAS
VIH -
VIL -
tCSH
tCRP
tRCD
tRSH
tCRP
CAS
VIH -
VIL -
tCAS
tRAD
tRAL
tASR
tRAH
tASC
tCAH
A
VIH -
VIL -
ROW ADDRESS
COLUMN ADDRESS
tRCH
tRCS
tRRH
W
VIH -
VIL -
tAA
tWEZ
tCEZ
tCAC
tCLZ
tREZ
tRAC
DQ
VOH -
VOL -
OPEN
DATA-OUT
Don't care
Undefined

WRITE CYCLE (EARLY WRITE)

NOTE : DOUT = OPEN

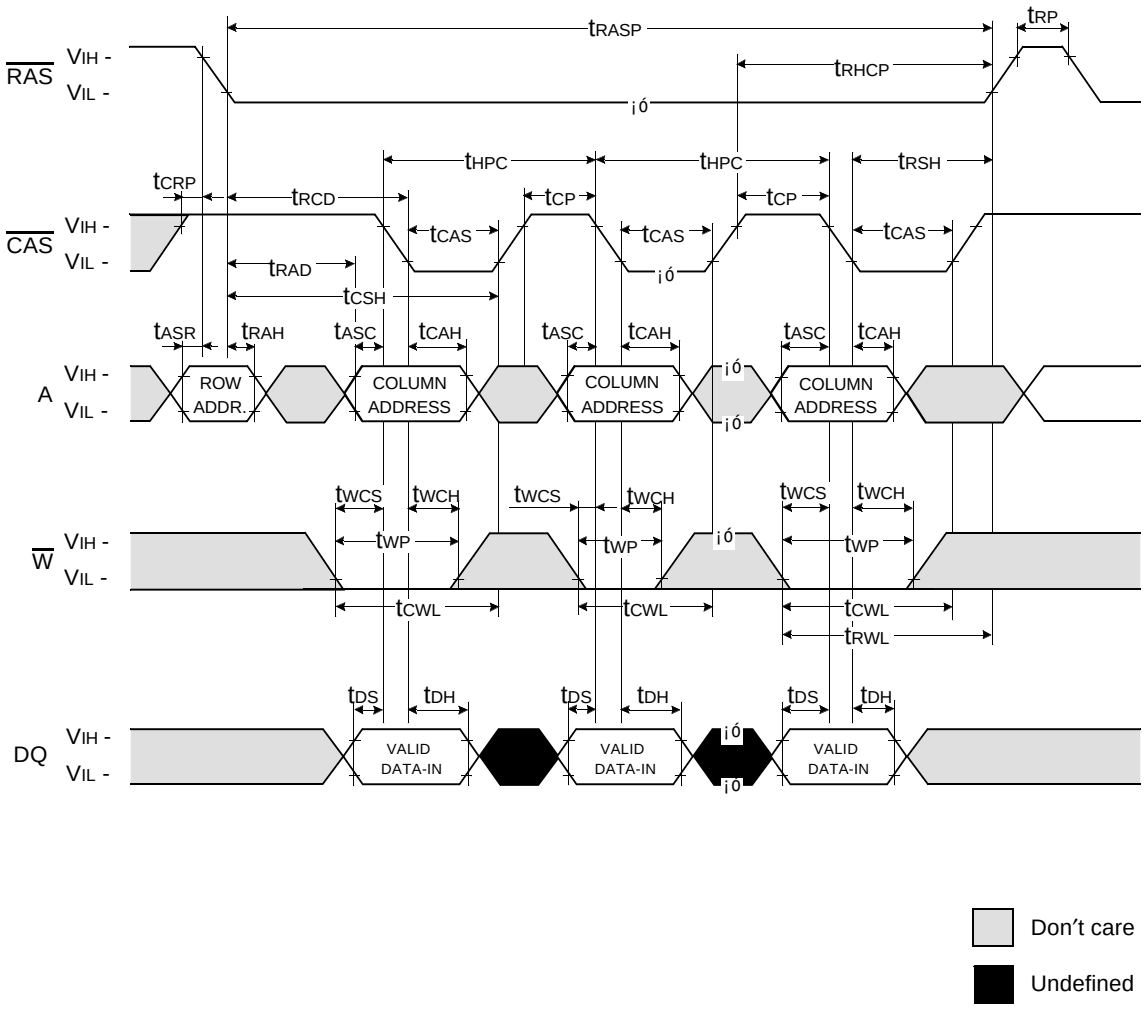


HYPER PAGE READ CYCLE



HYPER PAGE WRITE CYCLE (EARLY WRITE)

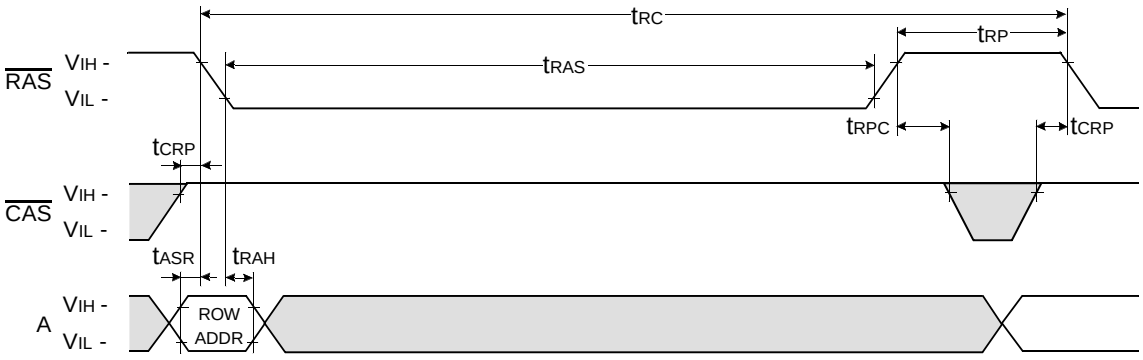
NOTE : DOUT = OPEN



$\overline{RAS}$ - ONLY REFRESH CYCLE*

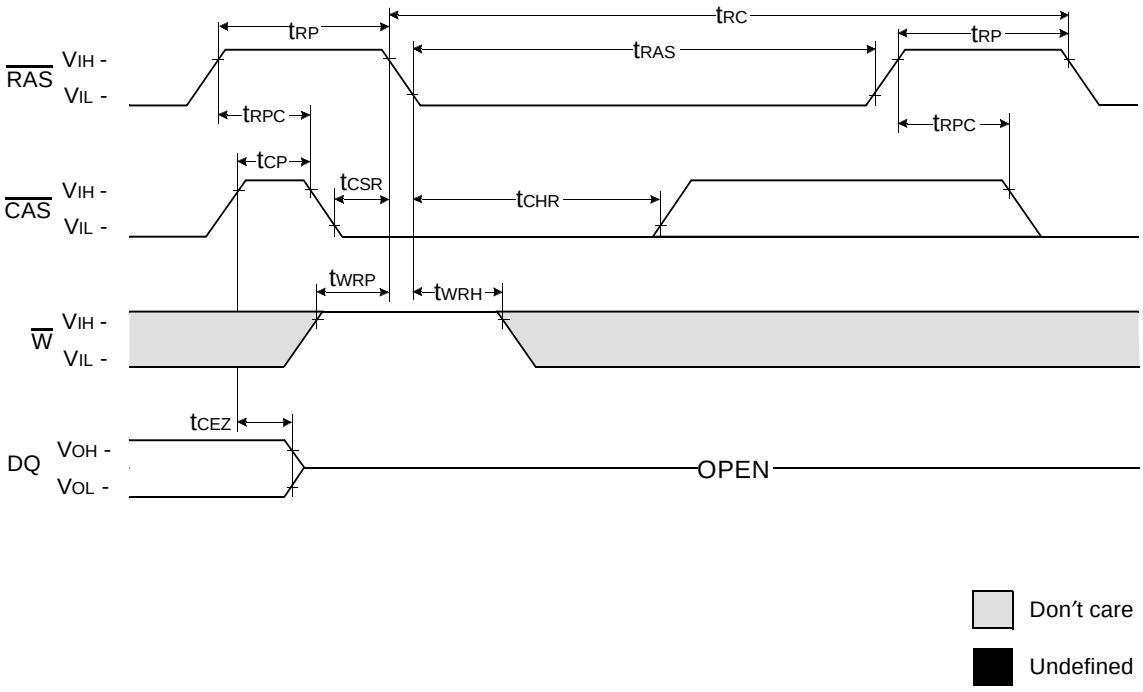
NOTE : $\overline{W}$, $\overline{OE}$, D_{IN} = Don't care

D_{OUT} = OPEN



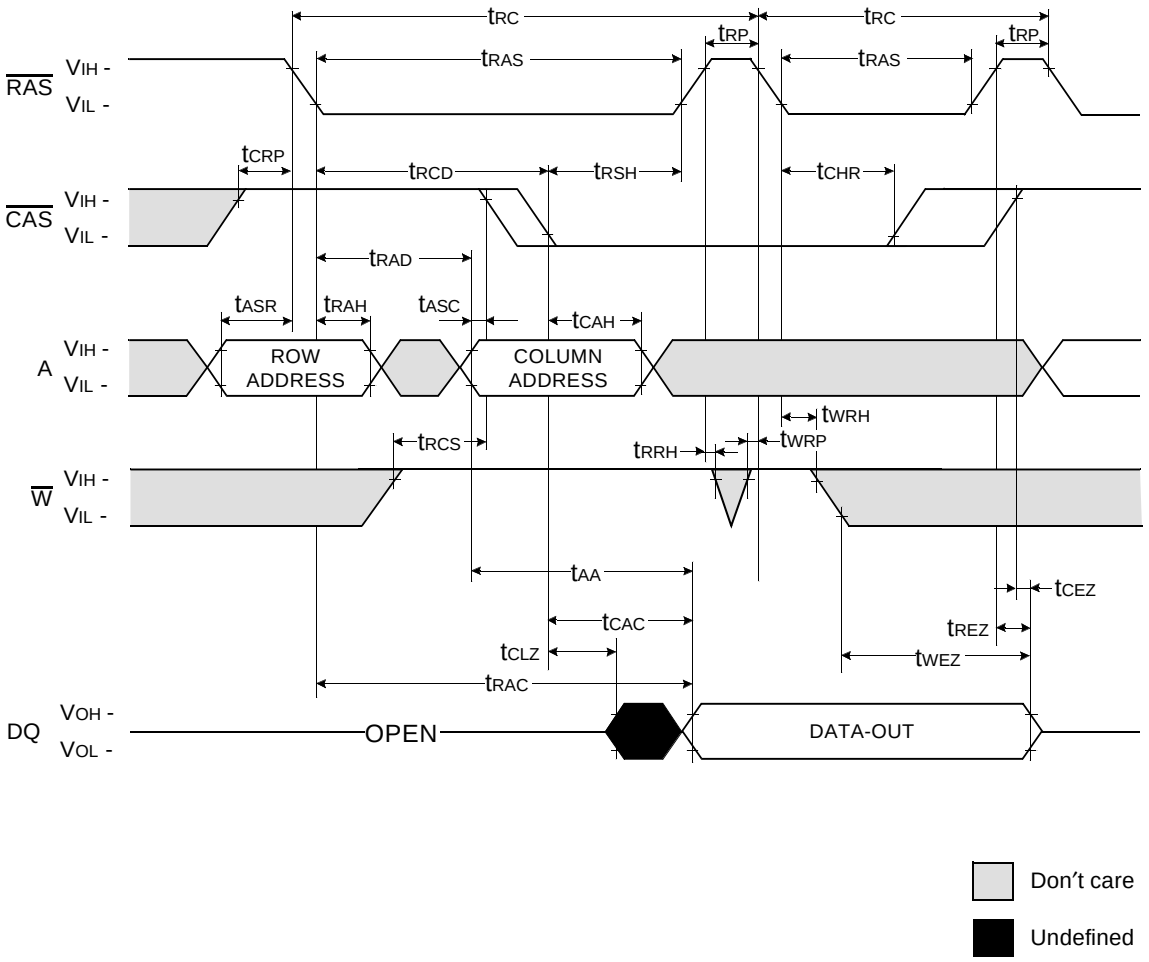
$\overline{CAS}$ - BEFORE - $\overline{RAS}$ REFRESH CYCLE

NOTE : $\overline{OE}$, A = Don't care



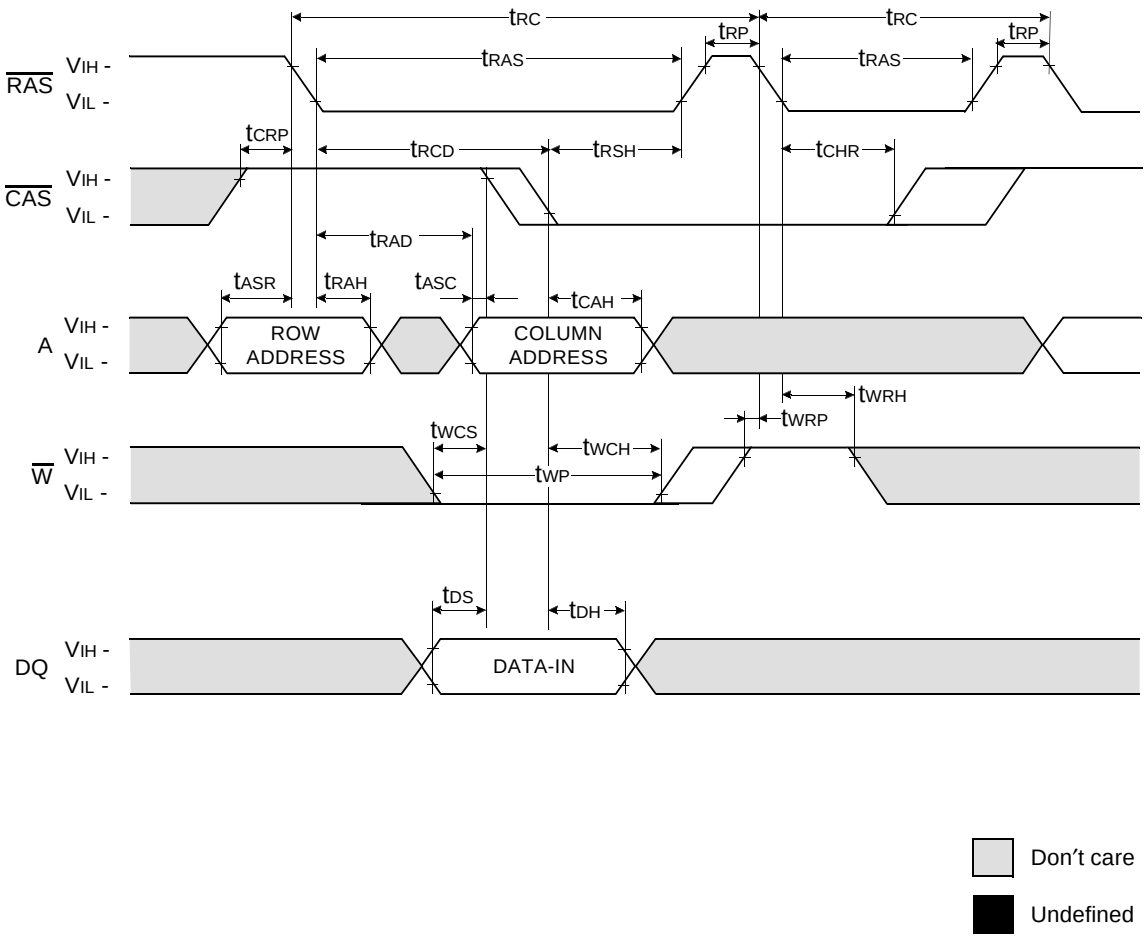
* In $\overline{RAS}$-only refresh cycle of 64Mb A-dile & B-die, when $\overline{CAS}$ signal transits from Low to High, the valid data may be cut off.

HIDDEN REFRESH CYCLE (READ)

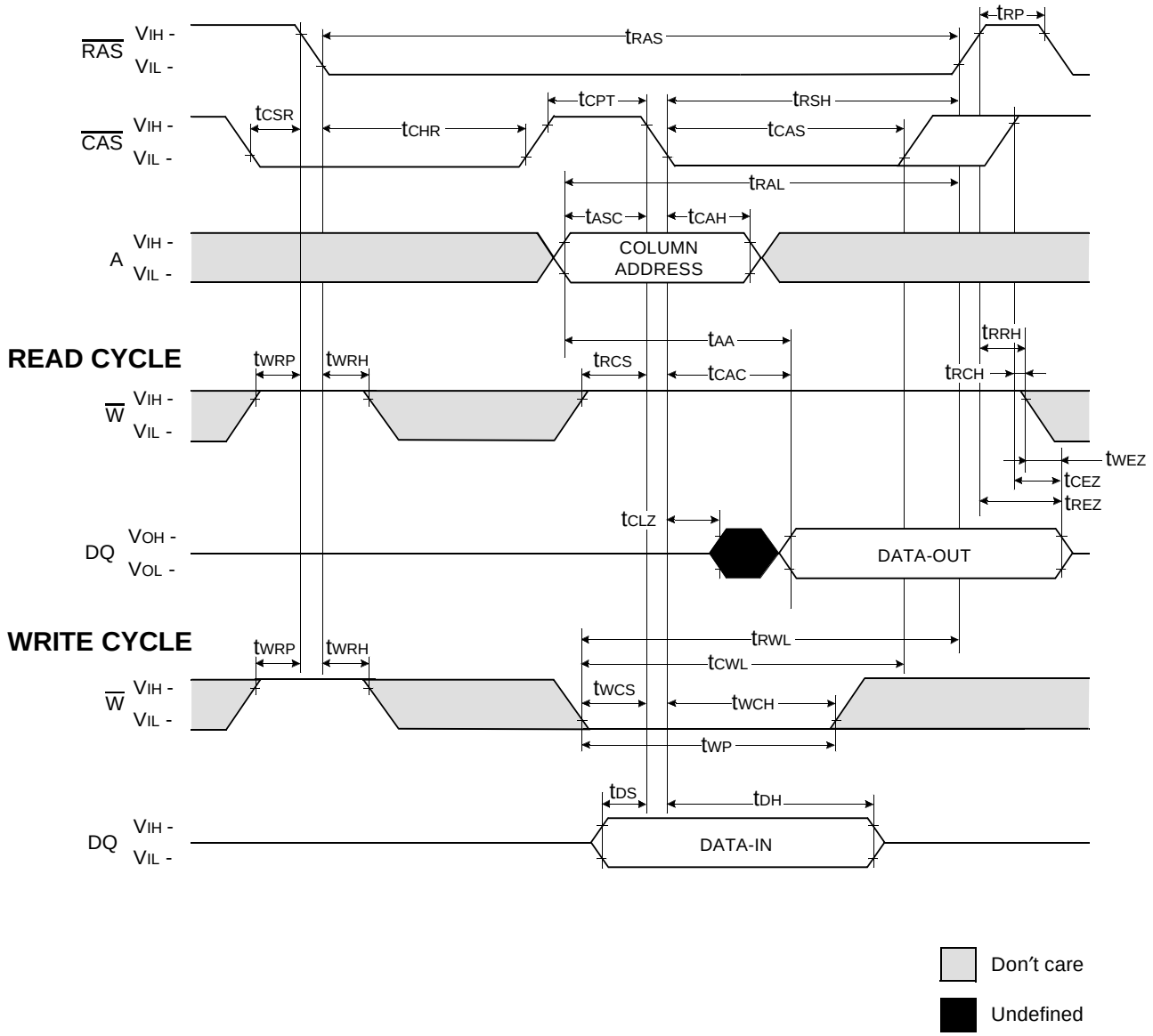


HIDDEN REFRESH CYCLE (WRITE)

NOTE : D_{OUT} = OPEN



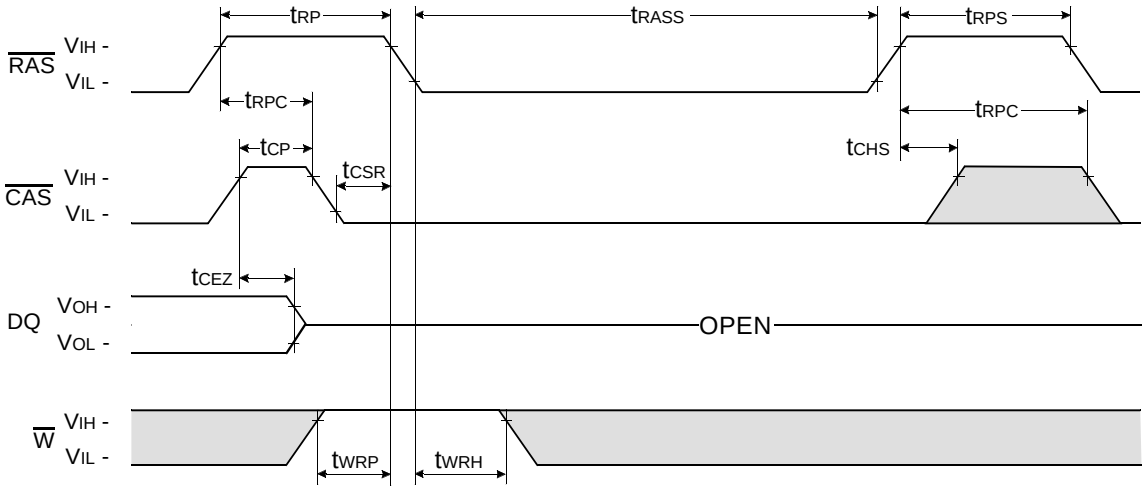
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH COUNTER TEST CYCLE



NOTE : This timing diagram is applied to all devices besides 64M DRAM based modules.

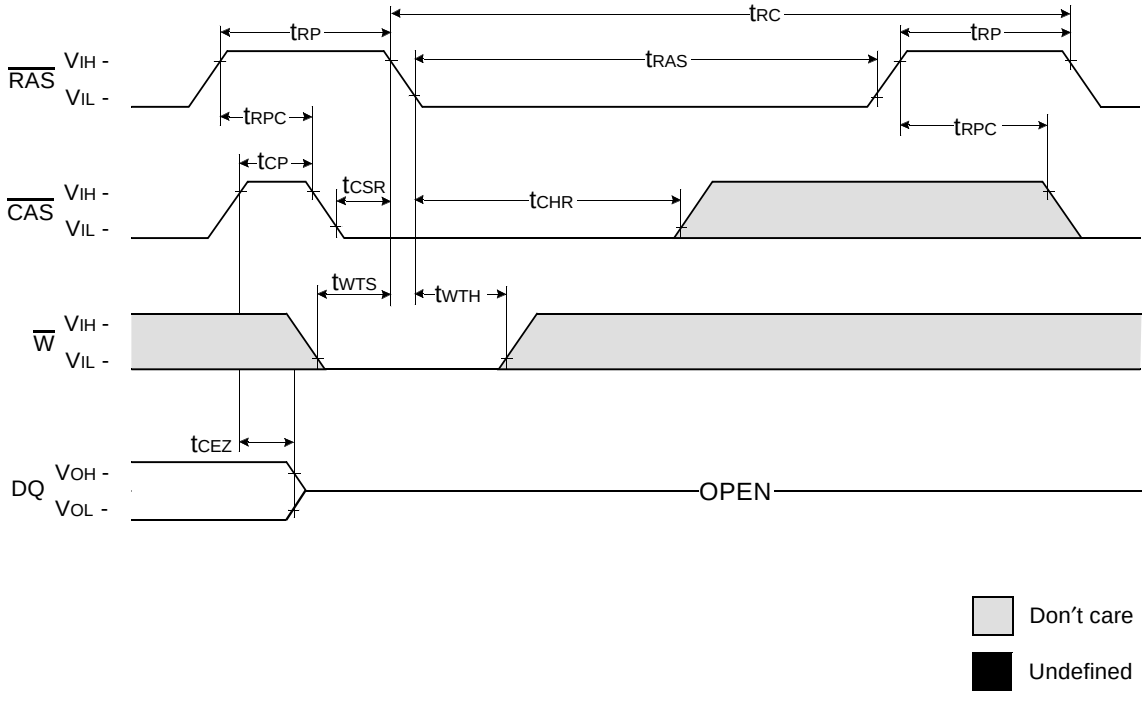
$\overline{CAS}$ - BEFORE - $\overline{RAS}$ SELF REFRESH CYCLE

NOTE : $\overline{OE}$, A = Don't care



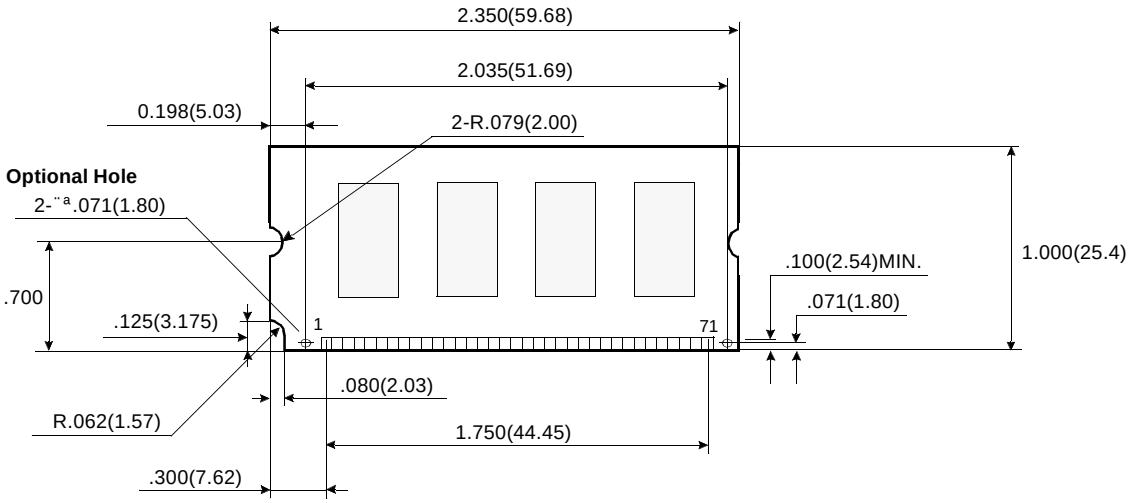
TEST MODE IN CYCLE

NOTE : $\overline{OE}$, A = Don't care

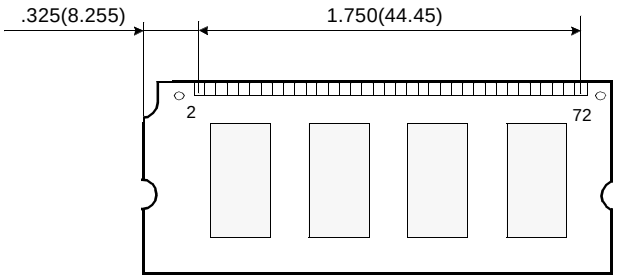


PACKAGE DIMENSIONS

Units : Inches (millimeters)

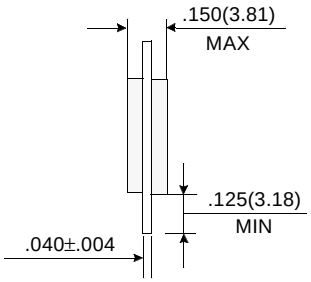


(Front View)

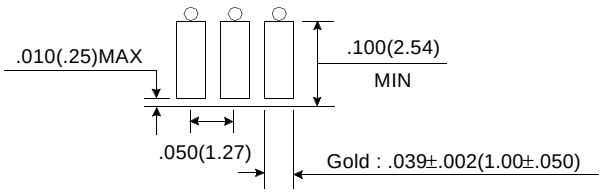


(Back View)

KMM332F40(1)0CS-L



Gold Plating Lead



Tolerances : ±.005(.13) unless otherwise specified

NOTE: The used device is 4Mx4 DRAM, TSOP II

DRAM Part No : KMM332F400CS-L - KM44V4004CS-L (300mil) with Self Refresh
DRAM Part No : KMM332F410CS-L - KM44V4104CS-L (300mil) with Self Refresh

Revision History
Rev 0.0 : Aug. 1997