SiW1602 Link Controller IC

1. INTRODUCTION

The Odyssey™ SiW1602 Link Controller IC is part of Silicon Wave's solutions for Bluetooth™ wireless communications. The SiW1602 provides the Bluetooth link management and control functions in a digital ASIC. Combined with the SiW1502 Radio Modem IC, it provides a complete and cost effective hardware solution to integrate into products.

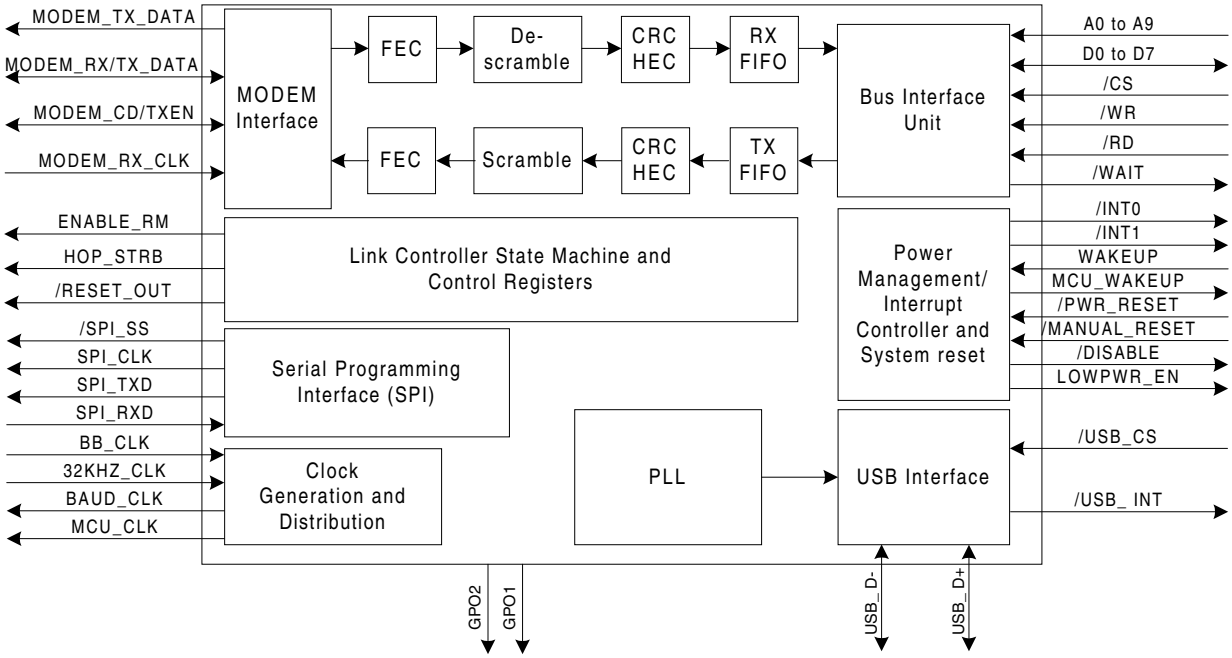


Figure 1: SiW1602 Link Controller IC Functional Block Diagram

2. FEATURES

- Direct interface to SiW1502 Radio Modem.
- USB (compliant to specification v1.1) interface to host computer system.
- Link control function implemented in hardware compliant to Bluetooth specification 1.1.
- Support for all Bluetooth packet types.
- ACL and SCO connections at full speed of 1 Mbit/s.
- Piconet functions, including master/slave switch capabilities.
- Authentication and encryption as defined in the specification.
- Dual on-chip 384-byte transmit and receive FIFOs ensure packet data is never lost due to interrupt latency.
- Programmable interrupt controller.
- Time-critical packet processing.
- Low-power modes such as sniff, hold and park.
- Support for transmit power control and receiver RSSI functions.
- Available in 108-pin fine-pitch BGA flip chip package.

3. APPLICATIONS

The SiW1602 is suitable for all applications requiring packet processing and link management for Bluetooth communications. When combined with the SiW1502 Radio Modem IC, a low power and cost effective solution can be implemented.

- Bluetooth access points.
- Cellular telephones.
- Desktop and notebook PCs and accessories.
- Printers.
- PDAs (personal digital assistant) and palmtops.

A typical design of a Bluetooth compliant product consists of the SiW1502 Radio Modem and the SiW1602 Link Controller along with the Hitachi H8S/2238 or H8S/2214 processor. This example illustrates the connection flow between the system's main components for USB applications:

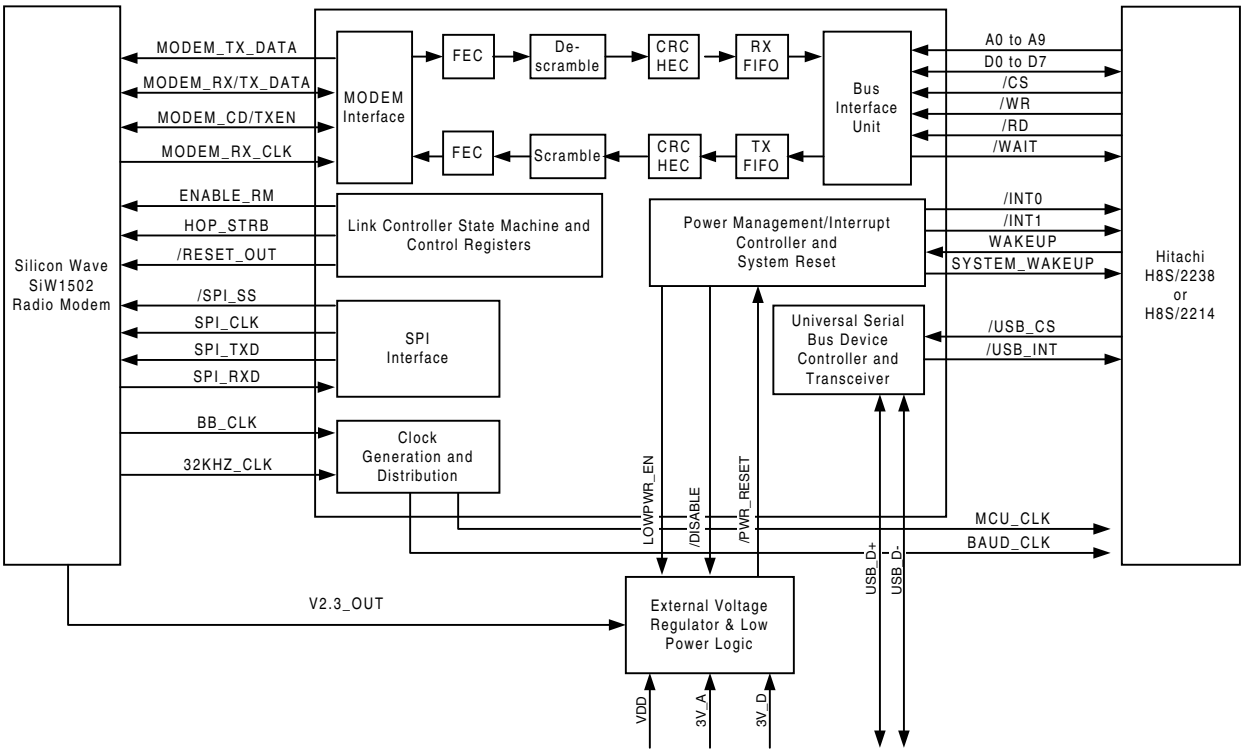


Figure 2: Typical SiW1602 Implementation

UART applications are also possible using the same system components. The UART signals can drive the serial interface on the Hitachi H8S directly. In this case, the USB functionality of the SiW1602 can be turned off.

4. LINK CONTROLLER DESCRIPTION

The link controller hardware in the SiW1602 implements all the real-time, lower-layer protocol processing. This hardware performs the logical protocol processing within the unit that enables the host to communicate over a Bluetooth link. Real-time functions such as frequency hopping, burst timing, synthesizer programming, and clock synchronization are implemented in hardware. Also incorporated within the SiW1602 logic is power management and clock distribution. In addition to the radio control functions described above, the SiW1602 processes Bluetooth transmit and receive data as described below in sections 4.1 through 4.7.

4.1. FEC: Forward Error Correction

FEC corrects errors, which might have occurred during the transmission or receipt of the original data. FEC correction rates at 1/3 and 2/3 are implemented.

4.2. Whiten/De-whiten: Scramble/Unscramble

Whiten/Scramble refers to the process of randomizing transmitted data to avoid any undesirable DC bias effects that might result from long strings of 1's or 0's in data packets. De-whiten/Unscramble is the reversal of the original process where the original data can be extracted.

4.3. Encrypt/Decrypt: Apply/Remove Encryption

Encryption is the security feature where keys are used to prevent unauthorized access to data. This functional block is responsible for the processing of authentication and essential management functions required for Bluetooth communications.

4.4. CRC: Cyclic Redundancy Check

This is the error detection function implemented to process the CRC field within the payload section of a Bluetooth transfer packet. On the receive side, the CRC is checked with the expected value based on Bluetooth specified algorithms. Prior to transmit, a proper CRC is generated and appended to the payload.

4.5. HEC: Header Error Correction

This is the error correction function for the 8-bit HEC field of the Bluetooth packet header as described in the Bluetooth specification 1.1.

4.6. Rx Buffers: Storage for Received Packets

The FIFO buffer is 384 bytes in length. This functional block contains the actual FIFO buffer and the associated control and management functions.

4.7. Tx Buffers: Storage for Packets to be Transmitted

The FIFO buffer for transmit packets is 384 bytes in length. This functional block contains the actual FIFO buffers and the associated control and management functions.

5. USB INTERFACE DESCRIPTION

The SiW1602 integrates a USB device controller and transceiver on-chip. This device controller will permit a host device to download HCI commands to the Bluetooth processor (typically a Hitachi H8 MPU) via the USB. The USB device controller has a memory-mapped peripheral interface to the MPU.

The controller complies with the Bluetooth HCI transport layer specifications. It is configured to support 6 endpoints. Each endpoint is mapped to one of 6 128x8-bit FIFOs as summarized in the following table.

Endpoint	Direction	Mapped FIFO
Control	Bi-directional	0
Bulk	In	1
Bulk	Out	2
Interrupt	In	3
Isochronous	In	4
Isochronous	Out	5

6. PIN DESCRIPTIONS

NOTE: All output pins are full CMOS drivers. There are no open drain drivers on the outputs.

6.1. Microprocessor Interface

The main interface to the microprocessor is an 8-bit data bus with a 10-bit address bus. This interface is designed to connect to standard microprocessors with common interface signals. Interrupt request lines provide sleep/wake control to the processor. To facilitate system power management, the SiW1602 controls the clock signal to the processor.

Name	Direction	Description
A0 to A9	I	10-bit parallel address from the microprocessor. For the Hitachi H8S/2238, connect to A0 to A9 on the H8.
D0 to D7	I/O	8-bit parallel data bus between the microprocessor and the SiW1602. Since only 8 bits are used, connect these pins to <D8 to D15> of the Hitachi H8 microprocessor. This signal is an input during reset.
/CS	I	Chip select or enable from the microprocessor for selecting the SiW1602's link controller memory map. This is an active low signal.
/USB_CS	I	Chip select or enable from the microprocessor for selecting the SiW1602's USB memory map. **NOTE:** /USB_CS and /CS are mutually exclusive. This is an active low signal.
/WR	I	Write signal from the microprocessor. This is an active low signal.
/RD	I	Read signal from the microprocessor. This is an active low signal.
/WAIT	O	Provides wait state control signal to the microprocessor. A low output tells the MPU to insert wait states into its memory access. The number of wait states is programmable. This is an active low signal. This signal outputs 1 when in reset.
/INT0	O	Interrupt request 0 to the processor. This is an active low signal. This signal outputs 1 when in reset.
/INT1	O	Interrupt request 1 to the processor. This is an active low signal. This signal outputs 1 when in reset.
WAKEUP	I	Asynchronous interrupt input that forces the SiW1602 to wake up when in sleep mode.
MCU_WAKEUP	O	Wake up signal to the microprocessor. This signal outputs 0 when in reset.
GPO1	O	Output reserved for future use.
GPO2	O	Output reserved for future use.

6.2. USB Interface

The SiW1602 contains a USB device controller and transceiver. Both run at either full-speed (12 Mbit/s) or low-speed (1.5 Mbit/s). The USB differential data signal (D+, D-) can be input directly to the chip. HCI data received by the USB controller is transferred to the microprocessor through the memory mapped interface defined above.

Name	Direction	Description
USB_D+	I/O	Positive USB differential data bus connection. This pin is not driven during reset. An external 1.5-kΩ pull-up resistor is required during full-speed operation. A series resistance is necessary to meet USB 1.1 specification compliance for the output impedance range.
USB_D-	I/O	Negative USB differential data bus connection. This pin is not driven during reset. An external 1.5-kΩ pull-up resistor is required during low-speed operation. A series resistance is necessary to meet USB 1.1 specification compliance for the output impedance range.
/USB_INT	O	USB interrupt request to the processor. This is an active low signal. This signal outputs 1 when in reset.

6.3. Radio Modem Interface

The SiW1602 interfaces to the SiW1502 Radio Modem for transmit/receive data and radio control. The SPI bus is used to access the internal control registers of the radio modem. Please refer to the SiW1502 Radio Modem IC Data Sheet for additional information on the modem interface.

Name	Direction	Description
MODEM_TX_DATA	O	Transmit data supplied to the SiW1502. This signal outputs 0 when in reset.
MODEM_RX/TX_DATA	I/O	A bi-directional data pin used to transfer data between the controller and the SiW1502. Direction is programmable, based on mode of interface. This signal is an input during reset.
MODEM_CD/TXEN	I/O	Dual function carrier detect (CD) input from the SiW1502 and transmit enable (TXEN) to the SiW1502. During transmit, this pin is used as an output to indicate valid transmit data. During receive, this pin is used as input to detect valid carrier. This signal is an input when in reset.
MODEM_RX_CLK	I	Receive data clock input from the SiW1502.
/SPI_SS	O	SPI slave select signal to the SiW1502 to select a device as the target of data transfer. This is an active low signal. This signal outputs 1 when in reset.
SPI_CLK	O	SPI clock signal. This signal outputs 0 when in reset.
SPI_TXD	O	SPI transmit data to the SiW1502. This signal outputs 0 when in reset.
SPI_RXD	I	SPI receive data from the SiW1502.
HOP_STRB	O	Hop strobe signals from the controller to indicate the start of a transmit or receive cycle. This signal outputs 0 when in reset.
ENABLE_RM	O	This is the enable signal for the SiW1502. This signal outputs 1 when in reset.
/RESET_OUT	O	Output signal used to reset the SiW1502. This is an active low signal. This signal outputs 0 when in reset.

6.4. Clock and Reset Signals

There are two clock inputs into the SiW1602. 32KHZ_CLK is used in the power-down mode to drive the minimal logic circuits to maintain the Bluetooth compliant clock. The 32-MHz clock used for the radio modem is also used to run the SiW1602. When the 32-MHz oscillator is disabled, the current draw is measured in microamperes (µA).

Name	Direction	Description
BB_CLK	I	Baseband main clock input.
32KHZ_CLK	I	32-kHz clock input. This input is typically from the SiW1502 32-kHz output.
MCU_CLK	O	Controlled clock to the microprocessor. This clock is generated from the 32-MHz crystal and is programmable. Typical output to the H8S/2238 is 10.667 MHz. Typical output to the H8S/2214 is 16 MHz. This signal outputs 1 when in reset.
BAUD_CLK	O	Clock output to microprocessor's serial interface clock logic for baud rate generation. This clock rate is derived from the 32-MHz clock and is programmable for various baud rates. This signal outputs 0 when in reset.
/PWR_RESET	I	Reset input signal to reset the SiW1602. Will cause /RESET_OUT to go active (low) and reset the SiW1502. /PWR_RESET and /MANUAL_RESET are joined internally through OR gates.
/MANUAL_RESET	I	Alternate reset input signal to reset the SiW1602. Will cause /RESET_OUT to go active (low) and reset the SiW1502. /PWR_RESET and /MANUAL_RESET are joined internally through OR gates.
/DISABLE	O	Power control signal used to indicate disable state. This signal outputs 1 when in reset.
LOWPWR_EN	O	Power control signal used to indicate low power state. This signal outputs 0 when in reset.

6.5. Power and Ground

Name	Direction	Description
VDD	I	3.0-V voltage supply for link controller. Nominal range is 2.7-to-3.3 V.
USB_VDD	I	3.0-V voltage supply for USB logic and transceiver. Nominal range is 3.0-to-3.3 V.
VSS	I	Ground input.
GND	I	Unused input. Connect to ground.

6.6. Test Interface

The SiW1602 includes a test interface that will allow test and debug of internal logic.

Name	Direction	Description
JTMS	I	JTAG test mode input.
JTCK	I	JTAG test clock.
JTDI	I	JTAG test data serial input.
JTDO	O	JTAG test data serial output.
/JTRST	I	JTAG test reset in.
NC	O	No connect.

7. PIN ASSIGNMENTS

The I/O signals pin assignments are detailed below but are preliminary and subject to change. Refer to the package drawing for correct orientation. This is the TOP view.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	A3	A4	A6	VSS	A8	NC	NC	NC	NC	VDD	NC	NC	NC	GND
B	A1													NC
C	VSS		A2	A7	VDD	NC	NC	NC	VSS	NC	NC	NC		MODEM_TX_DATA
D	BB_CLK		A0									MODEM_RX/TX_DATA		VDD
E	/PWR_RESET		VDD		A5	A9	NC	NC	GND	HOP_STRB		VSS		MODEM_CD/TXEN
F	D6		D7		WAKEUP					LOWPWR_EN		ENABLE_RM		MODEM_RX_CLK
G	VDD		D4		D5					VDD		MCU_WAKE		/DISABLE
H	D2		D3		VSS					SPI_TXD		SPI_RXD		VSS
J	D1		D0		/MANUAL_RESET					/USB_CS		/SPI_SS		SPI_CLK
K	32KHZ_CLK		VDD		/CS	NC	BAUD_CLK	/JTRST	/RESET_OUT	USB_VDD		VSS		/USB_INT
L	VSS		/WR									USB_GPO2		VDD
M	/RD		/INT1	NC	VDD	NC	VDD	JTCK	JTDO	VSS	USB_D+	NC		USB_GPO1
N	/WAIT													GND
P	/INT0	GND	VSS	NC	NC	MCU_CLK	VSS	JTMS	JTDI	VSS	USB_D-	USB_VDD	NC	VSS

8. SIW1602 SPECIFICATIONS

Always turn off power before adding or removing devices from test and/or systems.

8.1. ESD Precautions

These devices are electrostatic sensitive. Devices should by handled in accordance with MIL-STD-1686. Devices should be transported and stored in anti-static containers. Ensure that equipment and personnel contacting the devices are properly grounded. Cover workbenches with grounded conductive mats.

8.2. Absolute Maximum Ratings

Parameter	Description	Min	Max	Units
T_{ST}	Storage temperature	-55	+125	°C
V_{ddmax}	Supply voltage	-0.3	4.0	V
I_{in}	Input current	-10	10	mA
ESD	ESD protection (human body model)	–	2000	V
Tj	Junction temperature	–	125	°C

8.3. Recommended Operating Conditions

Parameter	Description	Min	Max	Units
T_{OP}	Operating temperature	-40	+85	°C
V_{dd}	DC supply voltage (USB operation)	3.0	3.3	V
V_{dd}	DC supply voltage (UART operation)	2.7	3.3	V

8.4. DC Parameters (T_{op} = -40 to 85°C; V_{DD} = 3.0 V)

Parameter	Description	Min	Max	Units
V_{IL1}	Input low voltage, normal input pins	GND - 0.1	$0.3 \cdot V_{DD}$	V
V_{IH1}	Input high voltage, normal input pins	$0.7 \cdot V_{DD}$	V_{DD}	V
V_{IL2}	Input low voltage, D0 to D7, 32KHZ_CLK, BB_CLK, MODEM_CD/TXEN, MODEM_RX/TX_DATA, (Schmitt-trigger input, hysteresis = 0.8 V_{DD})	GND - 0.1	$0.2 \cdot V_{DD}$	V
V_{IH2}	Input high voltage, D0 to D7, 32KHZ_CLK, BB_CLK, MODEM_CD/TXEN, MODEM_RX/TX_DATA (Schmitt-trigger input, hysteresis = 0.8 V_{DD})	$0.8 \cdot V_{DD}$	V_{DD}	V
V_{OL}	Output low voltage, normal output and bi-directional pins	GND	0.4	V
V_{OH}	Output high voltage, normal output and bi-directional pins	$0.8 \cdot V_{DD}$	V_{DD}	V
I_{OH}	Output high current	–	-3.9	mA
I_{OL}	Output low current	–	3.9	mA
I_{LI}	Input leakage current, high-impedance state	–	10	µA
I_{LO}	Output leakage current, high-impedance state	–	10	µA

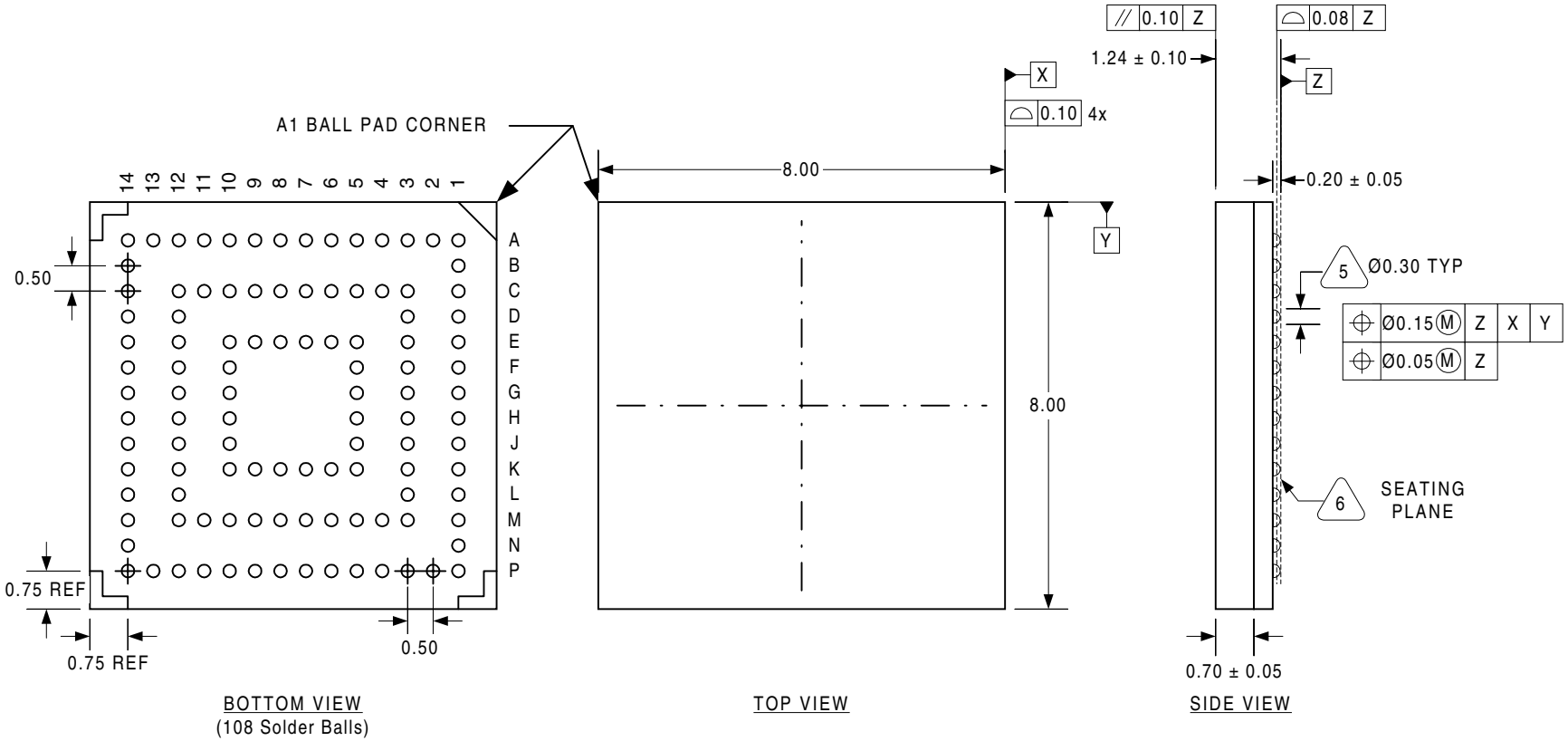
8.5. Current Consumption

Parameter	Description	Typical	Units
I_{DD} (standby)	Current draw in standby mode (USB not included)	TBD	mA
I_{DD} (idle)	Current draw in active mode (USB not included)	8.0	mA
I_{DD} (USB)	Current draw for USB controller and transceiver	8.0	mA

9. PACKAGING

The packaging diagram for the BGA package follows. Information on the flip chip package is available from Silicon Wave, Inc. upon request.

9.1. SiW1602 package: 108 fine-pitch BGA, 8-mm x 8-mm body, 0.5-mm pitch



10. SOLDERING DATA

To be provided.

11. ORDERING INFORMATION

To be provided.

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