

HD74HC597

8-bit Latch/Shift Register

HITACHI

ADE-205-515 (Z)
1st. Edition
Sep. 2000




Description

The HD74HC597 consists of an 8-bit storage latch feeding a parallel-in, serial-out 8-bit shift register. Both the storage register and shift register have positive-edge triggered clocks. The shift register also has direct load (from storage) and clear inputs.

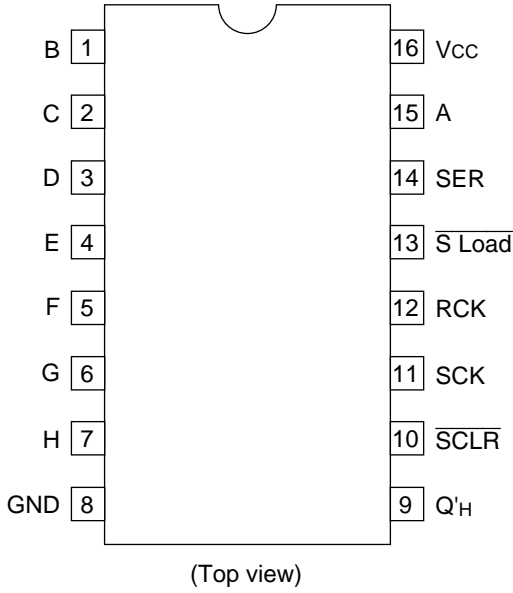
Features

- High Speed Operation: t_{pd} (SCK to Q_H') = 14 ns typ ($C_L = 50$ pF)
- High Output Current: Fanout of 10 LSTTL Loads
- Wide Operating Voltage: $V_{CC} = 2$ to 6 V
- Low Input Current: 1 μ A max
- Low Quiescent Supply Current: I_{CC} (static) = 4 μ A max ($T_a = 25^\circ\text{C}$)

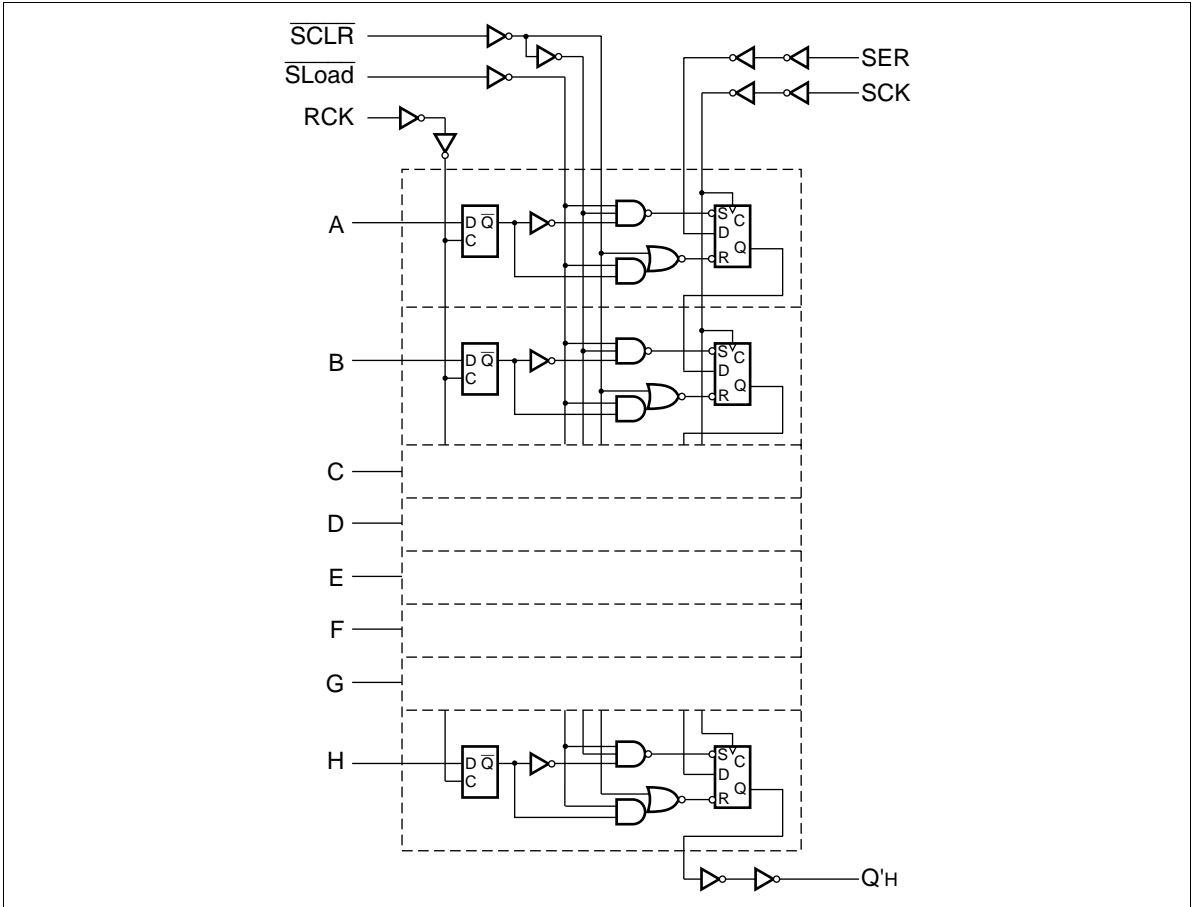
Function Table

RCK	SCK	$\overline{\text{SLoad}}$	$\overline{\text{SCLR}}$	Function
	X	X	X	Data loaded to input latches
	X	L	H	Data loaded from inputs to shift register
X	X	L	H	Data transferred from input latches to shift register
X	X	L	L	Invalid logic, state of shift register indeterminate when signals removed
X	X	H	L	Shift register cleared
X		H	H	Shift register clocked $Q_n = Q_{n-1}$, $Q_A = \text{SER}$

Pin Arrangement



Logic Diagram



DC Characteristics

Item	Symbol	V _{CC} (V)	Ta = 25°C			Ta = -40 to +85°C		Unit	Test Conditions	
			Min	Typ	Max	Min	Max			
Input voltage	V _{IH}	2.0	1.5	—	—	1.5	—	V		
		4.5	3.15	—	—	3.15	—			
		6.0	4.2	—	—	4.2	—			
	V _{IL}	2.0	—	—	0.5	—	0.5	V		
		4.5	—	—	1.35	—	1.35			
		6.0	—	—	1.8	—	1.8			
Output voltage	V _{OH}	2.0	1.9	2.0	—	1.9	—	V	Vin = V _{IH} or V _{IL} I _{OH} = -20 μA	
		4.5	4.4	4.5	—	4.4	—			
		6.0	5.9	6.0	—	5.9	—			
		4.5	4.18	—	—	4.13	—			I _{OH} = -4 mA
		6.0	5.68	—	—	5.63	—			I _{OH} = -5.2 mA
	V _{OL}	2.0	—	0.0	0.1	—	0.1	V	Vin = V _{IH} or V _{IL} I _{OL} = 20 μA	
		4.5	—	0.0	0.1	—	0.1			
		6.0	—	0.0	0.1	—	0.1			
		4.5	—	—	0.26	—	0.33			I _{OL} = 4 mA
		6.0	—	—	0.26	—	0.33			I _{OL} = 5.2 mA
Input current	I _{in}	6.0	—	—	±0.1	—	±1.0	μA	Vin = V _{CC} or GND	
Quiescent supply current	I _{CC}	6.0	—	—	4.0	—	40	μA	Vin = V _{CC} or GND, I _{out} = 0 μA	

AC Characteristics ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

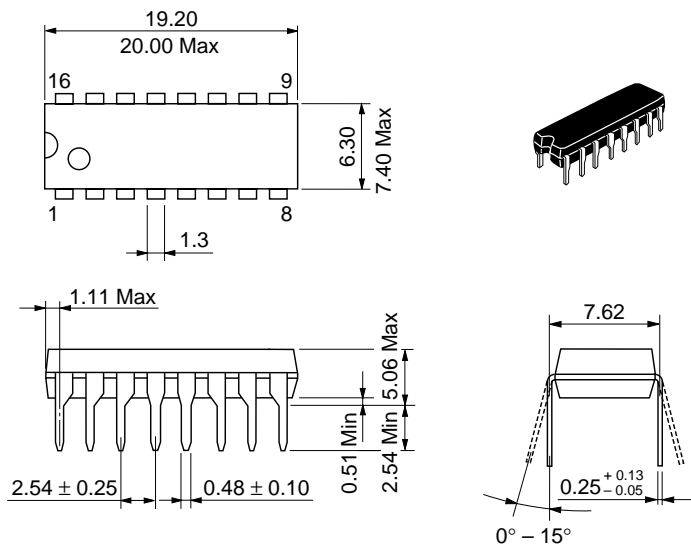
Item	Symbol	V_{CC} (V)	$T_a = 25^\circ\text{C}$			$T_a = -40$ to $+85^\circ\text{C}$		Unit	Test Conditions		
			Min	Typ	Max	Min	Max				
Maximum clock frequency	f_{max}	2.0	—	—	5	—	4	MHz			
		4.5	—	—	27	—	21				
		6.0	—	—	31	—	24				
Propagation delay time	t_{PLH}	2.0	—	—	175	—	220	ns	SCK or $\overline{\text{SLoad}}$ or $\overline{\text{SCLR}}$ to Q_H'		
		4.5	—	14	35	—	44				
		6.0	—	—	30	—	37				
	t_{PHL}	2.0	—	—	210	—	265	ns	RCK to Q_H'		
		4.5	—	17	42	—	53				
		6.0	—	—	36	—	45				
Removal time	t_{rem}	2.0	100	—	—	125	—	ns			
		4.5	20	—	—	25	—				
		6.0	17	—	—	21	—				
Setup time	t_{su}	2.0	100	—	—	125	—	ns	RCK to SCK		
		4.5	20	—	—	25	—				
		6.0	17	—	—	21	—				
		2.0	100	—	—	125	—	ns		SER to SCK	
		4.5	20	1	—	25	—				
		6.0	17	—	—	21	—				
	2.0	100	—	—	125	—	ns	Data to RCK			
	4.5	20	0	—	25	—					
	6.0	17	—	—	21	—					
	Hold time	t_h	2.0	5	—	—	5		—	ns	SCK to S_A
			4.5	5	—	—	5		—		
			6.0	5	—	—	5		—		
2.0			5	—	—	5	—	ns	LCK to Data		
4.5			5	—	—	5	—				
6.0			5	—	—	5	—				
Pulse width	t_w	2.0	80	—	—	100	—	ns			
		4.5	16	7	—	20	—				
		6.0	14	—	—	17	—				

AC Characteristics ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns) (cont)

Item	Symbol	V_{CC} (V)	$T_a = 25^\circ\text{C}$			$T_a = -40$ to $+85^\circ\text{C}$		Unit	Test Conditions
			Min	Typ	Max	Min	Max		
Output rise/fall time	t_{TLH}	2.0	—	—	75	—	95	ns	
		4.5	—	4	15	—	19		
		6.0	—	—	13	—	16		
Input capacitance	C_{in}	—	—	5	10	—	10	pF	

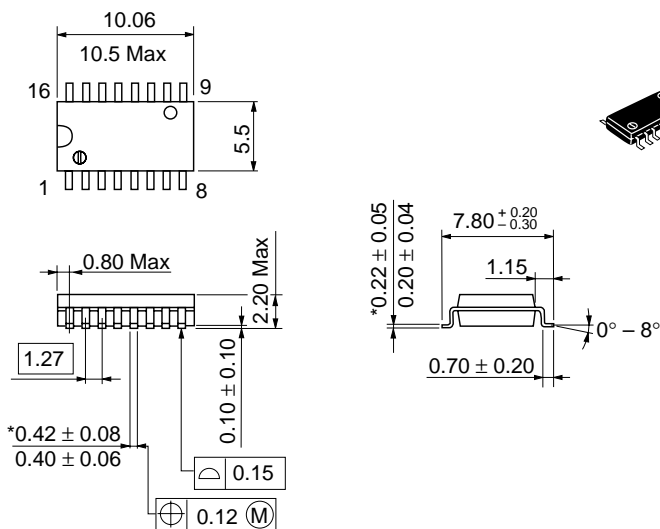
Package Dimensions

Unit: mm



Hitachi Code	DP-16
JEDEC	Conforms
EIAJ	Conforms
Mass (reference value)	1.07 g

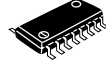
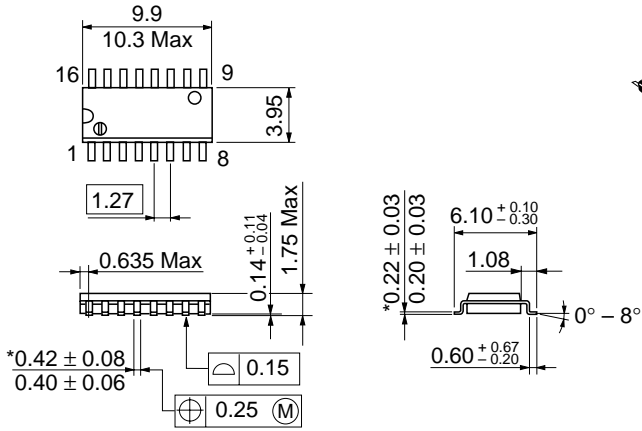
Unit: mm



*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-16DA
JEDEC	—
EIAJ	Conforms
Mass (reference value)	0.24 g

Unit: mm



*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-16DN
JEDEC	Conforms
EIAJ	Conforms
Mass (reference value)	0.15 g

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