3.3V FAST CMOS REGISTERED ADDRESS LINE DRIVER

IDT74FCT16V345

FEATURES:

- 0.5 MICRON CMOS Technology
- Typical $t_{SK(o)}$ (Output Skew) < 250ps
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- 25 mil pitch SSOP, 19.6 mil pitch TSSOP and 15.7 mil pitch TVSOP Packages
- Extended commercial range of -40°C to +85°C
- V_{CC} = 3.3V ±0.3V, Normal Range or
  V_{CC} = 2.7 to 3.6V, Extended Range
  V_{CC} = 2.5V ±0.2V
- CMOS power levels (0.4µW typ. static)
- Rail-to-Rail output swing for increased noise margin

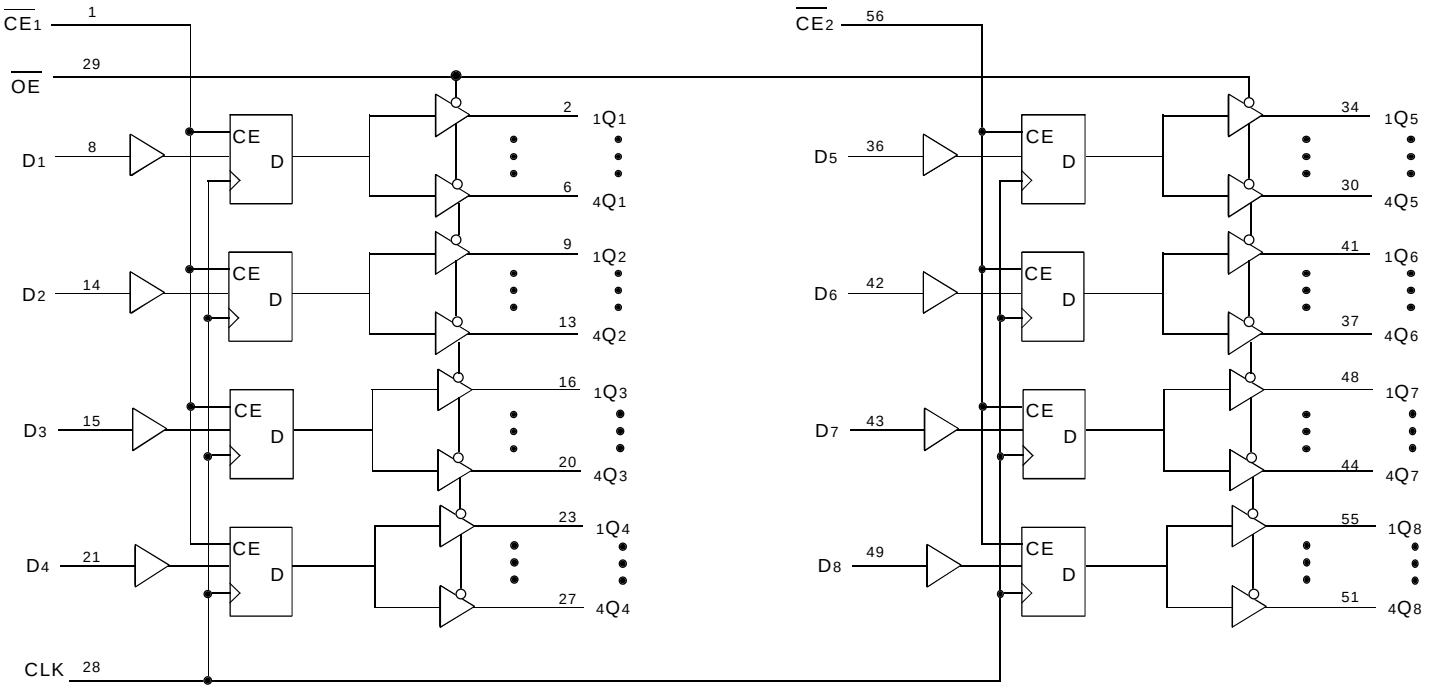
DESCRIPTION:

The FCT16V345 is a registered address driver built using advanced dual metal CMOS technology. The device is configured with fan out of four for use in high speed synchronous memory applications.

The FCT16V345 is ideal for driving memory modules in systems where multiple memory modules are used. If each of the four output banks drives a different module, modules can be added or removed without affecting the signal integrity of the other modules in the system.

Dual Clock Enables ($\overline{CE}x$) allow use of the FCT16V345 in high speed memory interleaving applications where the clock can be alternately enabled and disabled, allowing the address to be held for additional clock cycles during memory access.

FUNCTIONAL BLOCK DIAGRAM



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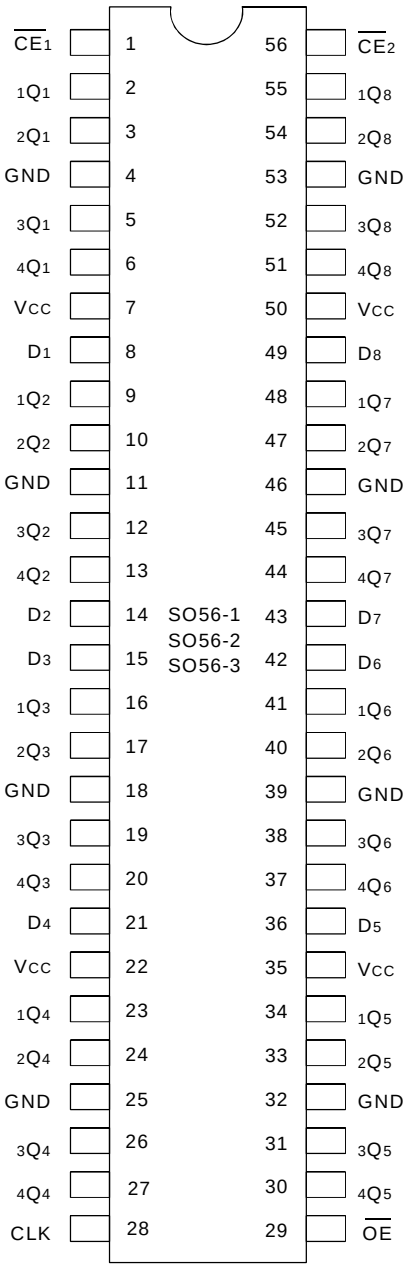
PIN CONFIGURATION



SSOP/ TSSOP/ TVSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Description	Max	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +4.6	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to V_{CC}+0.5	V
T_{STG}	Storage Temperature	–65 to +150	°C
I_{OUT}	DC Output Current	–60 to +60	mA

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Non bus-hold input terminals and Vcc terminals.
3. Output, I/O terminals, and bus-hold input terminals.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	3.5	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	3.5	8	pF

3v16-link

NOTE:
1. This parameter is measured at characterization but not tested.

PIN DESCRIPTION

Pin Names	Description
$\overline{OE}$	3-State Output Enable Input (Active LOW)
Dx	Inputs
xQx	3-State Outputs
CLK	Clock Input
$\overline{CE}$x	Clock Enable (Active LOW)

FUNCTION TABLE(1)

Inputs				Outputs
$\overline{CE}$x	CLK	$\overline{OE}$	Dx	xQx
H	X	L	X	B(2)
X	L	L	X	B(2)
L	↑	L	L	L
L	↑	L	H	H
X	X	H	X	Z

NOTES:
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   ↑ = LOW-to-HIGH Transition
   Z = High-Impedance
2. Output level before indicated steady-state input conditions were established.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Operating Condition: T_A = –40°C to +85°C

Symbol	Parameter	Test Conditions		Min.	Typ.(1)	Max.	Unit
V_{IH}	Input HIGH Voltage Level	V_{CC} = 2.3V to 2.7V		1.7	—	3.6	V
		V_{CC} = 2.7V to 3.6V		2	—	3.6	
V_{IL}	Input LOW Voltage Level	V_{CC} = 2.3V to 2.7V		– 0.5	—	0.7	V
		V_{CC} = 2.7V to 3.6V		– 0.5	—	0.8	
I_{IH}	Input HIGH Current	V_{CC} = 3.6V	V_I = V_{CC}	—	—	±1	µA
I_{IL}	Input LOW Current	V_{CC} = 3.6V	V_I = GND	—	—	±1	
I_{OZH}	High Impedance Output Current	V_{CC} = 3.6V	V_O = V_{CC}	—	—	±1	µA
I_{OZL}	(3-State Output pins)		V_O = GND	—	—	±1	
V_{IK}	Clamp Diode Voltage	V_{CC} = 2.3V, I_{IN} = – 18mA		—	– 0.7	– 1.2	V
V_H	Input Hysteresis	—		—	100	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	V_{CC} = 3.6V V_{IN} = GND or V_{CC}		—	0.1	10	µA

NOTE:
1. Typical values are at V_{CC} = 3.3V, +25°C ambient.

OUTPUT DRIVE CHARACTERISTICS

Following Conditions Apply Unless Otherwise Specified:
Operating Condition: T_A = –40°C to +85°C

Symbol	Parameter	Test Conditions(1)		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = 2.3V	I_{OH} = 0.1mA	V_{CC} – 0.2	—	V
			I_{OH} = – 6mA	2	—	
		V_{CC} = 2.3V	I_{OH} = – 12mA	1.7	—	
		V_{CC} = 2.7V		2.2	—	
		V_{CC} = 3V		2.4	—	
		V_{CC} = 3V	I_{OH} = – 24mA	2.2	—	
V_{OL}	Output LOW Voltage	V_{CC} = 2.3V	I_{OL} = 0.1mA	—	0.2	V
			I_{OL} = 6mA	—	0.4	
			I_{OL} = 12mA	—	0.7	
		V_{CC} = 2.7V	I_{OL} = 12mA	—	0.4	
		V_{CC} = 3V	I_{OL} = 24mA	—	0.55	

NOTE:
1. V_{IH} and V_{IL} must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate V_{CC} range.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = V_{CC} –0.6V[3]		—	2	3	µA
I_{CCD1}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{OE}$ = GND One Clock Input Bit Toggling No Output Bits Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	37	50	µA/ MHz
I_{CCD2}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{OE}$ = GND One Input Bit Toggling Four Output Bits Toggling One Clock Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	252	300	µA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open fcp= 10MHz 50% Duty Cycle $\overline{OE}$ = $\overline{CE}$x = GND At fi= 5MHz 50% Duty Cycle One Input Bit Toggling Four Output Bits Toggling One Clock Input Toggling	V_{IN} = V_{CC} V_{IN} = GND	—	1.63	2.01	mA
			V_{IN} = V_{CC} –0.6V V_{IN} = GND	—	1.63	2.04	
		V_{CC} = Max. Outputs Open fcp = 10MHz 50% Duty Cycle $\overline{OE}$ = $\overline{CE}$x = GND At fi= 2.5MHz 50% Duty Cycle Eight Input Bits Toggling Thirty Two Output Bits Toggling One Clock Input Toggling	V_{IN} = V_{CC} V_{IN} = GND	—	5.41	6.51	
			V_{IN} = V_{CC} –0.6V V_{IN} = GND	—	5.42	6.65	

NOTES:
1. V_{CC} (max.) = 3.6V
2. Typical values are at V_{CC} = 3.3V, +25°C ambient.
3. Per TTL driven input; all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current (I_{CCL}, I_{CCH} and I_{CCZ})
   ΔI_{CC} = Power Supply Current for a TTL High Input
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   N_{CP} = Number of Clock Inputs at f_{CP}
   f_i = Input Frequency
   N_i = Number of Inputs at fi

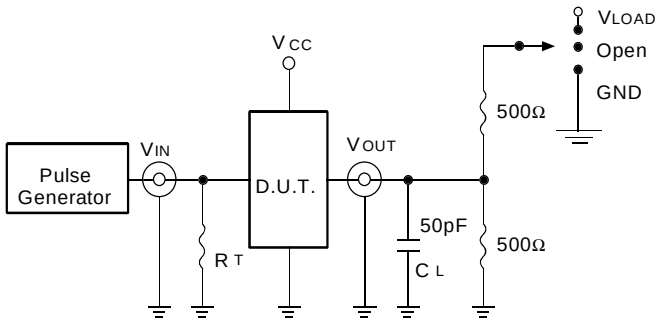
SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition[1]	Vcc = 2.5V±0.2V		Vcc = 2.7V		Vcc = 3.3V±0.3V		Unit
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
t_{PLH} t_{PHL}	Propagation Delay CLK to xQx	C_L = 50pF R_L = 500Ω	1.5	7	1.5	6	1.5	5.5	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to xQx		1.5	7.7	1.5	6.9	1.5	6	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ to xQx		1.5	6.2	1.5	5.2	1.5	4.9	ns
t_{SU}	Set-Up Time HIGH or LOW $\overline{CE}$x to CLK		2	—	2	—	1.2	—	ns
t_H	Hold Time HIGH or LOW $\overline{CE}$x to CLK		0	—	0	—	0	—	ns
t_{SU}	Set-Up Time HIGH or LOW Dx to CLK		2	—	2	—	0.8	—	ns
t_H	Hold Time HIGH or LOW CLK to Dx		0	—	0	—	0	—	ns
t_W	CLK Pulse Width HIGH or LOW[5]		3	—	3	—	3	—	ns
$t_{SK(o)}$	Output Skew[3]		—	500	—	500	—	500	ps
$t_{SK(b)}$	Bank Skew[4]		—	350	—	350	—	350	ps

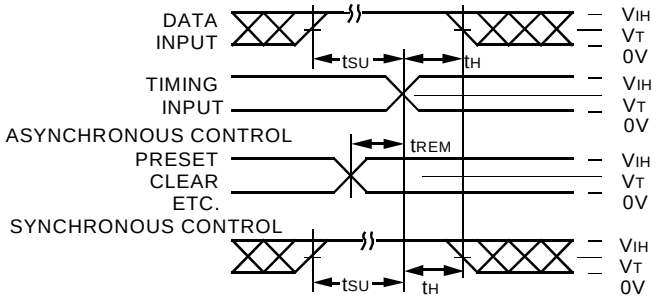
NOTES:
1. See test circuits and waveforms.
2. Minimum limits are guaranteed but not tested on propagation delays.
3. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.
4. Skew between any two outputs with a common input signal. This parameter is guaranteed by design.
5. This parameter is guaranteed but not tested.

TEST CIRCUITS AND WAVEFORMS

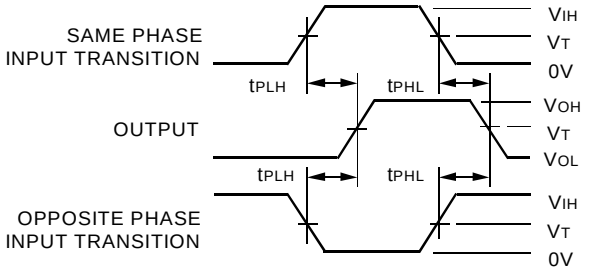
TEST CIRCUITS FOR ALL OUTPUTS



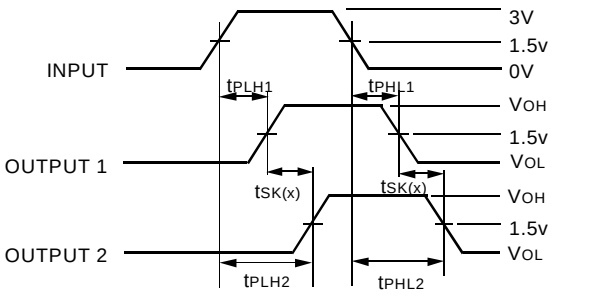
SET-UP, HOLD, AND RELEASE TIMES



PROPAGATION DELAY



OUTPUT SKEW - tSK (x)



$t_{SK(x)} = |t_{PLH2} - t_{PLH1}|$ or $|t_{PHL2} - t_{PLH1}|$

NOTES:
1. For tsk(b) OUTPUT1 and OUTPUT2 are in the same bank.
2. For tsk(o) OUTPUT1 and OUTPUT2 are in different banks on the same part.

SWITCH POSITION

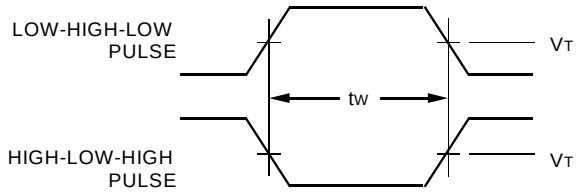
Test	Switch
Disable Low Enable Low	VLOAD
Disable High Enable High	GND
All Other Tests	Open

DEFINITIONS:
C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

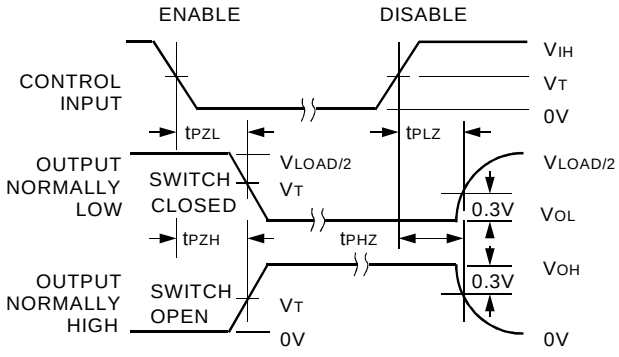
TEST VOLTAGES

Symbol	Vcc=3.3V±0.3V	Vcc=2.7V	Vcc=2.7V±0.2V	Unit
VLOAD	6	6	4.6	V
VIH	2.7	2.7	2.3	V
VT	1.5	1.5	1.2	V

PULSE WIDTH

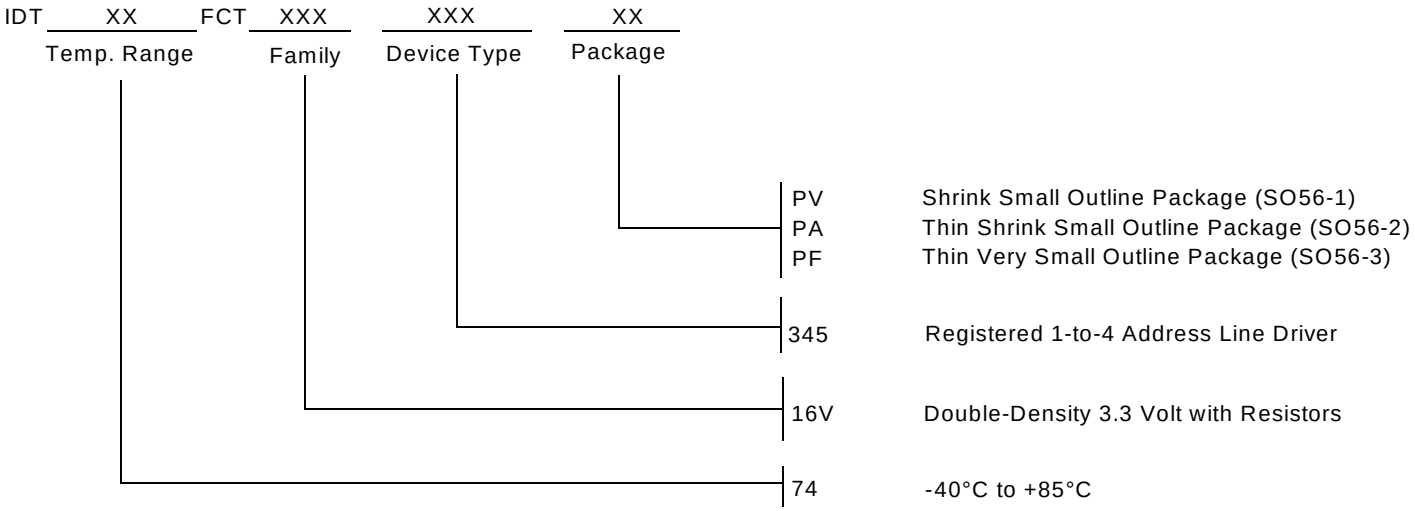


ENABLE AND DISABLE TIMES



NOTES:
1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns.

ORDERING INFORMATION



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