HD74HCT74A

Dual D–type Positive Edge–triggered Flip Flops with Clear and Preset

HITACHI

ADE-205-290 (Z)
1st. Edition
Jun. 1999

Description

The HD74HCT74A has independent data, preset, clear, and clock inputs Q and $\overline{Q}$ outputs in a 14 pin package. The logic level present at the data input is transferred to the output during the positive going transition of the clock pulse. Preset and clear are independent of the clock and accomplished by a low level at the appropriate input.

Features

- V_{CC} = 4.5 to 5.5 V operation
- Input terminal has protection diode

Function Table

Inputs				Outputs	
$\overline{PRE}$	$\overline{CLR}$	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H [*1]	H [*1]
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

H : High level

L : Low level

X : Immaterial

↑ : Low to high transition

Q_0 : Level to Q before the indicated steady state input conditions were established.

Note : 1. Q and $\overline{Q}$ will remain high as long as preset and clear are low, but Q and $\overline{Q}$ are unpredictable, if preset and clear go high simultaneously.

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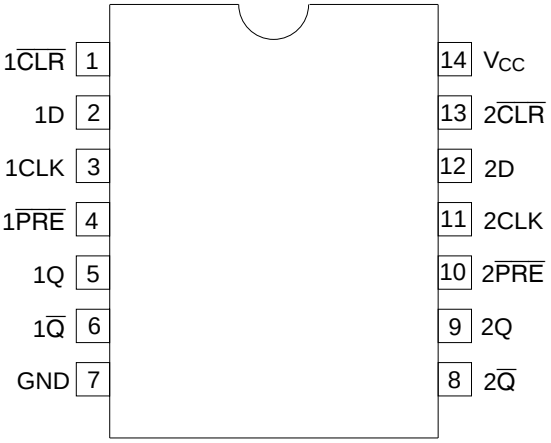
Pin Arrangement



(Top view)

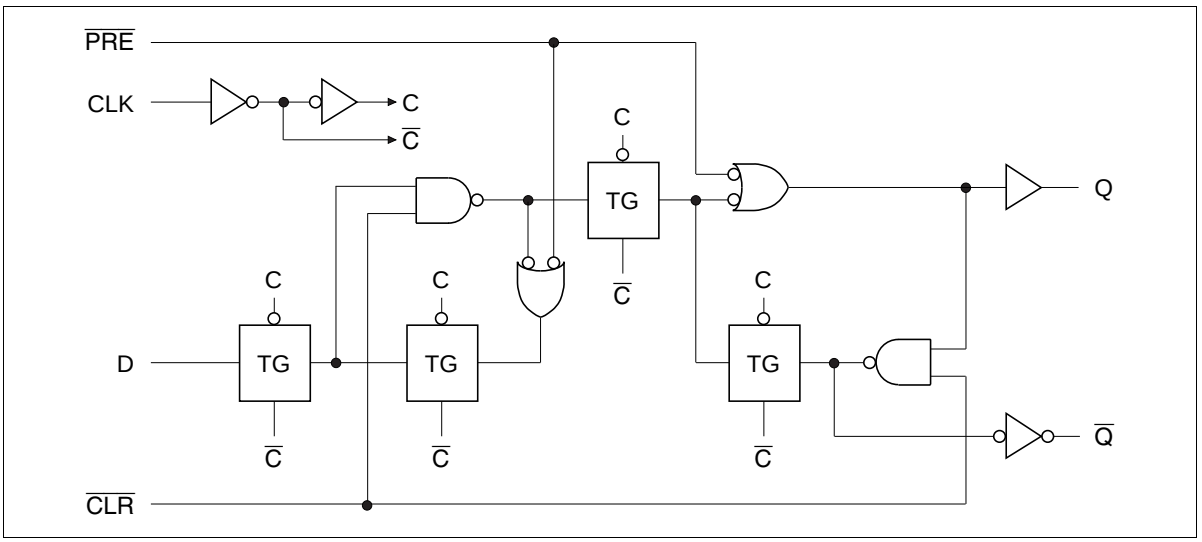
Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply voltage	V_{CC}	–0.5 to 7.0	V
Input diode peak current	I_{IK}	±20	mA
Output diode peak current	I_{OK}	±20	mA
Output current	I_O	±25	mA
V_{CC}, GND current / pin	I_{CC} or I_{GND}	±50	mA
Storage temperature	Tstg	–65 to 150	°C

Recommended Operating Conditions

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage	V_{IH}	2.0	—	—	V
	V_{IL}	0	—	0.8	
	V_I	0	—	V_{CC}	
Output voltage	V_O	0	—	V_{CC}	V
Output current	I_{OH}	—	–4	—	mA
	I_{OL}	—	4	—	
Input rise / fall time	t_r, t_f	—	—	500	ns
Operating temperature	Ta	–40	—	85	°C

Logic Diagram



Electrical Characteristics

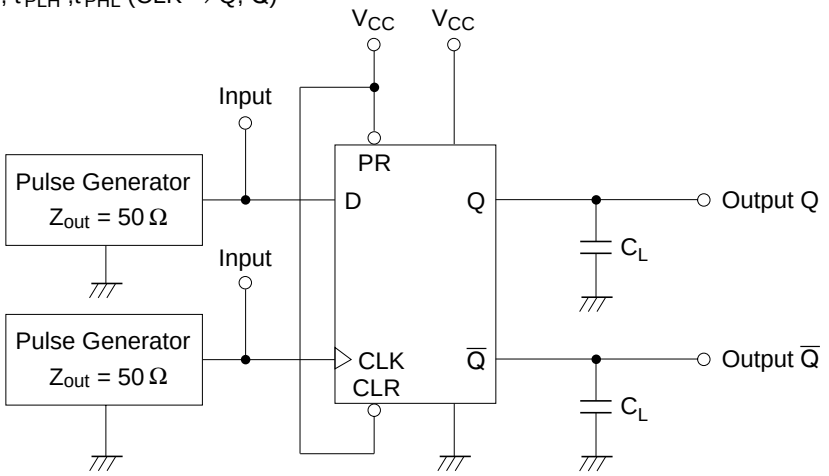
Item	Symbol	V_{cc} (V)	Ta = 25°C			Ta = –40 to 85°C		Unit	Test Conditions
			Min	Typ	Max	Min	Max		
Output voltage	V_{OH}	4.5	4.40	—	—	4.40	—	V	I_O = –20 µA
		4.5	3.98	—	—	3.84	—		I_O = –4 mA
	V_{OL}	4.5	—	—	0.10	—	0.10		I_O = 20 µA
		4.5	—	—	0.26	—	0.33		I_O = 4 mA
Input current	I_I	5.5	—	±0.1	±100	—	±1000	nA	V_I = V_{CC} or GND
Quiescent supply voltage	I_{CC}	5.5	—	—	4.0	—	40	µA	V_I = V_{CC} or GND, I_O = 0

Switching Characteristics (C_L = 50 pF)

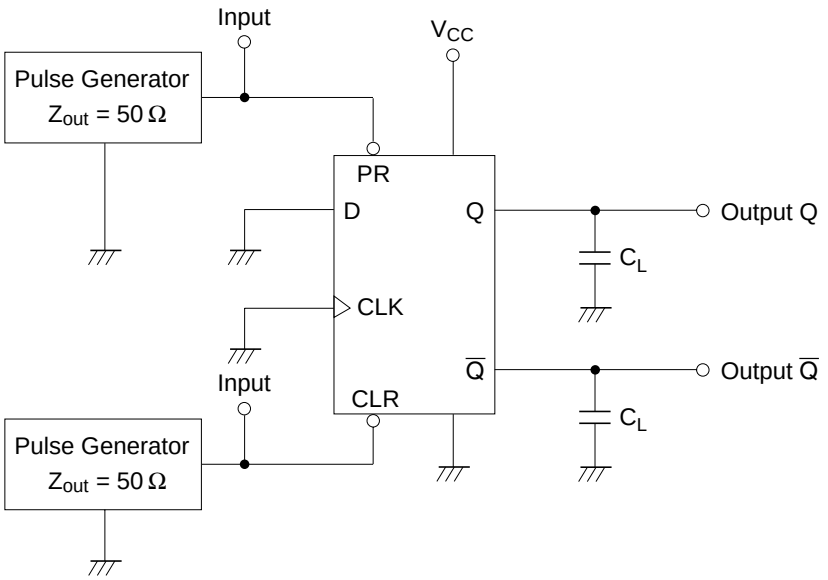
Item	Symbol	V_{cc} (V)	Ta = 25°C			Ta = –40 to 85°C		Unit	Input	Output
			Min	Typ	Max	Min	Max		FROM	TO
Maximum clock frequency	f_{max}	4.5	27	78	—	22	—	MHz		
		5.5	30	92	—	24	—			
Propagation delay time	t_{PLH}	4.5	—	14	28	—	35	ns	$\overline{PRE}$,	Q, $\overline{Q}$
	t_{PHL}	5.5	—	12	25	—	32		$\overline{CLR}$	
		4.5	—	14	22	—	28		CLK	Q, $\overline{Q}$
		5.5	—	13	20	—	25			
Output rise / fall time	t_r / t_f	4.5	—	7	15	—	19	ns		Each
		5.5	—	6	13	—	16			output
Setup time	t_{su}	4.5	10	—	—	13	—	ns	D	
		5.5	9	—	—	12	—			
		4.5	5	—	—	5	—		$\overline{PRE}$, $\overline{CLR}$	
		5.5	5	—	—	5	—		inactive	
Hold time	t_h	4.5	0	—	—	0	—	ns		
		5.5	0	—	—	0	—			
Pulse width	t_w	4.5	15	—	—	19	—	ns		
		5.5	14	—	—	17	—			
Input capacitance	C_I	—	—	3	10	—	10	pF		
Power dissipation capacitance	C_{PD}	—	—	35	—	—	—	pF		

Test Circuit

1) f_{max}, t_{PLH}, t_{PHL} (CLK → Q, $\overline{Q}$)

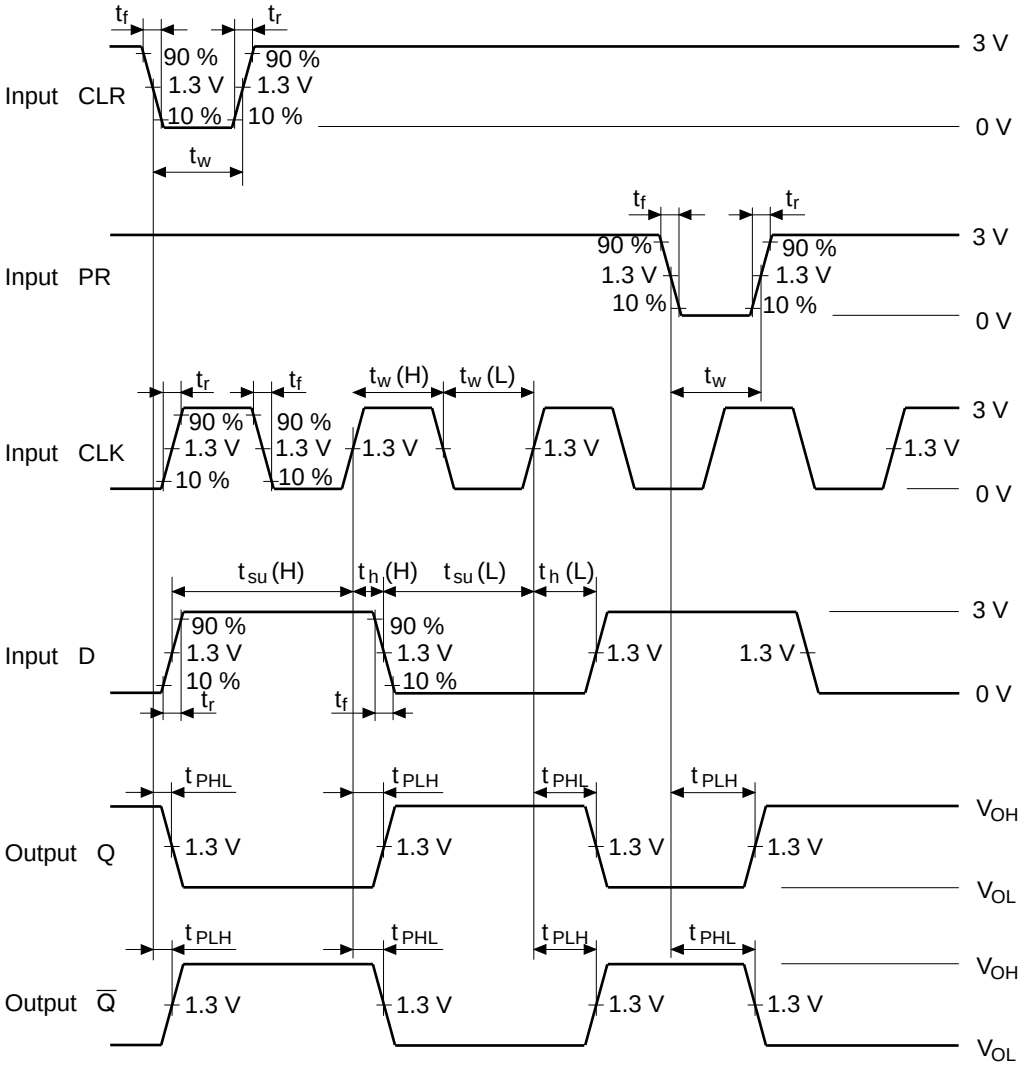


2) t_{PLH}, t_{PHL} (CLR or PR → Q, $\overline{Q}$)



Notes: 1. C_L includes probe and jig capacitance.
2. Test is put into the each flip flops.

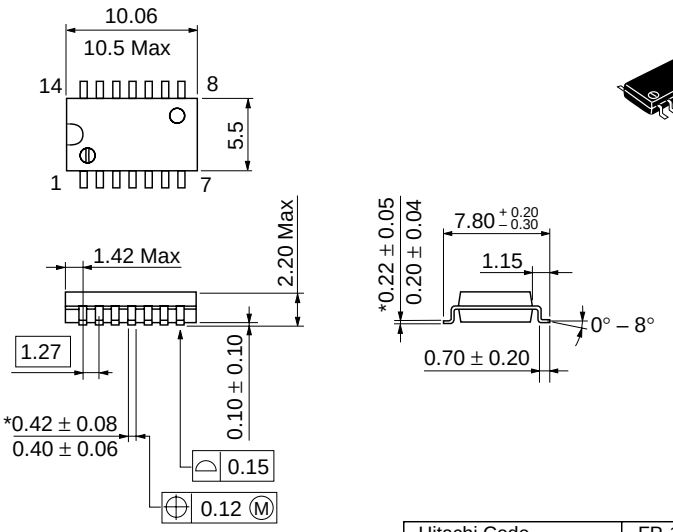
• **Waveform**



Note: 1. Input waveform : PRR = 1 MHz, duty cycle 50%, t_r = 6 ns, t_f = 6 ns

Package Dimensions

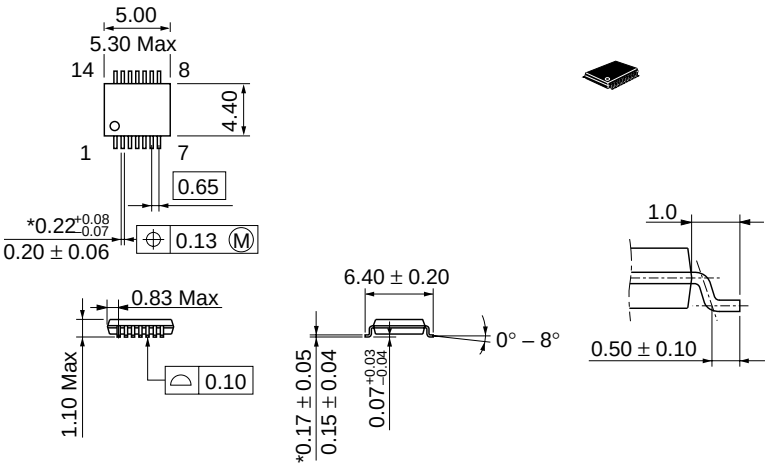
Unit: mm



*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-14DA
JEDEC	—
EIAJ	Conforms
Mass (reference value)	0.23 g

Unit: mm



*Dimension including the plating thickness
Base material dimension

Hitachi Code	TTP-14D
JEDEC	—
EIAJ	—
Mass (reference value)	0.05 g

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