INTEGRATED CIRCUITS

DATA SHEET

TDA9880

Alignment-free multistandard vision and FM sound IF-PLL demodulator

Preliminary specification Supersedes data of 1998 Apr 16 File under Integrated Circuits, IC02 1998 Aug 12





TDA9880

FEATURES

- 5 V supply voltage
- Gain controlled wide-band Vision Intermediate Frequency (VIF) amplifier (AC-coupled)
- True synchronous demodulation with active carrier regeneration (very linear demodulation, good intermodulation figures, reduced harmonics, excellent pulse response)
- Fully integrated VIF Voltage Controlled Oscillator (VCO), alignment-free
- Digital acquisition help, VIF frequencies of 38.0, 38.9, 45.75 and 58.75 MHz
- 4 MHz reference frequency input [signal from Phase-Locked Loop (PLL) tuning system] or operating as crystal oscillator
- VIF Automatic Gain Control (AGC) detector for gain control, operating as peak sync detector, fast reaction time

- Precise fully digital Automatic Frequency Control (AFC) detector with 4-bit digital-to-analog converter
- Fully integrated sound carrier trap for 4.5, 5.5, 6.0 and 6.5 MHz, controlled by reference signal
- Alignment-free selective FM-PLL demodulator with high linearity and low noise
- Digital frequency control, sound carrier frequencies 4.5, 5.5, 6.0 and 6.5 MHz
- Stabilizer circuit for ripple rejection and to achieve constant output signals
- Electrostatic discharge (ESD) protection for all pins.

GENERAL DESCRIPTION

The TDA9880 is an integrated circuit for multistandard vision IF signal processing and FM demodulation in TV and VTR sets.

ORDERING INFORMATION

TYPE NUMBER		PACKAGE				
TIPE NOWBER	NAME	DESCRIPTION	VERSION			
TDA9880	SDIP20	plastic shrink dual in-line package; 20 leads (300 mil)	SOT325-1			
TDA9880T	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1			

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QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage	note 1	4.5	5	5.5	V
l _P	supply current		85	100	115	mA
$V_{i(VIF)(rms)}$	VIF input signal voltage sensitivity (RMS value)	-1 dB video at output	-	50	100	μV
G _{VIF(cr)}	VIF gain control range	see Fig.4	65	69	_	dB
f_{VIF}	vision carrier operating frequencies	see Table 2	_	38.0	_	MHz
			_	38.9	_	MHz
			_	45.75	_	MHz
			_	58.75	_	MHz
Δf_{VIF}	VIF frequency window of digital acquisition help	referenced to f _{VIF}	-	±2.38	_	MHz
$V_{o(v)(p-p)}$	video output signal voltage	normal mode; see Fig.10	1.7	2.0	2.3	V
	(peak-to-peak value)	trap bypass mode; see Fig.10	0.95	1.10	1.25	V
G _{dif}	differential gain	"NTC-7 Composite"	1-	2	5	%
Φdif	differential phase	"NTC-7 Composite"	Ī-	2	4	deg
B _{v(-3dB)(trap)}	-3 dB video bandwidth including sound carrier trap	C_L < 20 pF; R_L > 1 k Ω ; AC load; note 2				
		f _{trap} = 4.5 MHz (M/N standard)	3.95	4.05	_	MHz
		f _{trap} = 5.5 MHz (B/G standard)	4.90	5.00	-	MHz
α_{SC1}	trap attenuation at first sound carrier	M/N standard	30	36	_	dB
		B/G standard	30	36	_	dB
S/N _W	weighted signal-to-noise ratio of video signal	see Fig.6; note 3	56	60	_	dB
PSRR ₁₃	power supply ripple rejection at pin 13	f _{ripple} = 70 Hz; video signal; grey level; see Fig.9	25	28	-	dB
B _{v(-1dB)}	-1 dB video bandwidth	$C_L < 20 \text{ pF}; R_L > 1 \text{ k}\Omega;$ AC load; trap bypass mode	5	6	_	MHz
I _{ch(max)(20)}	AGC maximum charge current at pin 20		6	8	10	μА
I _{dch(max)(20)}	AGC maximum discharge current at pin 20		7.5	10	12.5	μΑ
I _{sink(14)}	sink current of tuner AGC at pin 14	maximum tuner gain reduction; V ₁₄ = 1 V; see Fig.4	450	600	750	μΑ
AFC _{stps}	AFC steepness ΔI ₁₉ /Δf		0.85	1.05	1.25	μΑ/kHz
I _{o(source)(19)}	AFC output source current at pin 19		160	200	240	μΑ
I _{o(sink)(19)}	AFC output sink current at pin 19		160	200	240	μΑ
V _{o(intc)(rms)}	intercarrier output voltage (RMS value)	$\frac{V_{i(SC)}}{V_{i(PC)}} = -24 \text{ dB ; note 4}$	-	49	_	mV

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
B _{intc(-3dB)(ul)}	upper limit –3 dB intercarrier bandwidth		7.5	9	_	MHz
V _{o(AF)(rms)}	audio output signal voltage at pin 8 (RMS value)	25 kHz FM deviation; 75 μs de-emphasis	400	500	600	mV
THD	total harmonic distortion		_	0.15	0.5	%
B _{AF(-3dB)}	-3 dB audio frequency bandwidth	without de-emphasis; dependent on loop filter at pin 4	100	120	_	kHz
S/N _{W(AF)}	weighted signal-to-noise ratio of	black picture	50	56	_	dB
	audio signal	white picture	45	51	_	dB
		6 kHz sine wave (black-to-white modulation)	40	46	_	dB
		sound carrier subharmonics; f = 2.25 MHz ±3 kHz	35	40	_	dB
$\alpha_{AM(sup)}$	AM suppression of FM demodulator	75 μs de-emphasis; AM: f = 1 kHz; m = 0.3 referenced to 25 kHz FM deviation	40	46	-	dB
PSRR ₈	power supply ripple rejection at pin 8	f _{ripple} = 70 Hz; see Fig.9	14	20	_	dB
Δf _{FM}	frequency window of digital acquisition help for FM demodulator		_	±225	_	kHz
f _{ref}	frequency of reference signal at pin 15		_	4.0	_	MHz
V _{ref(rms)}	amplitude of reference signal source (RMS value)	operation as input terminal	80	_	400	mV

Notes

- 1. Values of video and sound parameters can be decreased at $V_P = 4.5 \text{ V}$.
- The sound carrier frequencies (depending on TV standard) are attenuated by the integrated sound carrier traps (see Figs 13 to 18; |H (s)| is the absolute value of transfer function).
- 3. S/N is the ratio of black-to-white amplitude to the black level noise voltage (RMS value, pin 13). B = 4.2 MHz (M/N standard) or B = 5.0 MHz (B/G, I and D/K standard) weighted in accordance with "CCIR 567".
- 4. The intercarrier output signal at pin 11 can be calculated by the following formula taking into account the internal video signal with 1.1 V (p-p) as a reference:

$$V_{o(intc)(rms)} = 1.1 \text{ V (p-p)} \times \frac{1}{2\sqrt{2}} \times 10^{\frac{V_{i(SC)}}{V_{i(PC)}}(dB) + 6 dB \pm 3 dB}}{20}$$

where:

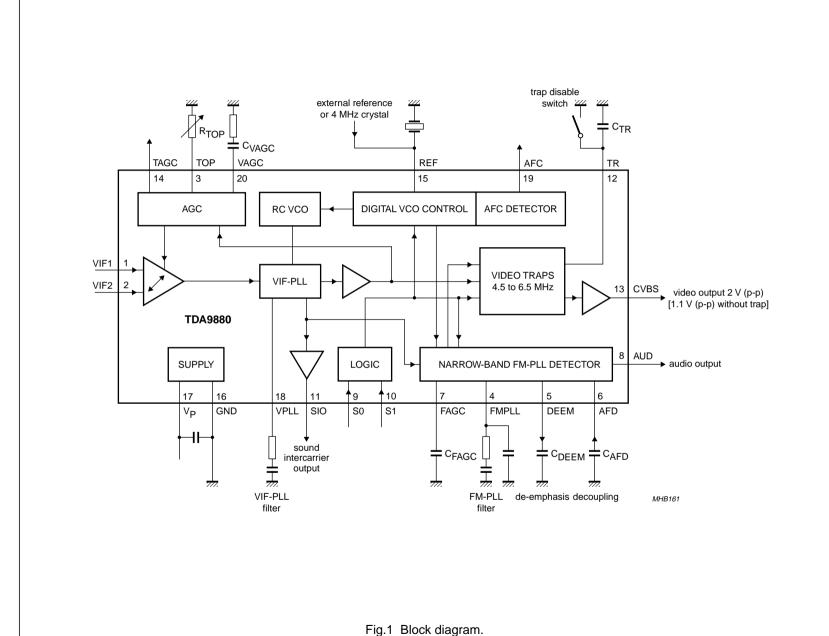
 $\frac{1}{2\sqrt{2}}$ = correction term for RMS value, $\frac{V_{i(SC)}}{V_{i(PC)}}$ (dB) = sound-to-picture carrier ratio at VIF input (pins 1 and 2) in dB,

6 dB = correction term of internal circuitry and ± 3 dB = tolerance of video output and intercarrier output amplitude $V_{o(intc)(rms)}$.

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BLOCK DIAGRAM

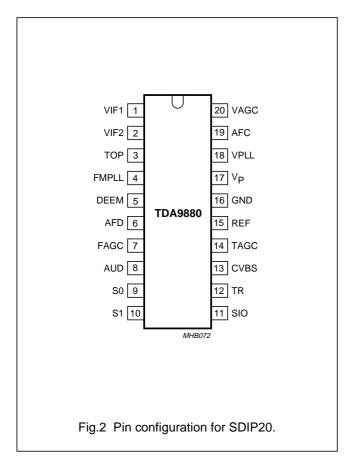


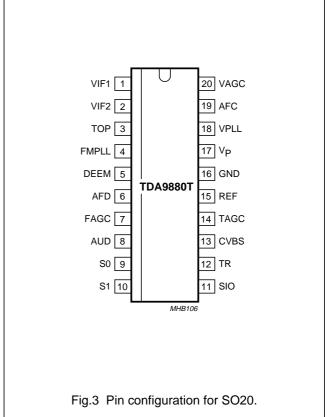
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PINNING

SYMBOL	PIN	DESCRIPTION
VIF1	1	VIF differential input 1
VIF2	2	VIF differential input 2
TOP	3	tuner AGC TakeOver Point (TOP)
FMPLL	4	FM-PLL for loop filter
DEEM	5	de-emphasis output for capacitor
AFD	6	AF decoupling input for capacitor
FAGC	7	FM-PLL AGC for capacitor
AUD	8	audio output
S0	9	switch input S0
S1	10	switch input S1

SYMBOL	PIN	DESCRIPTION
SIO	11	sound intercarrier output
TR	12	trap control
CVBS	13	video output
TAGC	14	tuner AGC output
REF	15	4 MHz crystal or reference input
GND	16	ground
V_{P}	17	supply voltage (+5 V)
VPLL	18	VIF-PLL for loop filter
AFC	19	AFC output
VAGC	20	VIF-AGC for capacitor





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FUNCTIONAL DESCRIPTION

Figure 1 shows the simplified block diagram of the integrated circuit. The integrated circuit comprises the following functional blocks:

- 1. VIF amplifier
- 2. Tuner and VIF-AGC
- 3. VIF-AGC detector
- 4. Frequency Phase-Locked Loop (FPLL) detector
- 5. VCO and Travelling Wave Divider (TWD)
- 6. Digital acquisition help and AFC
- 7. Video demodulator and amplifier
- 8. Sound carrier trap
- 9. Intercarrier mixer
- 10. FM demodulator and acquisition help
- 11. Audio amplifier
- 12. Internal voltage stabilizer.

VIF amplifier

The VIF amplifier consists of three AC-coupled differential amplifier stages. Each differential stage comprises a feedback network controlled by emitter degeneration.

Tuner and VIF-AGC

The AGC capacitor voltage is converted to an internal VIF gain control signal, and is fed to the tuner AGC to generate the tuner AGC output current at pin TAGC (open-collector output). The tuner AGC takeover point can be adjusted with R_{TOP}. This allows the tuner to be matched to the SAW filter in order to achieve the optimum IF input level.

VIF-AGC detector

The AGC detector generates the required VIF gain control voltage for constant video output by charging or discharging the AGC capacitor. Gain control is performed by sync level detection. The newly developed AGC circuit provides fast reaction time to cope with 'aeroplane fluttering'. The time constants for decreasing or increasing gain are nearly equal.

Frequency Phase-Locked Loop (FPLL) detector

The VIF amplifier output signal is fed into a Frequency Detector (FD) and into a Phase Detector (PD) via a limiting amplifier. During acquisition the frequency detector produces a DC current proportional to the frequency difference between the input and the VCO signal.

After frequency lock-in the phase detector produces a DC current proportional to the phase difference between the VCO and the input signal. The DC current of either the frequency detector or the phase detector is converted into a DC voltage via the loop filter, which controls the VCO frequency.

VCO and Travelling Wave Divider (TWD)

The Resistor Capacitor (RC) VCO operates as an integrated relaxation oscillator at double the picture carrier frequency. The control voltage required to tune the VCO to actually double the picture carrier frequency is generated by the FPLL detector and fed via the loop filter to the VCO control input terminal.

The oscillator signal is divided-by-two with a TWD which generates two differential output signals with a 90 degrees phase difference independent of the frequency.

Digital acquisition help and AFC

The integrated relaxation oscillator has a very wide frequency range from approximately 30 to 70 MHz (behind the TWD). To prevent false locking of the FPLL and with respect to the catching range of the frequency detector of maximum ± 2.5 MHz, the Digital Acquisition Help (DAH) provides current into the loop filter until the VCO is in a frequency window of ± 2.3 MHz around the wanted VIF frequency. In this case the analog operating FPLL will lock the VCO to the VIF carrier and the acquisition help does not provide any current to the loop filter.

The principle of the digital acquisition help is as follows: The VIF VCO is connected to a down counter, which is preset depending on the wanted VIF frequency. The counting time, as well as the counter control, is derived from a 4 MHz reference signal. Operation as 4 MHz crystal oscillator is possible as well as connecting to the 4 MHz reference oscillator of the tuning system. The counting result after a counting cycle corresponds to the actual VCO frequency.

The digital AFC is also derived from the counting result after a counting cycle by digital-to-analog converting the last four bits of the counter.

Video demodulator and amplifier

The video demodulator is realized by a multiplier which is designed for low distortion and large bandwidth. The vision IF input signal is multiplied with the 'in phase' signal of the travelling wave divider output.

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The demodulator output signal is fed via an integrated low-pass filter for attenuation of the carrier harmonics to the video amplifier. The video amplifier is realized by an operational amplifier with internal feedback and high bandwidth. A low-pass filter is integrated to achieve an attenuation of the carrier harmonics. The video signal of 1.1 V (p-p) for nominal vision IF modulation is fed internally to the integrated sound carrier trap as well as to the VIF-AGC detector. The second stage of the video amplifier converts and amplifies the differential output signal from the sound trap to the single-ended CVBS output signal at pin 13 with a 2 V (p-p) amplitude.

Noise clipping is provided. Furthermore the trap can be bypassed by the implemented input switch of the second amplifier stage, forced by connecting pin 12 to ground.

Sound carrier trap

The sound carrier trap consists of a reference filter, a phase detector and the sound trap itself.

A sound carrier reference signal is fed into the reference low-pass filter and is shifted by a nominal 90 degrees. The phase detector compares the original reference signal with the signal shifted by the reference filter and produces, at the external capacitor C_{TR} , a DC voltage by charging/discharging the capacitor with a current proportional to the phase difference between both signals, respectively to the frequency error of the integrated filters. The DC voltage is converted to currents which control the frequency position of the reference filter and the sound trap.

The sound trap itself is constructed of three separate traps to realize sufficient suppression of the first and second sound carrier. The right frequency position of the different standards is set by the sound carrier reference signal.

Intercarrier mixer

The intercarrier mixer is realized by a multiplier, operating in quadrature mode for suppression of low frequency video signals. The VIF amplifier output signal is fed to the intercarrier mixer and converted to an intercarrier frequency by the regenerated 90 degree picture carrier from the VCO. The mixer output signal is fed via a band-pass filter and amplifier for attenuation of the high frequency video signal components and carrier harmonics to the output pin 11. Also the intercarrier signal is fed to the integrated FM demodulator.

FM demodulator and acquisition help

The FM demodulator is realized as a narrow-band PLL with external loop filter, which provides the necessary selectivity. To achieve good selectivity, a linear phase detector and constant input level are required. The intercarrier signal from the intercarrier mixer is fed via a gain controlled amplifier to the phase detector, it's output signal controls (via the loop filter) the integrated relaxation oscillator. The possible frequency range is from 4 to 7 MHz. As a result of locking, the oscillator frequency tracks with the FM modulation of the input signal, therefore the oscillator control voltage is superimposed by the AF voltage. By this way the FM-PLL operates as an FM demodulator. The AF voltage is present at the loop filter and is fed via a buffer with 0 dB gain to the audio amplifier.

The digital acquisition help operates in the same way as described in Section "Digital acquisition help and AFC".

Audio amplifier

The audio amplifier consists of two parts:

- 1. The AF preamplifier is an operational amplifier with internal feedback, high gain and high common mode rejection. The AF voltage from the PLL demodulator, by principle a small output signal, is amplified by 30 dB. By use of a DC operating point control circuit (pin 6), the AF amplifier is decoupled from the PLL DC voltage. The low-pass characteristic of the amplifier reduces the harmonics of the intercarrier signal at the sound output terminal. If required, a de-emphasis network can be realized by the amplifier output resistance and an external capacitor.
- 2. The AF output amplifier (10 dB) provides the required output level by a rail-to-rail output stage. This amplifier makes use of an input selector for switching to mute state, automatically controlled by the mute switching voltage from the digital acquisition help in order to avoid lock-in noise. By normal operation the automatic audio mute function is not active. Application of a 2.2 kΩ resistor from the intercarrier output (pin 11) to GND will activate the automatic audio mute function.

Internal voltage stabilizer

The bandgap circuit internally generates a voltage of approximately 2.4 V, independent of supply voltage and temperature. A voltage regulator circuit, connected to this voltage, produces a constant voltage of 3.55 V which is used as an internal reference voltage.

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LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V _P	supply voltage	I_P = 115 mA; T_{amb} = 70 °C; maximum chip temperature of 125 °C	_	5.5	V
V _{i(n)}	input voltage at pins 1 to 4, 6 to 10, 12 and 17 to 20		0	V _P	V
V _{o(14)}	tuner AGC output voltage at pin 14		0	13.2	V
t _{sc}	short-circuit time to ground or V _P		_	10	s
T _{stg}	storage temperature		-25	+150	°C
T _{amb}	operating ambient temperature		-20	+70	°C
V _{es}	electrostatic handling for all pins	note 1	-250	+250	V
		note 2	-3000	+3000	V

Notes

- 1. Charge device model class A; machine model: discharging a 200 pF capacitor via a 0.75 μH inductance.
- 2. Charge device model class B; human body model: discharging a 100 pF capacitor via a 1.5 k Ω series resistor.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
R _{th(j-a)}	thermal resistance from junction to ambient	in free air		
	TDA9880 (SDIP20)		85	K/W
	TDA9880T (SO20)		85	K/W

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CHARACTERISTICS

 $V_P = 5 \text{ V}$; $T_{amb} = 25 \,^{\circ}\text{C}$; see Table 2 for input frequencies; M standard ($f_{PC} = 45.75 \,\text{MHz}$; $f_{SC} = 41.25 \,\text{MHz}$; $PC/SC = 10 \,\text{dB}$) is used for specification; input level $V_{i(V|F)(rms)} = 10 \,\text{mV}$ (sync level); IF input from 50 Ω via broadband transformer 1 : 1; video modulation DSB; residual carrier: 10%; video signal in accordance with "NTC-7 Composite"; measurements taken in test circuit of Fig.19; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply (pin 17)			•	•	•	•
V _P	supply voltage	note 1	4.5	5	5.5	V
l _Р	supply current		85	100	115	mA
P _{tot}	total power dissipation		_	500	633	mW
VIF amplifier (p	ins 1 and 2)		•		•	
V _{i(VIF)(rms)}	VIF input signal voltage sensitivity (RMS value)	-1 dB video at output	-	50	100	μV
V _{i(max)(rms)}	maximum input signal voltage (RMS value)	1 dB video at output	110	145	_	mV
ΔV_{int}	internal IF amplitude difference between picture and sound carrier	within AGC range; $\Delta f = 4.5 \text{ MHz}$	-	0.7	1	dB
G _{VIF(cr)}	VIF gain control range	see Fig.4	65	69	_	dB
B _{VIF(-3dB)(II)}	lower limit –3 dB VIF bandwidth		_	15	25	MHz
B _{VIF(-3dB)(ul)}	upper limit –3 dB VIF bandwidth		70	100	-	MHz
R _{i(dif)}	differential input resistance	note 2	1.7	2.2	2.7	kΩ
C _{i(dif)}	differential input capacitance	note 2	1.2	1.7	2.5	pF
VI	DC input voltage		_	3.35	_	V
FPLL and true	synchronous video demodulato	or; note 3				
f _{VCO(max)}	maximum oscillator frequency for carrier regeneration	f = 2f _{PC}	120	140	-	MHz
f_{VIF}	vision carrier operating	see Table 2	_	38.0	_	MHz
	frequencies		_	38.9	_	MHz
			_	45.75	_	MHz
			_	58.75	_	MHz
Δf_{VIF}	VIF frequency window of digital acquisition help	referenced to f _{VIF}	_	±2.38	_	MHz
t _{acq}	acquisition time	BL = 70 kHz; note 4	_	_	30	ms
V _{i(VIF)(rms)}	VIF input signal voltage sensitivity at pins 1 and 2 (RMS value)					
	for PLL to be locked	maximum IF gain	_	30	70	μV
	for C/N = 10 dB	notes 5 and 6	_	100	140	μV
I _{o(source)(PD)(max)}	maximum source current of phase detector output at pin 18		_	17	_	μА

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$I_{o(sink)(PD)(max)}$	maximum sink current of phase detector output at pin 18		_	17	_	μΑ
I _{o(source)(DAH)}	output source current of digital acquisition help at pin 18		_	23	_	μΑ
I _{o(sink)(DAH)}	output sink current of digital acquisition help at pin 18		_	23	_	μΑ
t _{W(min)(DAH)}	minimum pulse width of digital acquisition help current		_	64	_	μs
K _{O(VIF)}	VCO steepness Δf _{VIF} /ΔV ₁₈		_	20	_	MHz/V
$K_{D(VIF)}$	phase detector steepness $\Delta I_{18}/\Delta \phi_{VIF}$		_	23	-	μA/rad
Video output s	signal and sound carrier trap (pi	n 13; sound carrier off)		•		
$V_{o(v)(p-p)}$	video output signal voltage (peak-to-peak value)	see Fig.10	1.7	2.0	2.3	V
V _{sync}	synchronized voltage level		1.15	1.35	1.55	V
V _{zc}	zero carrier voltage level		3.27	3.57	3.87	V
$V_{v(clu)}$	upper video clipping voltage level		V _P – 1.1	V _P – 1	_	V
$V_{v(cll)}$	lower video clipping voltage level		_	0.7	1.0	V
R _o	output resistance	note 2	_	_	30	Ω
I _{bias(int)}	internal DC bias current for emitter-follower		2.0	2.5	_	mA
I _{o(source)(max)}	maximum AC and DC output source current		2.4	_	_	mA
I _{o(sink)(max)}	maximum AC and DC output sink current		1.4	_	_	mA
ΔV_{o}	deviation of CVBS output	50 dB gain control	_	_	0.5	dB
	signal voltage	30 dB gain control	_	_	0.1	dB
$\Delta V_{o(bl)}$	black level tilt		_	_	1	%
G _{dif}	differential gain	"NTC-7 Composite"	_	2	5	%
ϕ_{dif}	differential phase	"NTC-7 Composite"	_	2	4	deg
$B_{v(-3dB)(trap)}$	–3 dB video bandwidth including sound carrier trap	$C_L < 20 \text{ pF; } R_L > 1 \text{ k}\Omega;$ AC load; note 7				
		f _{trap} = 4.5 MHz (M/N standard)	3.95	4.05	_	MHz
		f _{trap} = 5.5 MHz (B/G standard)	4.90	5.00	_	MHz
		f _{trap} = 6.0 MHz (I standard)	5.2	5.50	_	MHz
		f _{trap} = 6.5 MHz (D/K standard)	5.5	5.95	_	MHz

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
α_{SC1}	attenuation at first sound	M/N standard	30	36	-	dB
	carrier	B/G standard	30	36	-	dB
		I standard	26	32	Ī-	dB
		D/K standard	26	32	-	dB
αSC1(60 kHz)	attenuation at first sound	M/N standard	21	27	_	dB
, ,	carrier f _{SC1} ±60 kHz	B/G standard	24	30	Ī-	dB
		I standard	20	26	-	dB
		D/K standard	20	26	_	dB
α_{SC2}	attenuation at second sound	M/N standard	21	27	-	dB
	carrier	B/G standard	21	27	_	dB
		I standard	12	18	-	dB
		D/K standard	18	24	Ī-	dB
α _{SC2(60 kHz)}	attenuation at second sound	M/N standard	15	21	_	dB
, ,	carrier f _{SC2} ±60 kHz	B/G standard	15	21	_	dB
		I standard	10	15	_	dB
		D/K standard	13	18	_	dB
t _{d(g)(cc)}	group delay at colour carrier	3.58 MHz at M/N standard	110	180	250	ns
-(3)()	frequency	4.43 MHz at B/G standard	110	180	250	ns
		4.43 MHz at I standard	_	90	160	ns
		4.28 MHz at D/K standard	_	60	130	ns
S/N _W	weighted signal-to-noise ratio	weighted in accordance with "CCIR 567"; see Fig.6; note 8	56	60	_	dB
S/N _{UW}	unweighted signal-to-noise ratio	note 8	47	51	-	dB
αd _{blue}	intermodulation attenuation at 'blue'	f = 0.92 MHz; see Fig.7; note 9	58	64	-	dB
		f = 2.76 MHz; see Fig.7; note 9	58	64	-	dB
αd _{yellow}	intermodulation attenuation at 'yellow'	f = 0.92 MHz; see Fig.7; note 9	60	66	_	dB
		f = 2.76 MHz; see Fig.7; note 9	59	65	_	dB
$\Delta V_{r(vc)(rms)}$	residual vision carrier (RMS value)	fundamental wave and harmonics	_	2	5	mV
$lpha_{H(sup)}$	suppression of video signal harmonics	C_L < 20 pF; R_L > 1 k Ω ; AC load; note 10a	35	40	_	dB
$\alpha_{H(spur)}$	suppression of spurious elements	note 10b	40	_	_	dB
PSRR ₁₃	power supply ripple rejection at pin 13	f _{ripple} = 70 Hz; video signal; grey level; see Fig.9	25	28	_	dB

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Video output :	signal (pin 13; trap bypass mode	e; V ₁₂ < 0.8 V; sound carrie	er off); see	e Fig.10; n	ote 11	
$V_{o(v)(p-p)}$	video output signal voltage (peak-to-peak value)	see Fig.10	0.95	1.10	1.25	V
V _{sync}	synchronized voltage level		1.4	1.5	1.6	V
V _{zc}	zero carrier voltage level		2.57	2.72	2.87	V
$V_{v(clu)}$	upper video clipping voltage level		3.1	3.25	_	V
$V_{v(\text{cll})}$	lower video clipping voltage level		_	1.15	1.3	V
B _{v(-1dB)}	-1 dB video bandwidth	C_L < 20 pF; R_L > 1 k Ω ; AC load	5	6	_	MHz
B _{v(-3dB)}	-3 dB video bandwidth	C_L < 20 pF; R_L > 1 k Ω ; AC load	7	8	_	MHz
S/N _W	weighted signal-to-noise ratio	weighted in accordance with "CCIR 567"; see Fig.6; note 8	56	60	_	dB
S/N _{UW}	unweighted signal-to-noise ratio	note 8	49	53	_	dB
Trap control (pin 12)		•			
I _{o(source)(max)}	maximum output source current		5	9	13	μΑ
I _{o(sink)(max)}	maximum output sink current		9	13	17	μΑ
$K_{D(trap)}$	frequency detector steepness $\Delta I_{12}/\Delta f_{trap}$	$f_{trap} = 4.5 \text{ MHz}$ (M/N standard)	_	-8	_	μA/MHz
		f _{trap} = 6.5 MHz (D/K standard)	_	-5.5	_	μA/MHz
V ₁₂	operating voltage range of trap frequency control at pin 12		1.5	_	3.5	V
I _{L(12)}	allowable leakage current at pin 12	$\Delta f_{trap} < \pm 25 \text{ kHz}$	_	-	±80	nA
CR _{stps}	control steepness $\Delta f_{trap}/\Delta V_{12}$	f _{trap} = 4.5 MHz (M/N standard)	_	4.5	-	MHz/V
		f _{trap} = 6.5 MHz (D/K standard)	_	9	-	MHz/V
V _{sw}	switching voltage	trap bypass mode active	_	-	0.8	V
I _{source}	source current	trap bypass mode active; $V_{12} \le 0.8 \text{ V}$	_	185	_	μΑ

Alignment-free multistandard vision and FM sound IF-PLL demodulator

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
VIF-AGC detec	ctor (pin 20)			-!-	'	
I _{ch(max)(20)}	maximum charge current		6	8	10	μΑ
I _{dch(max)(20)}	maximum discharge current		7.5	10	12.5	μΑ
t _{res}	AGC response time to an	6 dB; note 12	-	2.0	_	ms
	increasing VIF step	20 dB; note 12	_	2.5	_	ms
		40 dB; note 12	_	4.0	_	ms
	AGC response time to a	-6 dB; note 12	_	1.0	_	ms
	decreasing VIF step	-20 dB; note 12	_	1.5	_	ms
		-40 dB; note 12	_	2.5	_	ms
V ₂₀	gain control voltage range at pin 20		1.7	_	3.6	V
CR _{stps}	control steepness $\Delta G_{IF}/\Delta V_{20}$	V ₂₀ = 2.2 to 3.2 V	_	-40	_	dB/V
Tuner AGC (pi	n 14); see Figs 4 and 5					•
V _{i(VIF)(rms)}	VIF input signal voltage for minimum starting point of tuner takeover at pins 1 and 2 (RMS value)	$R_{TOP} = 22 \text{ k}\Omega;$ $I_{14} = 120 \mu\text{A}$	_	2	5	mV
	VIF input signal voltage for maximum starting point of tuner takeover at pins 1 and 2 (RMS value)	$R_{TOP} = 0 \Omega$; $I_{14} = 120 \mu A$	45	90	-	mV
QV _{i(VIF)(rms)}	tuner takeover point accuracy	$R_{TOP} = 12 \text{ k}\Omega;$ $I_{14} = 120 \mu\text{A}$	5	10	20	mV
V _o	permissible output voltage	from external source	_	_	13.2	V
V _{sat}	saturation voltage	I ₁₄ = 450 μA	-	_	0.2	V
$V_{i(VIF)(rms)}/\Delta T$	variation of takeover point with temperature	I ₁₄ = 120 μA	_	0.03	0.07	dB/K
I _{sink(14)}	sink current	no tuner gain reduction; see Fig.4				
		V ₁₄ = 12 V	_	_	0.75	μΑ
		V ₁₄ = 13.2 V	_	_	1.5	μΑ
		maximum tuner gain reduction; V ₁₄ = 1 V; see Fig.4	450	600	750	μΑ
ΔG_{IF}	IF slip by automatic gain control	tuner gain current from 20 to 80%	_	5	8	dB

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
AFC circuit (p	in 19); notes 13 and 14			'	'	!
AFC _{stps}	AFC steepness ΔI ₁₉ /Δf _{VIF}		0.85	1.05	1.25	μΑ/kHz
Qf _{VIF}	accuracy of AFC circuit	$I_{o(19)} = 0$; $f_{15} = 4.0 \text{ MHz}$	-20	_	+20	kHz
V _{sat(ul)}	upper limit saturation voltage	see Fig.8	V _P – 0.6	V _P – 0.3	_	V
V _{sat(II)}	lower limit saturation voltage	see Fig.8	_	0.3	0.6	V
I _{o(source)}	output source current		160	200	240	μΑ
I _{o(sink)}	output sink current		160	200	240	μΑ
Intercarrier mi	xer (pin 11)					
V _{o(intc)(rms)}	intercarrier output voltage (RMS value)	$\frac{V_{i(SC)}}{V_{i(PC)}} = -24 \text{ dB}; \text{ note 15}$	_	49	_	mV
B _{intc(-3dB)(ul)}	upper limit –3 dB intercarrier bandwidth		7.5	9	_	MHz
$\Delta V_{r(SC)(rms)}$	residual sound carrier (RMS value)	fundamental wave and harmonics	_	2	_	mV
R _o	output resistance	note 2	_	_	70	Ω
Vo	DC output voltage		1.85	2.05	2.35	V
I _{bias(int)}	internal DC bias current for emitter-follower		0.9	1.15	_	mA
I _{o(source)(max)}	maximum AC output source current	note 16	0.6	0.8	_	mA
$I_{o(sink)(max)}$	maximum AC output sink current	note 16	0.6	0.8	_	mA
I _{O(source)}	DC output source current	automatic audio mute function activated; note 16	0.75	0.93	1.20	mA
FM-PLL demo	dulator; notes 14 and 17 to 20					
V _{o(AF)(rms)}	audio output signal voltage at	25 kHz FM deviation	400	500	600	mV
, ,, ,	pin 8 (RMS value)	27 kHz FM deviation	432	540	648	mV
V _{O(AF)(cl)(rms)}	audio output clipping signal voltage level at pin 8 (RMS value)	THD < 1.5%	1.3	1.4	_	V
THD	total harmonic distortion		_	0.15	0.5	%
$\Delta V_{o(AF)}/\Delta T$	temperature drift of AF output signal voltage		_	3 × 10 ⁻³	7 × 10 ⁻³	dB/K
Δf_{AF}	audio frequency deviation	THD < 1.5%; note 21	_	_	±55	kHz
V _{FM(rms)}	IF intercarrier level at pin 11 for gain controlled operation of FM-PLL (RMS value)	corresponding PC/SC ratio at input pins 1 and 2 is 7 to 40 dB	6	-	320	mV
V _{FM(lock)(rms)}	IF intercarrier level at pin 11 for lock-in of PLL (RMS value)		_	_	3	mV
G _{FM}	IF intercarrier gain control range		30	34	_	dB

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V ₇	gain control voltage range at pin 7		1.5	_	3.5	V
I _{ch(max)(7)}	maximum charge current at pin 7		1.5	2.2	2.9	μА
I _{dch(max)(7)}	maximum discharge current at pin 7		1.5	2.2	2.9	μΑ
CR _{stps}	control steepness $\Delta G_{FM}/\Delta V_7$	$V_7 = 2.2 \text{ to } 2.7 \text{ V}$	_	-30	_	dB/V
B _{AF(-3dB)}	-3 dB audio frequency bandwidth	without de-emphasis; dependent on loop filter at pin 4; measured in accordance with Fig.19	80	100	_	kHz
S/N _W	weighted signal-to-noise ratio	black picture	50	56	_	dB
	of audio signal	white picture	45	51	_	dB
		6 kHz sine wave (black-to-white modulation)	40	46	_	dB
		sound carrier subharmonics; f = 2.25 MHz ±3 kHz	35	40	-	dB
$\Delta V_{r(SC)(8)(rms)}$	residual sound carrier at pin 8 (RMS value)	fundamental wave and harmonics; without de-emphasis	_	_	2	mV
$\alpha_{AM(sup)}$	AM suppression of FM demodulator	75 μs de-emphasis; AM: f = 1 kHz; m = 0.3 referenced to 25 kHz FM deviation	40	46	-	dB
PSRR ₈	power supply ripple rejection at pin 8	f _{ripple} = 70 Hz; see Fig.9	14	20	-	dB
f _{intc}	sound intercarrier operating	see Table 2	_	4.5	_	MHz
	frequencies		_	5.5	_	MHz
			_	6.0	_	MHz
			_	6.5	_	MHz
Δf_{FM}	frequency window of digital acquisition help for FM demodulator		_	±225	_	kHz
I _{o(source)(PD)(max)}	maximum phase detector output source current of at pin 4		_	86	_	μΑ
I _{o(sink)(PD)(max)}	maximum phase detector output sink current of at pin 4		_	80	-	μΑ
I _{o(source)(DAH)}	output source current of digital acquisition help at pin 4		_	110	_	μΑ
I _{O(Sink)(DAH)} output sink current of digital acquisition help at pin 4			_	110	_	μΑ

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$t_{w(DAH)}$	pulse width of digital acquisition help current		-	16	-	μs
T _{cy(DAH)}	cycle time of digital acquisition help		_	64	-	μs
K _{O(FM)}	VCO steepness $\Delta f_{FM}/\Delta V_4$		-	3.3	_	MHz/V
K _{D(FM)}	phase detector steepness $\Delta I_4/\Delta\phi_{FM}$		_	9	_	μA/rad
Audio amplifie	r (pins 5, 6 and 8)		•	•	•	•
R _{o(5)}	output resistance at pin 5	note 22	4.4	5.0	5.6	kΩ
V _{AF(5)(rms)}	audio signal (RMS value) at pin 5		_	170	-	mV
V _{O(5)}	DC output voltage at pin 5		_	2.37	_	V
R _{o(8)}	output resistance at pin 8	note 2	_	_	200	Ω
V _{O(8)}	DC output voltage at pin 8		_	2.37	_	V
I _{o(source)(max)(8)}	maximum AC and DC output source current at pin 8		_	-	0.5	mA
I _{o(sink)(max)(8)}	maximum AC and DC output sink current at pin 8		_	_	0.5	mA
V ₆	DC decoupling voltage at pin 6	dependent on intercarrier frequency f _{FM}	1.5	_	3.3	V
I _{L(6)}	allowable leakage current at pin 6	$\Delta V_{O(8)} < \pm 50 \text{ mV}$	_	_	±25	nA
I _{ch(max)(6)}	maximum charge current at pin 6		1.15	1.5	1.85	μА
I _{dch(max)(6)}	maximum discharge current at pin 6		1.15	1.5	1.85	μА
B _{AF(-3dB)}	-3 dB audio frequency	upper limit	150	_	_	kHz
	bandwidth of audio amplifier	lower limit; note 23	_	_	20	Hz
$\alpha_{mute(8)}$	mute attenuation of AF signal at pin 8	note 16	70	75	-	dB
ΔV_8	DC jump voltage at pin 8 for switching AF output to mute state and vice versa	activated by digital acquisition help; note 16		±50	±150	mV
Standard swite	ch (pins 9 and 10); see Table 2		•			
Vi	input voltage	pin open-circuit; I _{i(9,10)} < 0.1 μΑ	2.8	3.0	3.6	V
		for LOW	0	_	0.8	V
		for MID	1.3	1.8	2.3	V
		for HIGH	2.8	_	V _P	V
I _{i(source)}	input source current	$V_{i(9,10)} = 0 V$	87	105	122	μΑ
		V _{i(9,10)} = 1.8 V	33	39	45	μΑ

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Reference inpu	it (pin 15); note 24			•	•	•
VI	DC input voltage		2.3	2.6	2.9	V
R _i	input resistance		2.5	3.0	3.5	kΩ
R _{xtal}	resonance resistance of crystal	operation as crystal oscillator	_	_	200	Ω
C _x	pull-up/down capacitance	note 25	_	_	_	pF
f _{ref}	frequency of reference signal		_	4.0	_	MHz
Δf_{ref}	tolerance of reference frequency	note 14	-	_	±0.1	%
V _{ref(rms)}	amplitude of reference signal source (RMS value)	operation as input terminal	80	_	400	mV
R _{o(ref)}	output resistance of reference source		_	_	4.7	kΩ
C _K	decoupling capacitance to external reference source	operation as input terminal	22	100	_	pF

Notes to the Characteristics

- 1. Values of video and sound parameters can be decreased at $V_P = 4.5 \text{ V}$.
- This parameter is not tested during production and is only given as application information for designing the television receiver.
- 3. Loop bandwidth BL = 70 kHz (damping factor d = 1.9; calculated with sync level within gain control range). Calculation of the VIF-PLL filter can be done by use of the following formula:

$$BL_{-3 dB} = \frac{1}{2\pi} K_O K_D R$$
, valid for $d \ge 1.2$

$$d \; = \; \frac{1}{2} R \, \sqrt{K_O K_D C} \; , \label{eq:delta_relation}$$

where:

$$K_{O}$$
 = VCO steepness $\left(\frac{\text{rad}}{V}\right)$ or $\left(2\pi\frac{\text{Hz}}{V}\right)$; K_{D} = phase detector steepness $\left(\frac{\mu A}{\text{rad}}\right)$;

R = loop resistor; C = loop capacitor; $BL_{-3 dB}$ = loop bandwidth for -3 dB; d = damping factor.

- V_{i(VIF)(rms)} = 10 mV; Δf = 1 MHz (VCO frequency offset related to picture carrier frequency); white picture video modulation.
- 5. V_{i(VIF)} signal for nominal video signal.
- Broadband transformer at VIF input. The C/N ratio at IF input is defined as the VIF input signal (sync level, RMS value) in relation to a superimposed 4.2 MHz band-limited white noise signal (RMS value); white picture video modulation.
- 7. The sound carrier frequencies (depending on TV standard) are attenuated by the integrated sound carrier traps (see Figs 13 to 18; |H (s)| is the absolute value of transfer function).

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8. S/N is the ratio of black-to-white amplitude to the black level noise voltage (RMS value, pin 13). B = 4.2 MHz (M/N standard) or B = 5.0 MHz (B/G, I and D/K standard).

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9. The intermodulation figures are defined:

$$\alpha_{0.92} = 20 \, \log\!\left(\frac{\text{V}_0 \text{at } 3.58 \, \text{MHz}}{\text{V}_0 \text{at } 0.92 \, \text{MHz}}\right) + 3.6 \, \text{dB} \; ; \; \alpha_{0.92} \; \text{value at } 0.92 \, \text{MHz} \; \text{referenced to black or white signal;}$$

$$\alpha_{2.76} = 20 \, \log\!\left(\frac{\text{V}_0 \text{at } 3.58 \, \text{MHz}}{\text{V}_0 \text{at } 2.76 \, \text{MHz}}\right) ; \; \alpha_{2.76} \; \text{value at } 2.76 \, \text{MHz} \; \text{referenced to colour carrier.}$$

- 10. Measurements taken with SAW filter M1963M (sound shelf: 20 dB); loop bandwidth BL = 70 kHz.
 - a) Modulation Vestigial Side-Band (VSB); sound carrier off; f_{video} > 0.5 MHz.
 - b) Sound carrier on; f_{video} = 10 kHz to 10 MHz.
- 11. The sound carrier trap can be disabled by switching pin 12 to ground (<0.8 V). By this way the full composite video spectrum appears at pin 13. The amplitude is 1.1 V (p-p).
- 12. Response time valid for a VIF input level range of 200 μ V to 70 mV.
- 13. To match the AFC output signal to different tuning systems a current source output is provided. The test circuit is given in Fig.8. The AFC steepness can be changed by resistors R1 and R2.
- 14. The tolerance of the reference frequency determines the accuracy of the VIF AFC, FM demodulator centre frequency and maximum FM deviation.
- 15. The intercarrier output signal at pin 11 can be calculated by the following formula taking into account the internal video signal with 1.1 V (p-p) as a reference:

$$V_{o(intc)(rms)} = 1.1 \text{ V (p-p)} \times \frac{1}{2\sqrt{2}} \times 10^{\frac{V_{i(SC)}}{V_{i(PC)}}(dB) + 6 dB \pm 3 dB}$$

where:

 $\frac{1}{2\sqrt{2}} = \text{correction term for RMS value}, \frac{V_{i\,(SC)}}{V_{i\,(PC)}} \, (\text{dB}) = \text{sound-to-picture carrier ratio at VIF input (pins 1 and 2) in dB},$

6 dB = correction term of internal circuitry and ± 3 dB = tolerance of video output and intercarrier output amplitude $V_{o(intc)(rms)}$.

- 16. For normal operation no DC load at pin 11 is allowed, the automatic audio mute function is not active. By application of a 2.2 k Ω resistor from pin 11 to GND the automatic audio mute function will be activated. With this application also the series capacitor C_S of the loop filter at pin 4 should be changed from $C_S = 33$ nF to $C_S = 4.7$ nF.
- 17. Calculation of the FM-PLL filter can be done approximately by use of the following formulae:

$$\begin{split} &f_o = \frac{1}{2\pi} \sqrt{\frac{K_O K_D}{C_P}} \\ &\vartheta = \frac{1}{2R \sqrt{K_O K_D C_P}} \\ &BL_{-3 \ dB} = f_o \bigg(\ 1.55 - \vartheta^2 \bigg) \end{split}$$

The formulae are only valid under the following conditions:

 $\vartheta \le 1$ and $C_S > 5C_P$

where:

$$K_{O} = VCO \; steepness \left(\frac{rad}{V}\right) \; or \left(2\pi \frac{Hz}{V}\right); \; K_{D} = phase \; detector \; steepness \left(\frac{\mu A}{rad}\right);$$

 R_S = loop resistor; C_S = series capacitor; C_P = parallel capacitor; f_o = natural frequency of PLL;

 $BL_{-3 dB}$ = loop bandwidth for -3 dB; ϑ = damping factor. For examples see Table 1.

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18. For all S/N measurements the used vision IF modulator has to meet the following specification: Incidental phase modulation for black-to-white jump less than 0.5 degrees.

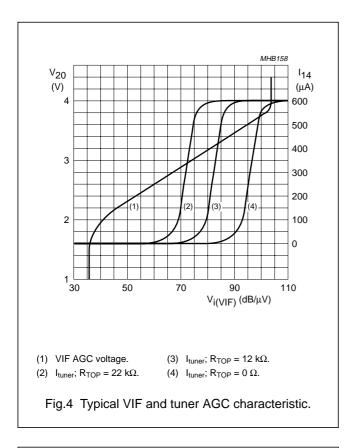
- 19. Measurements taken with SAW filter M1963M (Siemens) for vision and sound IF (sound shelf: 20 dB). Picture-to-sound carrier ratio of transmitter: PC/SC = 10 dB. Input level at pins 1 and 2 $V_{i(VIF)(rms)}$ = 10 mV (sync level), 25 kHz FM deviation for sound carrier, f_{AF} = 400 Hz. Measurement in accordance with "CCIR 468-4". De-emphasis = 75 μ s.
- 20. The PC/SC ratio is calculated as the addition of TV transmitter PC/SC ratio and SAW filter PC/SC ratio. This PC/SC ratio is necessary to achieve the S/N_W values as noted. A different PC/SC ratio will change these values.
- 21. Measured with an FM deviation of 25 kHz, the typical AF output signal is 500 mV RMS value. By using R_x = 20 k Ω the AF output signal is attenuated by 6 dB (250 mV RMS value). For handling an FM deviation of more than 55 kHz the AF output signal has to be reduced by using R_x in order to avoid clipping (THD < 1.5%). For an FM deviation up to 100 kHz an attenuation of 6 dB is recommended.
- 22. C_{DEEM} = 10 nF results in τ = 50 μ s and C_{DEEM} = 15 nF results in τ = 75 μ s.
- 23. The lower limit of audio bandwidth depends on the value of the capacitor at pin 6. A value of C_{AFD} = 470 nF leads to $f_{AF(-3 \text{ dB})} \approx 20 \text{ Hz}$ and C_{AFD} = 220 nF leads to $f_{AF(-3 \text{ dB})} \approx 40 \text{ Hz}$.
- 24. The reference input pin 15 is able to operate as a 1-pin crystal oscillator as well as input terminal with external reference signal, e.g. from the tuning system.
- 25. The value of C_x determines the accuracy of the resonance frequency of crystal. It depends on the type of crystal used.

Table 1 Examples to note 17 of Chapter "Characteristics"

BL _{-3 dB} (kHz)	C _S (nF)	C _P (pF)	R (kΩ)	ϑ
100	33	820	2.7	0.5
160	33	330	3.9	0.5

Table 2 Standard switch settings

S0	S1	f _{VIF} (MHz)	f _{intc} (MHz)	STANDARD	REMARK
LOW	LOW	38.9	5.5	B/G	Europe
LOW	MID	38.9	6.5	D/K	
LOW	HIGH	38.9	6.0	I	United Kingdom
MID	LOW	38.0	5.5	B/G	
MID	MID	38.0	6.0	I	
MID	HIGH	38.0	6.5	D/K	
HIGH	LOW	45.75	4.5	M/N	USA
HIGH	MID	38.0	4.5	М	
HIGH	HIGH	58.75	4.5	М	Japan



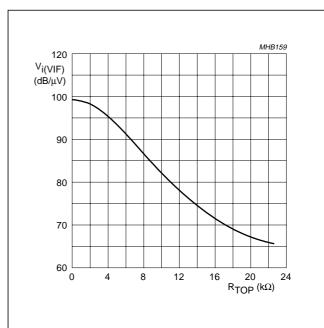


Fig.5 Typical tuner takeover point as a function of R_{TOP} .

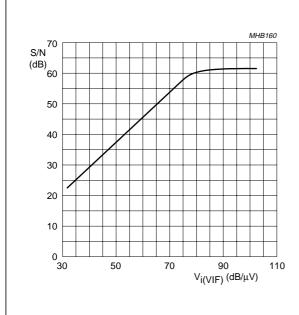
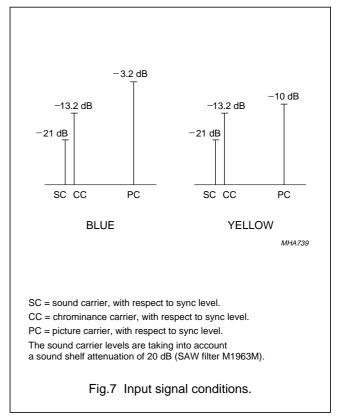
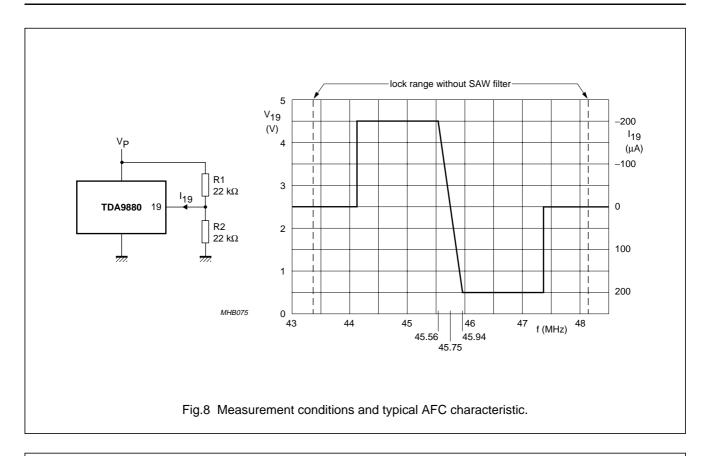
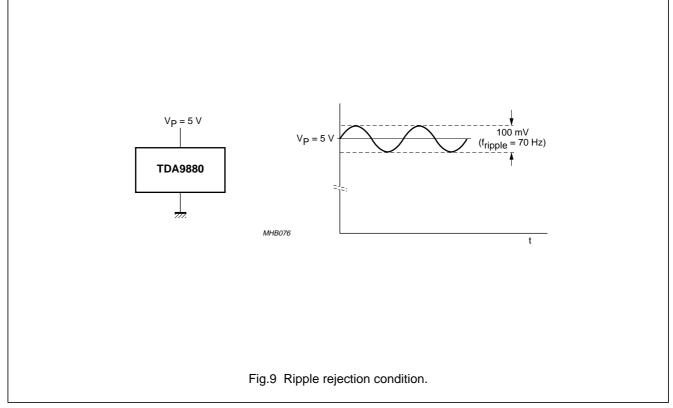


Fig.6 Typical signal-to-noise ratio as a function of VIF input voltage.



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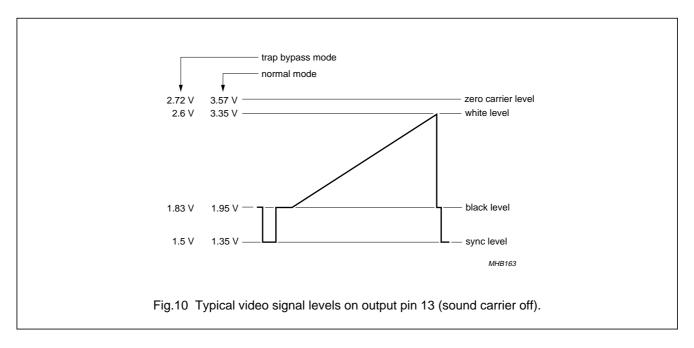


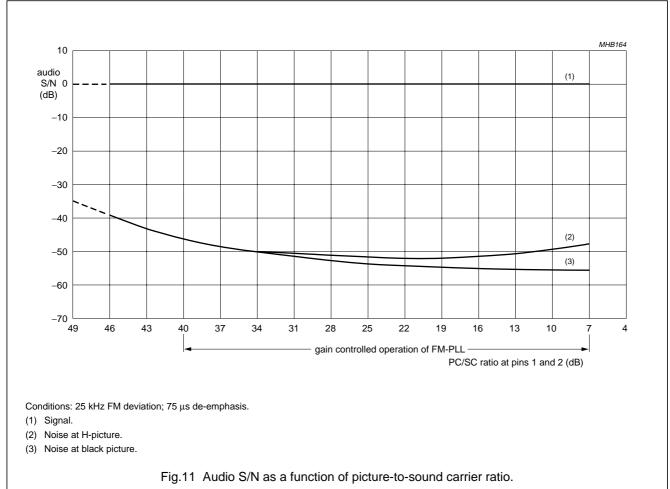


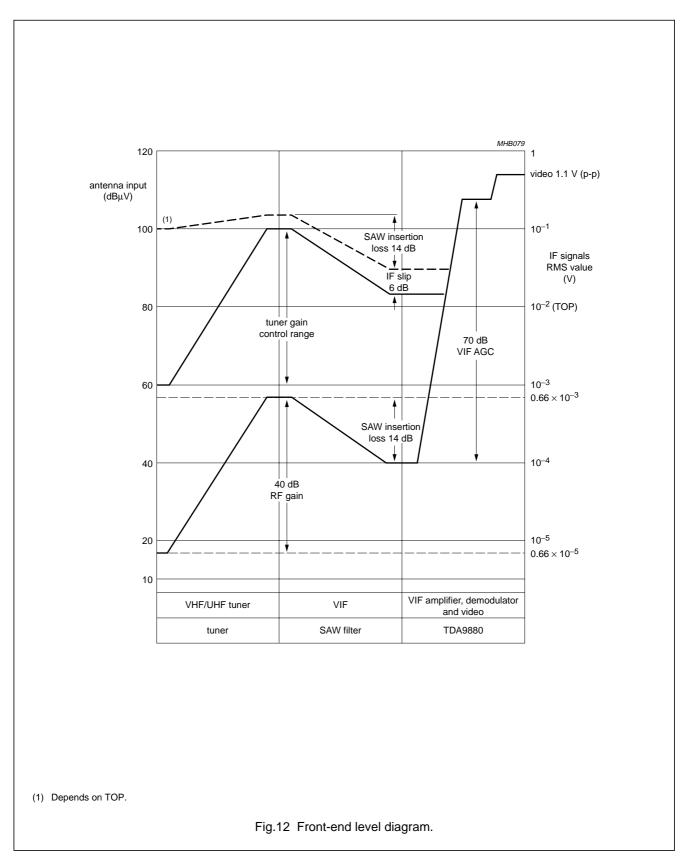
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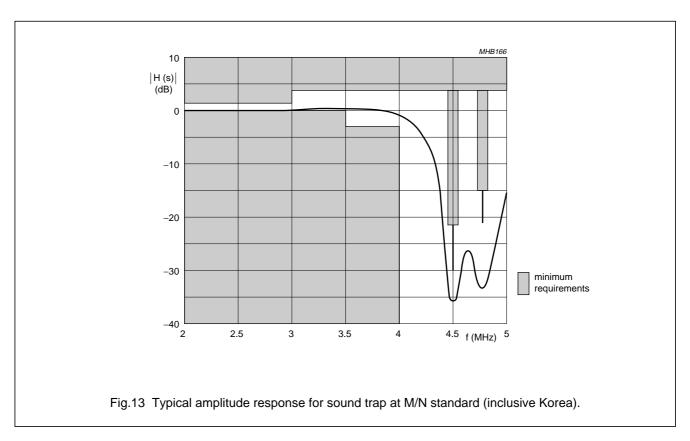
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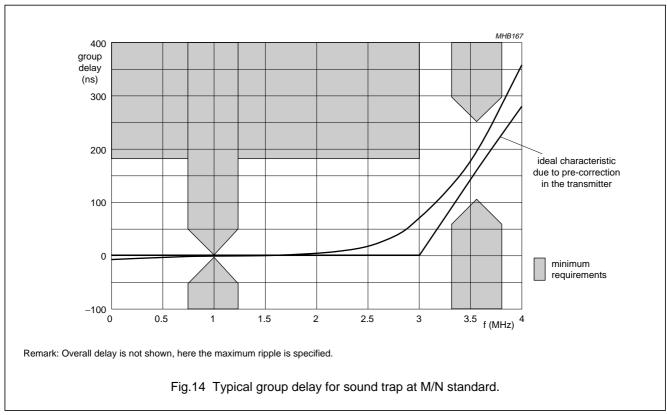




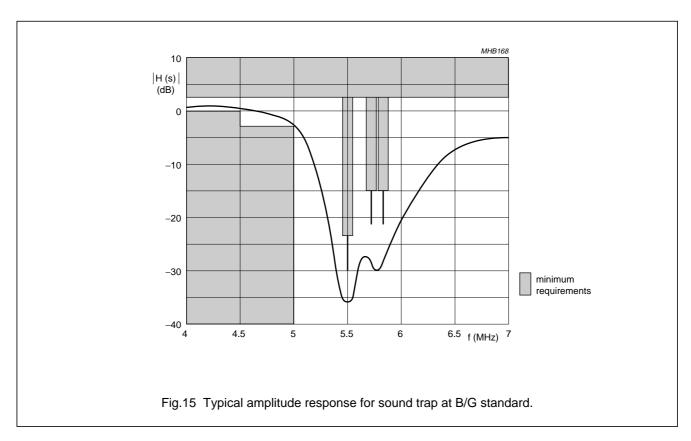


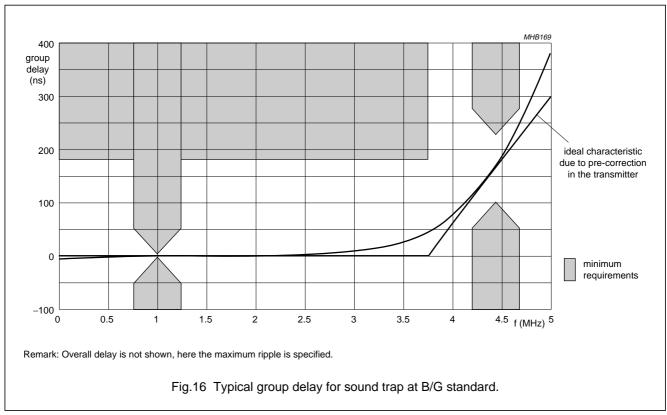
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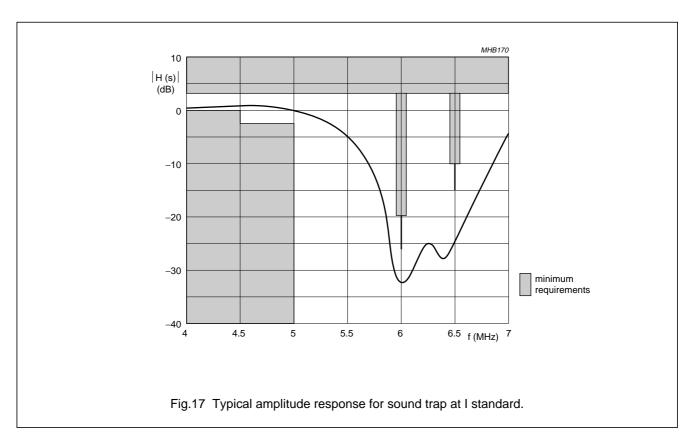


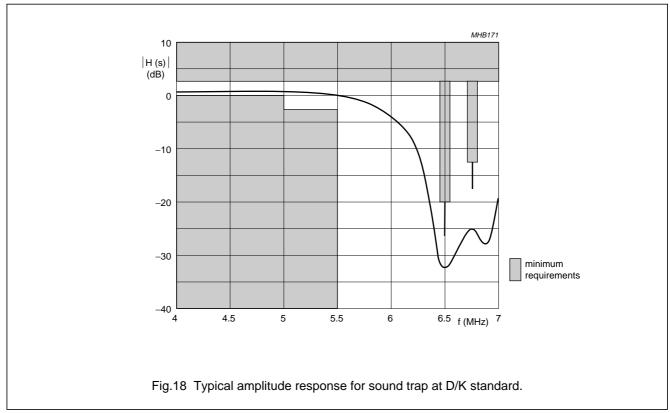
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TEST CIRCUIT

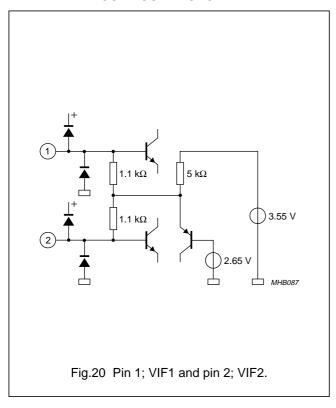
Philips Semiconductors

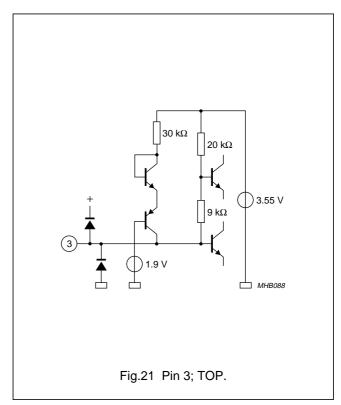
(1) VIF-PLL sound AFC TAGC **CVBS** intercarrier output filter output output output 1.5 kΩ $k\Omega$ 100 nF auto 3.3 150 Ω МΩ mute C_{TR} 📥 4 MHz 470 | 10 nF С 2.2 kΩ ≠ 220 nF $+ c_{x^{(3)}}$ C_{VAGC} $22 \text{ k}\Omega$ fref bypass V_{P} VAGC AFC VPLL **GND** REF **TAGC CVBS** TR SIO 20 19 18 17 16 15 14 13 12 11 TDA9880 3 8 9 10 VIF1 VIF2 TOP FMPLL DEEM AFD FAGC AUD S1 # 470 nF 1:1 C_S IF input C_{FAGC} $22 \text{ k}\Omega$ 33 nF C_{P} (4) RTOP 820 = $\int R_{X}$ 50 47 47 Ω рF R_S C_{DEEM} kΩ kΩ $2.7 \text{ k}\Omega$ FM-PLL audio logic filter output MHB162 (2)

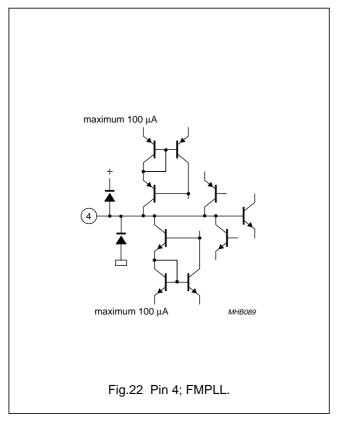
- (1) See note 3 of Chapter "Characteristics".
- (2) See notes 16 and 17 of Chapter "Characteristics".
- (3) See note 25 of Chapter "Characteristics".
- (4) See note 21 of Chapter "Characteristics".

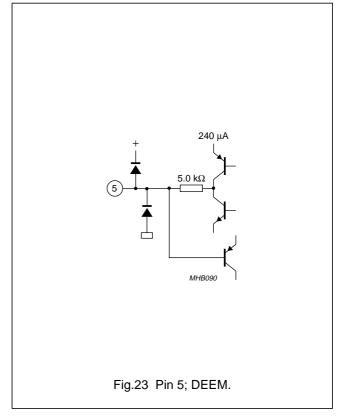
Fig.19 Test circuit.

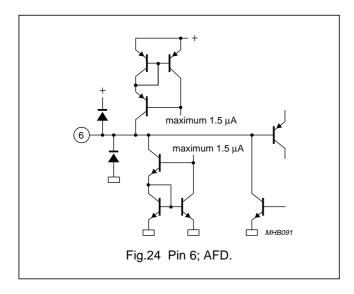
INTERNAL PIN CONFIGURATIONS

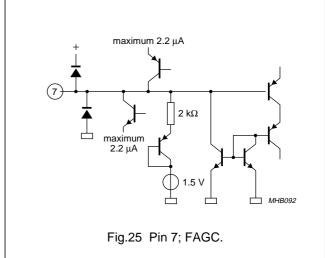


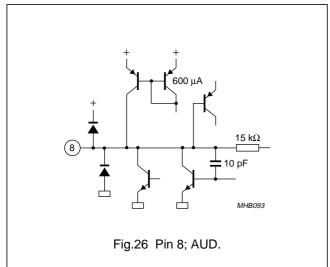


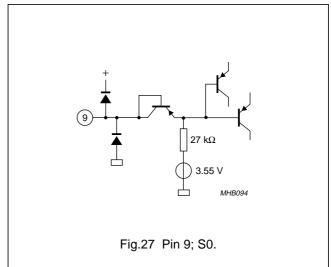


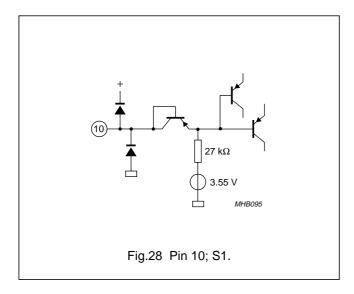


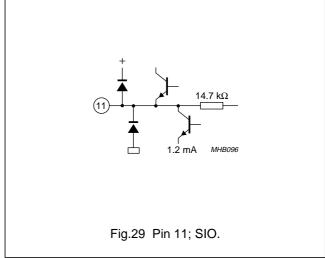


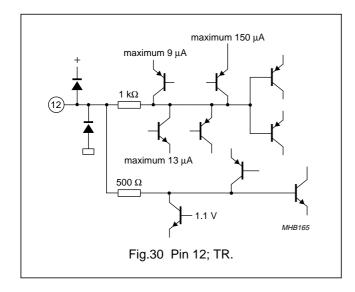


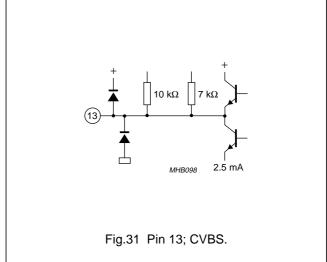


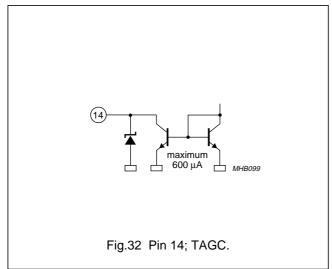


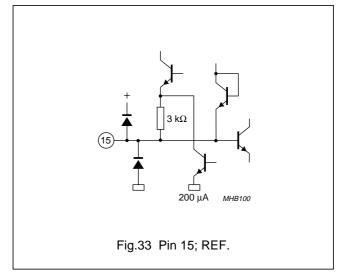


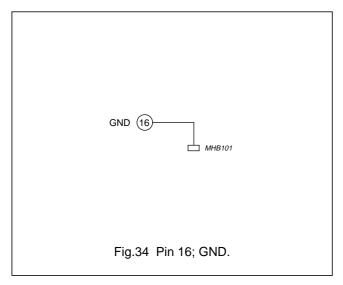


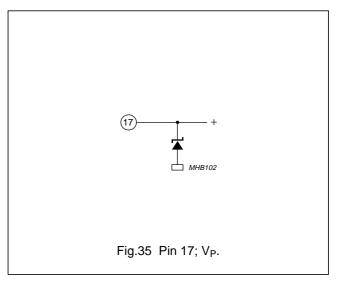


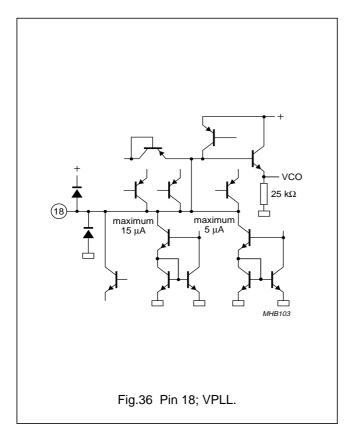


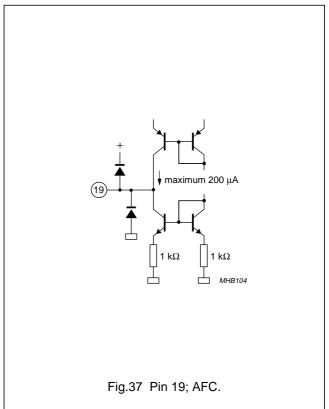


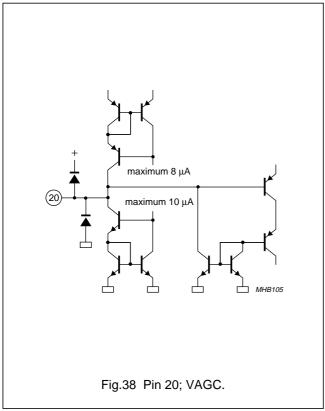










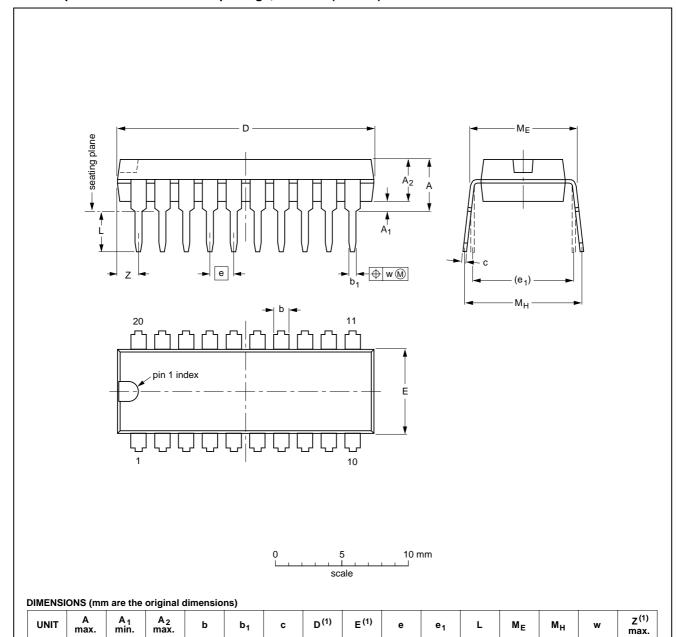


TDA9880

PACKAGE OUTLINES

SDIP20: plastic shrink dual in-line package; 20 leads (300 mil)

SOT325-1



UNIT

mm

4.2

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

3.2

b

1.3

1.0

 b_1

0.53

0.38

С

0.32

0.20

A₁ min.

0.51

OUTLINE		REFER	ENCES	EUROPEAN	ISSUE DATE
VERSION	IEC	JEDEC	EIAJ	PROJECTION	ISSUE DATE
SOT325-1					92-10-13 95-02-04

E⁽¹⁾

6.14

L

3.2

2.8

e₁

7.62

1.778

 M_{E}

8.25

7.80

 M_{H}

10.0

0.18

1.9

D⁽¹⁾

19.50

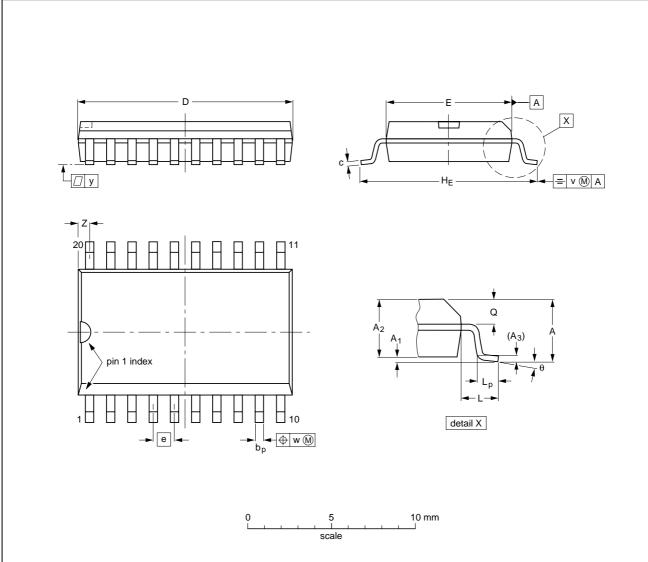
18.55

1998 Aug 12 33

TDA9880

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	bp	С	D ⁽¹⁾	E ⁽¹⁾	е	HE	L	Lp	Q	v	w	у	z ⁽¹⁾	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	0°

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE		REFER	ENCES	EUROPEAN	ISSUE DATE
VERSION	IEC	JEDEC	EIAJ	PROJECTION	ISSUE DATE
SOT163-1	075E04	MS-013AC			95-01-24 97-05-22

TDA9880

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our "Data Handbook IC26; Integrated Circuit Packages" (order code 9398 652 90011).

SDIP

SOLDERING BY DIPPING OR BY WAVE

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

REPAIRING SOLDERED JOINTS

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

SO

REFLOW SOLDERING

Reflow soldering techniques are suitable for all SO packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at $45\,^{\circ}\text{C}$.

WAVE SOLDERING

Wave soldering techniques can be used for all SO packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream end.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

REPAIRING SOLDERED JOINTS

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 $^{\circ}$ C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 $^{\circ}$ C.

Alignment-free multistandard vision and FM sound IF-PLL demodulator

TDA9880

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	

Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information

Where application information is given, it is advisory and does not form part of the specification.

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

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Printed in The Netherlands

545104/00/02/pp40

Date of release: 1998 Aug 12

Document order number: 9397 750 03888

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