Wireless Communications

GSM

Power and Flexibility in a Single Chip

OVERVIEW

The 1990's are witnessing the development of GSM as the leading worldwide cellular standard. Having achieved a worldwide leadership position, GSM is now evolving into multi-band solutions and into multi-mode systems in combination with other wireless technologies.

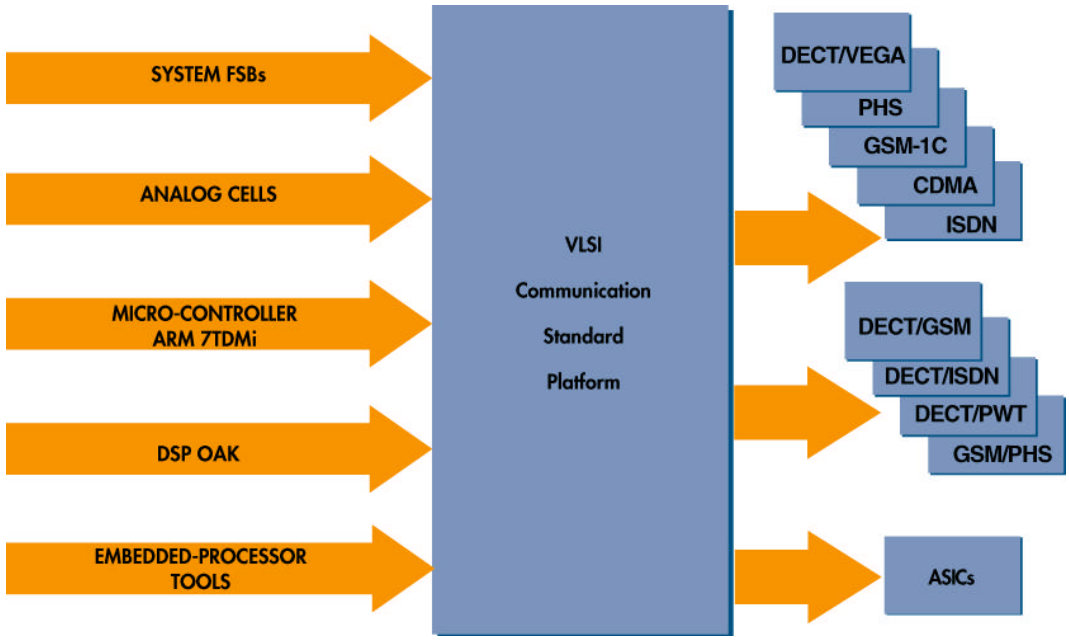
VLSI has maintained a leading market position since the early days of GSM as an ASIC and ASSP supplier to major GSM phone manufacturers. VLSI's major investment in building up GSM knowledge has resulted in an outstanding GSM competence, keeping us ahead of the competition as the leading edge technology provider in the wireless industry. VLSI's offerings go beyond traditional silicon products, ranging from specifically developed FSBs™ (Functional System Blocks) and DSP code up to a fully integrated, type-approved GSM chipset. After more than seven years' activity in the GSM market, developing our own technology as well as working with the standards bodies, VLSI silicon is now in 3 of every 10 phones sold in GSM.

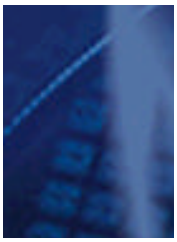
At an early stage, VLSI recognized the importance of integrating multiple future digital communication standards. For this reason, in parallel with our GSM development, we have made significant investments in DECT, PHS and CDMA technology. These strengths will allow VLSI to continue to play a leading role in the evolution of future communication platforms towards multi-band and multi- standard technologies such as UMTS and FPLMTS.

PROCESS TECHNOLOGY

Keeping one step ahead, VLSI has already moved all current GSM products to our industry-leading 0.35µm process technology. Coupled with an unmatched library of optimized cells and Functional System Blocks (FSB). This enables the company to meet the harsh expectations of overall cost reduction in the market at 20 to 30 percent per annum. In addition, migration to the latest silicon process, coupled with technical enhancements

VLSI Communication Standard Platform





and a reduction of the supply voltage to 2.7V, has cut typical idle-mode power consumption to less than 2mA. VLSI's process technology will allow further supply voltage reductions to 2.4V and 1.8V to optimize power consumption even more.
VLSI's long-standing design and process capabilities have allowed us to integrate full mixed-signal capabilities in our standard CMOS process. All our GSM ASSPs incorporate mixed-signal technology to implement the voice band analog front end (VBAFE) as well as RF front end interface. Thanks to this process advantage, we have been able to minimize the component count. By cutting back on interfaces, and providing a dedicated power control for each analog block, we have been able to reduce the system power consumption significantly.
At the same time, on a functional level, these circuits have enabled our customers to win various awards for best voice quality using the integrated VBAFE.

System-Level Silicon™

System-Level Silicon integrates increasingly complex system logic functions onto a smaller and smaller silicon footprint, reducing the size, power consumption and the cost of integrated circuits. The market now demands embedded processing power with Risc controllers and DSP engines. Wether in an ASSP or an ASIC, VLSI leads the field with its range of embedded processors and integrated analog interface cicuits, giving unrivaled system-level silicon.

Design Methodology

Common high-level hardware description languages (HDLs) used in VLSI's device design not only speed the design cycle but also permit rapid migration to new silicon process technologies, thus ensuring long-term competitiveness. Standardizing the design approach over a complete product range, as we have done with our GSM, DECT, PHS and CDMA products, delivers still greater advantages, allowing fast reaction to the future evolution and combinations of these standards. Furthermore, this design approach eases the design of derivative products, allowing custom ASSPs or ASICs to be produced by modifying key blocks or DSP code, or by combining standard design core blocks with customer-specified functions.

PROCESSOR CORES

ARM7TDMI Cores

The ARM7TDMI ("Thumb") includes a real time instruction decompression circuit which combines the advantages of the 32-bit RISC core with significantly increased code density and improved performance in systems based on 8-bit or 16-bit-wide memory. Supporting flexible system clocks, and with the ability to reduce clock rates to minimize power consumption in battery-powered applications, the ARM core spans a wide spectrum of performance and delivers sufficient processing power for future communication standards evolution. The core's processing power allows customer applications to run on the same processor as the communications protocol; these applications may range all the way from standard supplementary services up to a full PDA implementation.
VLSI is one of the founders of ARM Ltd. and is widely recognized for its unmatched application-specific ARM core optimization and integration skills as well as for its excellent support capability. Dedicated wireless ARM cores optimized for minimal power consumption are available. The full suite of libraries and design environments can be provided to allow quick design integration in customer products.

OAK DSP Core

Building on the success of DSP Technology's "Pine" digital signal processor core and serving as a stepping-stone towards future DSP cores, the Oak DSP core is rapidly becoming an industry standard in cellular applications. VLSI Technology implementation of the Oak core, the VVF3500, achieves 80MHz @3V (typical operating conditions). When coupled with appropriate hardware accelerator circuits such as our Viterbi co-processor, this level of processing power gives enough flexibility to carry out not only the standard-specific communication processing, but also supplementary functions typically needed in multimode phones as well as for customer-specific applications such as echo cancellation or speech recognition.

Multiprocessor System Design

To support application development around the ARM7TDMI-RISC and VVF3500 Oak DSP multi-core platform and to offer a low risk path to system design VLSI is offering an integrated development package including:

- Multiprocessor Development Chip (MDC)
  - Dual RISC/DSP cores running asynchronously on chip to provide a chip solution for system integration
- Multiprocessor Development Tools (MDT)
  - Complete software simulation/emulation development

kit which allows to test, analyze and modify the RISC/DSP code before the hardware is available
- Multiprocessor Development Platform (MDP)
- Flexible development board with JTAG port, prototyping area and Logic Analyzer support

Future Cores

Complementing the currently available processors, the powerful SH3 and SH4 cores—based on the VLSI-Hitachi licensing agreement—open up new horizons of performance.

GSM Chipset Offering

FEATURES

VWS22030 Voice-Coprocessor

- FR/EFR Voice coding
- Custom echo and noise suppression algorithm
- Asynchronous code & decode
- SE, CN, DTX, VAD, test
- Analog microphone and loudspeaker interface
- Low power
- Dedicated mode: 10mA @ 3V, 30mA in EFR mode
- Idle Mode: 30µA @3V

VP22003 Kernel Processor

- Complete peripheral set, SIM, UART and GPIOs
- Integrated FSC/CRC check for data application
- Battery management and charging control
- 144 TQFP package
- Fully integrated phase 2 data support (T/NT) 0.3-9.6Kbits/s
- Low power
- Dedicated: 20mA @ 3V
- Idle: <2mA @ 3V

GSM Software

- L1 software
- Fully documented and supported
- Software modules for transparent/Non-transparent data support.

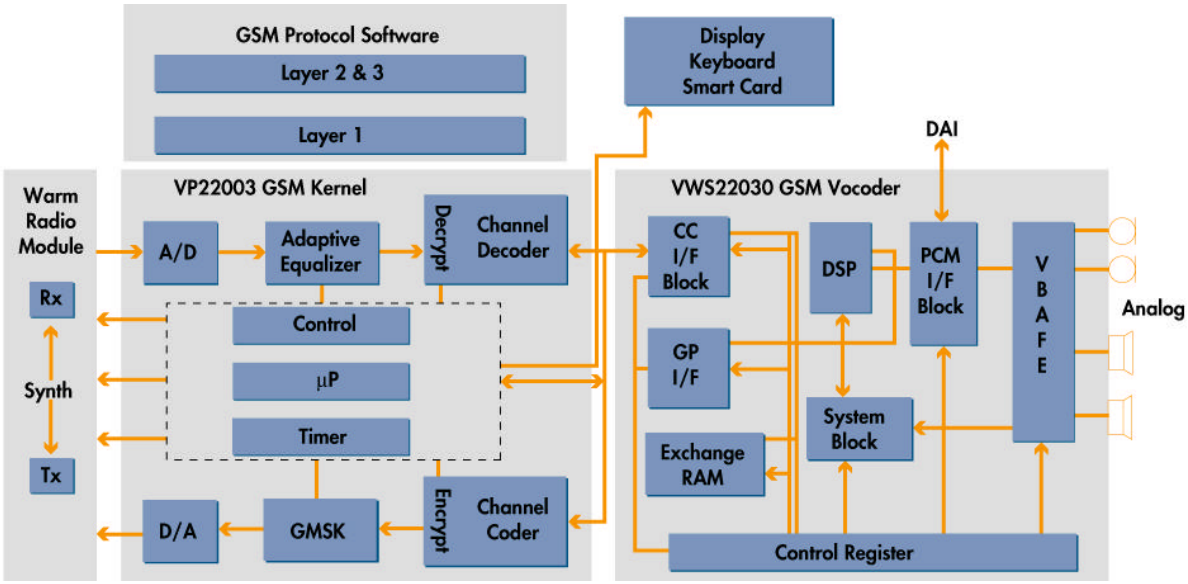
Type Approved GSM Chipset

VLSI today produces a fully type-approved two-chip GSM chipset, already integrated in a wide range of mobile phones. The chipset is partitioned into the "GSM Kernel" and the Vocoder (voice coding part). The GSM Kernel handles all the signalling and protocol stack handling as well as the external interface to the MMI.
The voice coding part is responsible for all the speech processing and the interface with the microphone and loudspeaker.

VP22003

The VP22003 GSM kernel processor is a direct, fully software-compatible evolution of the type-approved VP22002 device. The VP22003 uses VLSI's functional system block (FSB) technology with a 32-bit ARM RISC microcontroller. Even when operating at low frequency to minimize power consumption, the efficient ARM microcontroller delivers enough MIPS to run the full protocol stack, at the same time as a

TwoC-EFR 3V Solution



sophisticated Man/Machine Interface and full data functions. It supports full GSM Phase II data features (transparent/non-transparent data) without needing expensive external PCMCIA cards or other hardware coprocessors. The GSM kernel also offers an asynchronous data port, serial EEPROM port, 25-key keypad scanner and general-purpose I/O. Power management facilities permit low-power operation: standby mode consumption is typically less than 2mA at 3V.

VWS22030

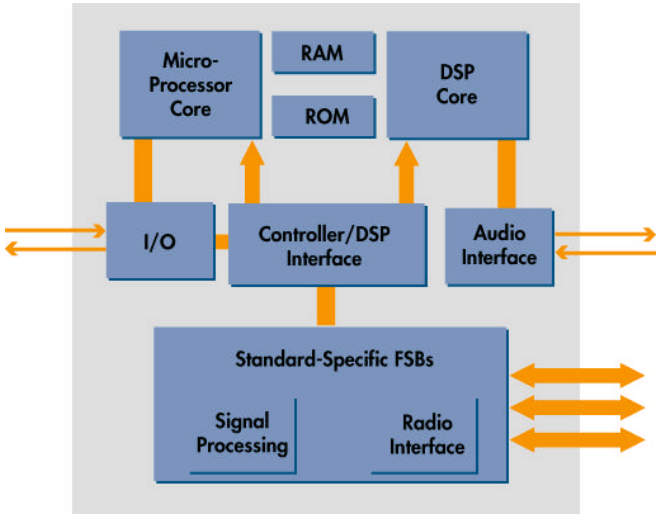
Operating at 3V ±10%, the VWS22030 IC combines the first-generation GSM Full Rate (FR) Vocoder function with the new Enhanced Full Rate (EFR) speech coding providing enhanced voice quality. Support of the new EFR voice codec is a key requirement for mobile phones to conform to the emerging US PCS1900 standard based on existing GSM technology. The new chip complies with all Phase II and 06 series GSM ETSI specification.
The integrated OAK DSP core provides sufficient processing power to support integrated noise and echo cancellation, eliminating the expensive external and coprocessors needed for today's hands-free kits.
The VWS22030, like its predecessor the VP22020, integrates mixed-signal circuitry such as a VBAFE (voice band analog front end) with which VLSI's GSM customers have already won awards for "Best Voice Quality" in previous models of GSM mobile phones.
The VWS22030 is also the first standard product in the GSM market to allow the customer such a wide range of customization capabilities for product feature differentiation. Previously, customers could only benefit from such features by investing significantly in time and technology for ASIC solutions.

Single Chip Communication Standard Platform OneC

OVERVIEW

Wireless markets have shown a significant growth, opening up tremendous development opportunities. But the dynamics of the market have also led to an intensely competitive environment similar to the consumer electronic marketplace. To succeed in these markets, companies need a reliable, innovative supplier who enables them to implement their differentiation ideas, ensuring competitiveness and profitability in the marketplace. Similarly, time to market is vital to allow quick product iterations.
The OneC platform approach is dedicated to support any future evolution of the GSM standard as well as combinations of future standards. But to allow customers to differentiate and

OneC Platform Architecture



succeed in a increasingly competitive market, the OneC platform architecture allows high-volume ASIC-like customization/adaptations at three levels:

- Customization based on additional on-circuit RAM into which custom DSP code can be downloaded from the system memory
- Metal-level ROM programmability of the GSM-1C product, allowing easy modification of the on-circuit ROM with custom DSP code
- Implemented using a high-level design language, the product is designed so that custom hardware blocks can easily be added to the design and existing blocks can be modified to match customer specifications.

OneC Platform

Based on the evolving standards, a clear trend is visible towards single chip architecture based around the ARM microcontroller and the OAK DSP core. The single chip architecture has the following key advantages:

- Higher design flexibility for customization
- First step to full multi-mode integration
- Power consumption, due to fewer interfaces
- Reduced number of components, easier manufacturing, cost reduction and yield improvement

The OneC provides a multi-standard platform. Common high-level hardware description languages (HDLs) used in device design speed the design cycle, but also permit rapid migration to new silicon process technologies to maintain long-term competitiveness. Still greater advantages occur as the design approach is standardized over a VLSI's complete product range, i.e. GSM, DECT, PHS and CDMA, allowing fast reaction to the future evolution and combinations of these standards. Such a standardized design approach will allow easy customization of standard products by modifying key blocks or DSP code but will also permit later ASIC derivatives of standard products by combining core blocks of the standard design with customer-specified functions.

Interprocessor Communication

The RISC and DSP cores work in synergy to make efficient use of the particular strengths of each processor. An efficient split of the processing tasks over the cores delivers a cost optimized solution as well as ensuring maximum flexibility. Such optimization is taken a stage further by a common bus interface which significantly reduces the pin count of the IC, while intelligent memory access technologies allow real-time download of different DSP software algorithms into on-chip fast memory depending on the moment-by-moment needs of the end user.

VLSI-WAVECOM Partnership

WM1-G900

Features System

- Licensed GSM Module
- Size: 64 x 46 x 8mm
- Target Handset Weight: <160g
- Performance
  - Talk Time: 1.5 to 3 hours
  - Standby Time: >40 hours
  - 550mAh batteries @4.8V

Baseband

- VLSI TwoC chipset consisting of VP22020 Vocoder and VP22002 GSM Kernel
- Embedded ARM processor
- Analog voice and radio interface
- Complete peripheral set, SIM, UART and GPIOs
- Battery management and charging control

GSM Radio Module

- Based on WARM RF chip of WAVECOM
- Full specification Class 4 GSM radio module
- Designed for easy manufacturing
- Only 0603 SMD components

GSM WAVECOM Software

- L1, L2, L3 & Core MMI
- Real time kernel
- Low memory requirements
  - 64Kbytes RAM
  - 256Kbytes ROM core SW
- Fully documented and supported

Performance

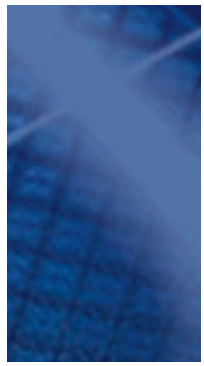
- Idle current consumption: 9-15mA @ 4.8V depending on frequency of paging frame occurrence
- Data services include transparent and non-transparent data at 0.3-9.6Kbit/s. ETSI compatible AT command set is used for interfacing.

VLSI-WAVECOM Cooperation

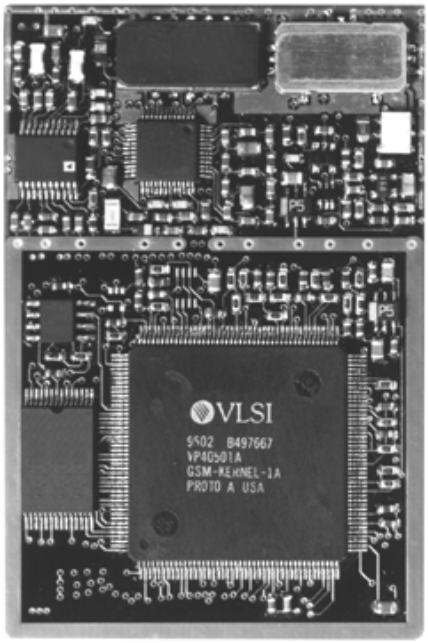
VLSI and Wavecom entered into cooperation with the objective of providing market-leading total solutions to the wireless market. The total solution concept includes BB, RF and SW design integrated into type-approved system design ready for manufacturing. The relationship between the companies allows continuous development of the BB, RF and SW portion to deliver an solution optimized in terms of cost, performance and size. The cooperation, which started in the field of GSM, will evolve to encompass other standards as well as multi-band and multi-mode solutions.

About WAVECOM

WAVECOM S.A., located in Issy-les-Moulineaux, France, was established in June 1993 to provide wireless system designs, product and systems for



WISMO GSM Module



WAVECOM
THE WIRELESS WORLD

radio communication markets.
WAVECOM's goal is to support equipment manufacturers in order to launch radio communication terminals on the market under the best possible conditions of cost and delay.
To this end, WAVECOM has developed its own technology for cellular phones (GSM , DCS1800, PCS1900), digital cordless telephones (CT2 & DECT), paging receivers (ERMES) and satellite mobile communication (ICO).

WISMO

The WISMO concept (WIreless Standard MOdule) is a generic concept fromWAVECOM developed in order to simplify the design of wireless terminals. Thefirst generation of module developed for GSM900 (referenced WM1-G900) has already obtained several FTAs and is today in volume production. The module allows handset development times which are unique in the market, at a highly competitive price level. The finished-product approach completely eliminates the widely known technical risk, and WISMO-based phones typically obtain FTA in less than 30 hours. WISMO's unique full data capability makes it very attractive for GSM-data-based services like PC/PDA mobility and other applications.

WAVECOM Offerings

The WAVECOM offering is based around the type-approved WISMO module. The WISMO offering includes three type of business models:

- Module supply
  - The module is supplied fully tested and tuned for direct integration into the end product
- Manufacturing license
  - All necessary elements for licensed manufacturing including test and manufacturing support are provided
- Technology license
  - Full technology access is provided on a system level for RF, BB and Software architecture

The Wavecom product offering is complemented by a wide range of customerservices which include type-approval services and engineering services up to the full product design.

Future Perspective

The current GSM 900 offering will be complemented with offerings for DCS1800 and PCS1900 by mid-1997. The range of offerings will be extended to cover multi-standard devices as well as multi-mode and multi-band solutions built around the basic GSM solutions at a later stage.

VLSI Technology

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