8Mx64 bit SDRAM Unbuffered DIMM F-Series

PC/100 SDRAM Specification Supporting
based on 8Mx8 SDRAM, LVTTL, 2/4-Banks & 4K/8KRefresh
HYM7V65800A/ HYM7V65801A/ HYM7V65830A/ HYM7V65A

DESCRIPTION

The HYM7V65800A/ 65801A/ 65830A/ 65831A F-Series are high speed 3.3-Volt synchronous dynamic RAM Modules composed of eight 8Mx8 bit Synchronous DRAMs in 54-pin TSOPII and 8-pin TSSOP 2K bit E^2PROM on a 168-pin glass-epoxy printed circuit board. A 0.33μF and 0.1μF decoupling capacitors per each SDRAM are mounted on the module.

The HYM7V65800A/ 65801A/ 65830A/ 65831A F-Series are gold plated socket type Dual In-line Memory Modules suitable for easy interchange and addition of 64M bytes memory. All addresses, data and control inputs are latched on the rising edge of the master clock input. The data paths are internally pipelined to achieve very high bandwidths.

FEATURES

- 1.375" (34.93mm) PCB Height
- 168-Pin Unbuffered DIMM with Single Sided
- One 0.33μF and one 0.1μF decoupling capacitors adopted
- Serial Presence Detect with Serial E^2PROM
- Meets all the other JEDEC specifications
- Single 3.3V±0.3V power supply
- All device pins are LVTTL compatible
- 4096 refresh cycles every 64ms or 8192 refresh cycles every 128ms
- Fully synchronous ; all inputs referenced to positive edge of system clock
- Dual or Quad internal banks with single pulsed /RAS
- Auto precharge/precharge all banks by A_{10} flag
- Possible to assert random column address every clock cycle
- Interleaved auto refresh mode
- Programmable burst lengths and sequences
- 1,2,4,8,full page for Sequential type
- 1,2,4,8 for Interleave type
- Programmable /CAS latency ; 2,3 clocks
- Support clock suspend/power down mode by CKE0
- Data mask function by DQM
- Mode register set programming
- Burst termination command
- Self refresh provides minimum power, full internal refresh control

ORDERING INFORMATION

Part No.	Max. Frequency	SDRAM Bank	Ref.	Package	Plating
HYM7V65800ATFG - 8/10P/10S	125/ 100/ 100 MHz	2 Banks	4K	TSOPII	Gold
HYM7V65801ATFG - 8/10P/10S	125/ 100/ 100 MHz	4 Banks	4K	TSOPII	Gold
HYM7V65830ATFG - 8/10P/10S	125/ 100/ 100 MHz	2 Banks	8K	TSOPII	Gold
HYM7V65831ATFG - 8/10P/10S	125/ 100/ 100 MHz	4 Banks	8K	TSOPII	Gold

BASED COMPONENTS

Module Part No.	Based Comp. Part No.	Module Part No.	Based Comp. Part No.
HYM7V65800ATFG	HY57V658010ATC	HYM7V65830ATFG	HY57V648010ATC
HYM7V65801ATFG	HY57V658020ATC	HYM7V65831ATFG	HY57V648020ATC

PIN DESCRIPTION

Pin Name	Pin Type	Description
CK0-CK3	INPUT	System Clock Input; All other inputs except CKE are registered to the SDRAM on the rising edge of CLK.
CKE0	INPUT	Clock Enable; Controls internal clock signal and when deactivated, the SDRAM will be either one of the states among power down, suspend, or self refresh.
/S0, /S2	INPUT	Chip select; Functions command mask(NOP).
/RAS	INPUT	Row address strobe
/CAS	INPUT	Column address strobe
/WE	INPUT	Write Enable
DQM0-7	INPUT	Data Input / Output Mask
DQ0-DQ63	INPUT/ OUTPUT	Data Input / Output; Include inputs, outputs, or Hi-z state.
V_{CC}	SUPPLY	Power Supplies; 3.3V±0.3V
V_{SS}	SUPPLY	Ground
SDA	INPUT/ OUTPUT	Serial Address and Data Input / Output.
SCL	INPUT	Serial Clock
SA0-SA2	INPUT	Addresses in Serial E^2PROM for Socket Presence.

HYM7V65800A/HYM7V65830A F-Series (2Bank 8Mx8 SDRAM Based)

Pin Name	Pin Type	Description
BA0	INPUT	Bank select address inputs; Select one of dual banks during both /RAS and /CAS activity.
A0-A12	INPUT	Address Inputs; A0-A8; X&Y addresses A10; Precharge flag, A9-A12; X addresses only.

HYM7V65801A/HYM7V65831A F-Series (4Bank 8Mx8 SDRAM Based)

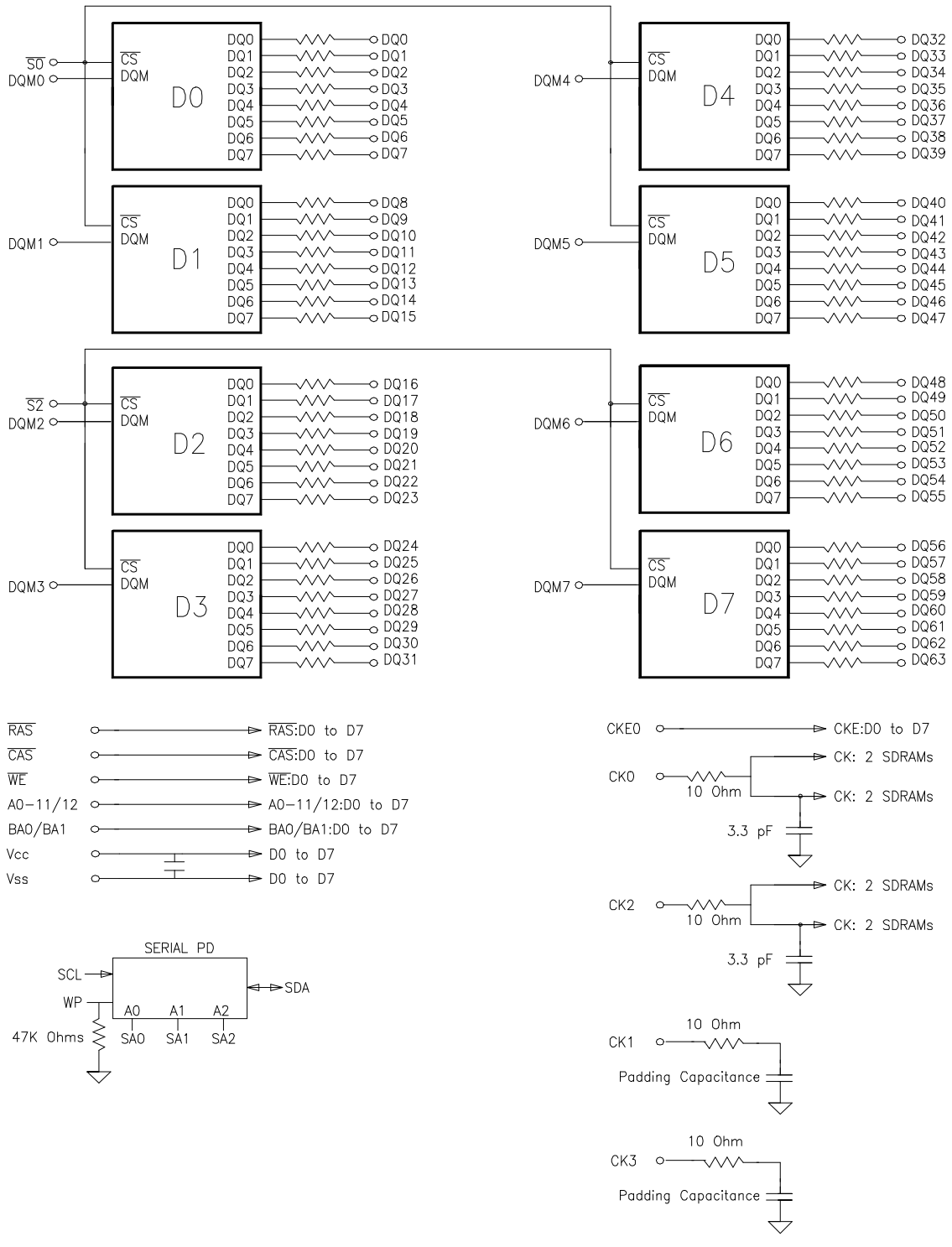
Pin Name	Pin Type	Description
BA0, BA1	INPUT	Bank address inputs; Select one of quad banks during both /RAS and /CAS activity.
A0-A11	INPUT	Address Inputs; A0-A8; X&Y addresses A10; Precharge flag, A9-A11; X addresses only.

PIN NAME

#	NAME	#	NAME	#	NAME	#	NAME
1	Vss	43	Vss	85	Vss	127	Vss
2	DQ0	44	NC	86	DQ32	128	CKE0
3	DQ1	45	/S2	87	DQ33	129	NC
4	DQ2	46	DQM2	88	DQ34	130	DQM6
5	DQ3	47	DQM3	89	DQ35	131	DQM7
6	Vcc	48	NC	90	Vcc	132	NC
7	DQ4	49	Vcc	91	DQ36	133	Vcc
8	DQ5	50	NC	92	DQ37	134	NC
9	DQ6	51	NC	93	DQ38	135	NC
10	DQ7	52	NC	94	DQ39	136	NC
11	DQ8	53	NC	95	DQ40	137	NC
12	Vss	54	Vss	96	Vss	138	Vss
13	DQ9	55	DQ16	97	DQ41	139	DQ48
14	DQ10	56	DQ17	98	DQ42	140	DQ49
15	DQ11	57	DQ18	99	DQ43	141	DQ50
16	DQ12	58	DQ19	100	DQ44	142	DQ51
17	DQ13	59	Vcc	101	DQ45	143	Vcc
18	Vcc	60	DQ20	102	Vcc	144	DQ52
19	DQ14	61	NC	103	DQ46	145	NC
20	DQ15	62	NC	104	DQ47	146	NC
21	NC	63	NC	105	NC	147	NC
22	NC	64	Vss	106	NC	148	Vss
23	Vss	65	DQ21	107	Vss	149	DQ53
24	NC	66	DQ22	108	NC	150	DQ54
25	NC	67	DQ23	109	NC	151	DQ55
26	Vcc	68	Vss	110	Vcc	152	Vss
27	/WE	69	DQ24	111	/CAS	153	DQ56
28	DQM0	70	DQ25	112	DQM4	154	DQ57
29	DQM1	71	DQ26	113	DQM5	155	DQ58
30	/S0	72	DQ27	114	NC	156	DQ59
31	NC	73	Vcc	115	/RAS	157	Vcc
32	Vss	74	DQ28	116	Vss	158	DQ60
33	A0	75	DQ29	117	A1	159	DQ61
34	A2	76	DQ30	118	A3	160	DQ62
35	A4	77	DQ31	119	A5	161	DQ63
36	A6	78	Vss	120	A7	162	Vss
37	A8	79	CK2	121	A9	163	*CK3
38	A10(AP)	80	NC	122	BA0	164	NC
39	* BA1	81	WP	123	A11	165	SA0
40	Vcc	82	SDA	124	Vcc	166	SA1
41	Vcc	83	SCL	125	*CK1	167	SA2
42	CK0	84	Vcc	126	* A12	168	Vcc

Note : 1. BA1 is used for HYM7V65801A/HYM7V65831A F-Series (4 Bank 8Mx8 Based)
2. A12 is used for HYM7V65800A/HYM7V65830A F-Series (2 Bank 8Mx8 Based)
3. CK1 and CK3 are connected with termination R/C (Refer to the block diagram)

BLOCK DIAGRAM



Note : 1. The serial resistor values of DQs are 10 Ohms.

2. The padding capacitance of termination R/C for CK1/3 is 10pF.

I-1 SERIAL PRESENCE DETECT

[HYM7V65800A/HYM7V65830A F-Series; 2 Banks]

BYTE NUMBER	FUNCTION DESCRIBED	FUNCTION -8	FUNCTION -10P	FUNCTION -10S	VALUE -8	VALUE -10P	VALUE -10S	NOTE
BYTE0	# of Bytes Written into Serial Memory at Module Manufacturer	128 Bytes			80h			
BYTE1	Total # of Bytes of SPD Memory Device	256 Bytes			08h			
BYTE2	Fundamental Memory Type	SDRAM			04h			
BYTE3	# of Row Addresses on This Assembly	2 Banks; 13			0Dh			1
BYTE4	# of Column Addresses on This Assembly	9			09h			
BYTE5	# of Module Banks on This Assembly	1 Bank			01h			
BYTE6	Data Width of This Assembly	64 Bits			40h			
BYTE7	Data Width of This Assembly (Continued)	-			00h			
BYTE8	Voltage Interface Standard of This Assembly	LVTTL			01h			
BYTE9	SDRAM Cycle Time @ /CAS Latency=3	8ns	10ns	10ns	80h	A0h	A0h	
BYTE10	Access Time from Clock @ /CAS Latency=3	6ns	6ns	6ns	60h	60h	60h	
BYTE11	DIMM Configuration Type	None			00h			
BYTE12	Refresh Rate/Type	15.625µs / Self Refresh Supported			80h			
BYTE13	Primary SDRAM Width	x8			08h			
BYTE14	Error Checking SDRAM Width	None			00h			
BYTE15	Minimum Clock Delay Back to Back Random Column Address	t_{CCD}=1 Latency			01h			
BYTE16	Burst Lengths Supported	1,2,4,8,Full Page			8Fh			2
BYTE17	# of Banks on SDRAM Device	2 Banks			02h			
BYTE18	CAS # Latency	/CAS Latency=2,3			06h			
BYTE19	CS # Latency	/CS Latency=0			01h			
BYTE20	Write Latency	/WE Latency=0			01h			
BYTE21	SDRAM Module Attributes	Neither Buffered nor Registered			00h			
BYTE22	SDRAM Module Attributes, General	+/-10% voltage tolerance, Burst read, Precharge all, Auto precharge			06h			
BYTE23	SDRAM Cycle Time @ /CAS Latency=2	10ns	10ns	12ns	A0h	A0h	C0h	
BYTE24	Access Time from Clock @ /CAS Latency=2	6ns	6ns	6ns	60h	60h	60h	
BYTE25	SDRAM Cycle Time @ /CAS Latency=1	-	-	-	00h	00h	00h	
BYTE26	Access Time from Clock @ /CAS Latency=1	-	-	-	00h	00h	00h	
BYTE27	Minimum Row Precharge Time (t_{RP})	20ns	20ns	20ns	14h	14h	14h	
BYTE28	Minimum Row Active to Row Active Delay (t_{RRD})	16ns	20ns	20ns	10h	14h	14h	
BYTE29	Minimum /RAS to /CAS Delay (t_{RCD})	20ns	20ns	20ns	14h	14h	14h	
BYTE30	Minimum /RAS Pulse width (t_{RAS})	48ns	50ns	50ns	30h	32h	32h	
BYTE31	Module Bank Density	64MB			10h			
BYTE32	Command & Address signal input setup time (t_{AS})	2ns	2ns	2ns	20h	20h	20h	
BYTE33	Command & Address signal input hold time (t_{AH})	1ns	1ns	1ns	10h	10h	10h	
BYTE34	Data signal input setup time (t_{DS})	2ns	2ns	2ns	20h	20h	20h	
BYTE35	Data signal input hold time (t_{DH})	1ns	1ns	1ns	10h	10h	10h	

I-2 SERIAL PRESENCE DETECT [HYM7V65800A/HYM7V65830A F-Series; 2 Banks: Continued]

BYTE NUMBER	FUNCTION DESCRIBED	FUNCTION -8	FUNCTION -10P	FUNCTION -10S	VALUE -8	VALUE -10P	VALUE -10S	NOTE
BYTE36 -61	Superset Information(May be used in the future)	-			00h			
BYTE62	SPD Revision	Intel SPD 1.2A			12h			4, 5
BYTE63	Checksum for Byte 0-62				D6h	FCh	1Ch	
BYTE64	Manufacturer JEDEC ID Code	Hyundai JEDEC ID			ADh			
BYTE65 -71	….Manufacturer JEDEC ID Code	Unused			FFh			
BYTE72	Manufacturing Location	HEI (Korea) HEA (United States) HEU (Europe)			01h 02h 03h			
BYTE73	Manufacturer's Part Number (SDRAM)	7			37h			6
BYTE74	Manufacturer's Part Number (3.3V)	V			56h			6
BYTE75	Manufacturer's Part Number (Data Width)	6			36h			6
BYTE76	….Manufacturer's Part Number (Data Width)	5			35h			6
BYTE77	Manufacturer's Part Number (Memory Depth)	8			38h			6
BYTE78	Manufacturer's Part Number (Refresh)	0 (4K Ref.) 3 (8K Ref.)			30h 33h			6
BYTE79	Manufacturer's Part Number (2 Internal Banks)	0			30h			6
BYTE80	Manufacturer's Part Number (Generation)	A			41h			6
BYTE81	Manufacturer's Part Number (TSOPII Mounted)	T			54h			6
BYTE82	Manufacturer's Part Number (x8 Unbuffered)	F			46h			6
BYTE83	Manufacturer's Part Number (Plating Type : Gold)	G			47h			6
BYTE84	Manufacturer's Part Number (Hyphen)	-			2Dh			6
BYTE85	Manufacturer's Part Number (Min. Cycle Time)	8	1	1	38h	31h	31h	6
BYTE86	….Manufacturer's Part Number (Min. Cycle Time)	Blank	0	0	20h	30h	30h	6
BYTE87	….Manufacturer's Part Number (Min. Cycle Time)	Blank	P	S	20h	50h	53h	6
BYTE88 -90	Manufacturer's Part Number	Blanks			20h			6
BYTE91	Revision Code for Components	Process Code			-			3, 6
BYTE92	….Revision Code for PCB	Process Code			-			3, 6
BYTE93	Manufacturing Date	Work Week			-			3, 5
BYTE94	….Manufacturing Date	Year			-			3, 5
BYTE95 -98	Assembly Serial Number	-			-			3
BYTE99 -125	Manufacturer Specific Data (May be used in the Future)	None			00h			
BYTE126	System Frequency support	100MHz			64h			4
BYTE127	Intel Specification details for 100MHz Support	Note 7			A7h	A7h	A5h	4
BYTE128 -256	Unused storage locations	-			00h			

Note: 1. The bank address is excluded. 2. In interleaved type, the burst lengths supported is 1, 2, 4, 8.
3. Not fixed but dependent. 4. Refer to Intel SPD 1.2A specifications.
5. BCD adopted. 6. ASCII adopted.
7. CLK0,2 connected to the DIMM, TBD junction temp, CL=2(3) support and supporting Intel defined Concurrent Auto Precharge.

II-1 SERIAL PRESENCE DETECT

[HYM7V65801A/HYM7V65831A F-Series; 4 Banks]

BYTE NUMBER	FUNCTION DESCRIBED	FUNCTION			VALUE			NOTE
		-8	-10P	-10S	-8	-10P	-10S	
BYTE0	# of Bytes Written into Serial Memory at Module Manufacturer	128 Bytes			80h			
BYTE1	Total # of Bytes of SPD Memory Device	256 Bytes			08h			
BYTE2	Fundamental Memory Type	SDRAM			04h			
BYTE3	# of Row Addresses on This Assembly	4 Banks; 12			0Ch			1
BYTE4	# of Column Addresses on This Assembly	9			09h			
BYTE5	# of Module Banks on This Assembly	1 Bank			01h			
BYTE6	Data Width of This Assembly	64 Bits			40h			
BYTE7	Data Width of This Assembly (Continued)	-			00h			
BYTE8	Voltage Interface Standard of This Assembly	LVTTL			01h			
BYTE9	SDRAM Cycle Time @ /CAS Latency=3	8ns	10ns	10ns	80h	A0h	A0h	
BYTE10	Access Time from Clock @ /CAS Latency=3	6ns	6ns	6ns	60h	60h	60h	
BYTE11	DIMM Configuration Type	None			00h			
BYTE12	Refresh Rate/Type	15.625µs / Self Refresh Supported			80h			
BYTE13	Primary SDRAM Width	x8			08h			
BYTE14	Error Checking SDRAM Width	None			00h			
BYTE15	Minimum Clock Delay Back to Back Random Column Address	t_{CCD}=1 Latency			01h			
BYTE16	Burst Lengths Supported	1,2,4,8,Full Page			8Fh			2
BYTE17	# of Banks on SDRAM Device	4 Banks			04h			
BYTE18	CAS # Latency	/CAS Latency=2,3			06h			
BYTE19	CS # Latency	/CS Latency=0			01h			
BYTE20	Write Latency	/WE Latency=0			01h			
BYTE21	SDRAM Module Attributes	Neither Buffered nor Registered			00h			
BYTE22	SDRAM Module Attributes, General	+/-10% voltage tolerance, Burst read, Precharge all, Auto precharge			06h			
BYTE23	SDRAM Cycle Time @ /CAS Latency=2	10ns	10ns	12ns	A0h	A0h	C0h	
BYTE24	Access Time from Clock @ /CAS Latency=2	6ns	6ns	6ns	60h	60h	60h	
BYTE25	SDRAM Cycle Time @ /CAS Latency=1	-	-	-	00h	00h	00h	
BYTE26	Access Time from Clock @ /CAS Latency=1	-	-	-	00h	00h	00h	
BYTE27	Minimum Row Precharge Time (t_{RP})	20ns	20ns	20ns	14h	14h	14h	
BYTE28	Minimum Row Active to Row Active Delay (t_{RRD})	16ns	20ns	20ns	10h	14h	14h	
BYTE29	Minimum /RAS to /CAS Delay (t_{RCD})	20ns	20ns	20ns	14h	14h	14h	
BYTE30	Minimum /RAS Pulse width (t_{RAS})	48ns	50ns	50ns	30h	32h	32h	
BYTE31	Module Bank Density	64MB			10h			
BYTE32	Command & Address signal input setup time (t_{AS})	2ns	2ns	2ns	20h	20h	20h	
BYTE33	Command & Address signal input hold time (t_{AH})	1ns	1ns	1ns	10h	10h	10h	
BYTE34	Data signal input setup time (t_{DS})	2ns	2ns	2ns	20h	20h	20h	
BYTE35	Data signal input hold time (t_{DH})	1ns	1ns	1ns	10h	10h	10h	

II-2 SERIAL PRESENCE DETECT [HYM7V65801A/HYM7V65831A F-Series; 4 Banks: Continued]

BYTE NUMBER	FUNCTION DESCRIBED	FUNCTION -8	FUNCTION -10P	FUNCTION -10S	VALUE -8	VALUE -10P	VALUE -10S	NOTE
BYTE36 -61	Superset Information(May be used in the future)	-			00h			
BYTE62	SPD Revision	Intel SPD 1.2A			12h			4, 5
BYTE63	Checksum for Byte 0-62				D7h	FDh	1Dh	
BYTE64	Manufacturer JEDEC ID Code	Hyundai JEDEC ID			ADh			
BYTE65 -71	….Manufacturer JEDEC ID Code	Unused			FFh			
BYTE72	Manufacturing Location	HEI (Korea) HEA (United States) HEU (Europe)			01h 02h 03h			
BYTE73	Manufacturer's Part Number (SDRAM)	7			37h			6
BYTE74	Manufacturer's Part Number (3.3V)	V			56h			6
BYTE75	Manufacturer's Part Number (Data Width)	6			36h			6
BYTE76	….Manufacturer's Part Number (Data Width)	5			35h			6
BYTE77	Manufacturer's Part Number (Memory Depth)	8			38h			6
BYTE78	Manufacturer's Part Number (Refresh)	0 (4K Ref.) 3 (8K Ref.)			30h 33h			6
BYTE79	Manufacturer's Part Number (4 Internal Banks)	1			31h			6
BYTE80	Manufacturer's Part Number (Generation)	A			41h			6
BYTE81	Manufacturer's Part Number (TSOPII Mounted)	T			54h			6
BYTE82	Manufacturer's Part Number (x8 Unbuffered)	F			46h			6
BYTE83	Manufacturer's Part Number (Plating Type : Gold)	G			47h			6
BYTE84	Manufacturer's Part Number (Hyphen)	-			2Dh			6
BYTE85	Manufacturer's Part Number (Min. Cycle Time)	8	1	1	38h	31h	31h	6
BYTE86	….Manufacturer's Part Number (Min. Cycle Time)	Blank	0	0	20h	30h	30h	6
BYTE87	….Manufacturer's Part Number (Min. Cycle Time)	Blank	P	S	20h	50h	53h	6
BYTE88 -90	Manufacturer's Part Number	Blanks			20h			6
BYTE91	Revision Code for Components	Process Code			-			3, 6
BYTE92	….Revision Code for PCB	Process Code			-			3, 6
BYTE93	Manufacturing Date	Work Week			-			3, 5
BYTE94	….Manufacturing Date	Year			-			3, 5
BYTE95 -98	Assembly Serial Number	-			-			3
BYTE99 -125	Manufacturer Specific Data (May be used in the Future)	None			00h			
BYTE126	System Frequency support	100MHz			64h			4
BYTE127	Intel Specification details for 100MHz Support	Note 7			A7h	A7h	A5h	4
BYTE128 -256	Unused storage locations	-			00h			

Note: 1. The bank address is excluded. 2. In interleaved type, the burst lengths supported is 1, 2, 4, 8.
3. Not fixed but dependent. 4. Refer to Intel SPD 1.2A specifications.
5. BCD adopted. 6. ASCII adopted.
7. CLK0,2 connected to the DIMM, TBD junction temp, CL=2(3) support and supporting Intel defined Concurrent Auto Precharge.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Rating	Unit
T_A	Ambient Temperature	0 to 70	°C
T_{STG}	Storage Temperature	-55 to 125	°C
V_{IN}, V_{OUT}	Voltage on Any Pin relative to V_{SS}	-1.0 to 4.6	V
V_{CC}	Voltage on V_{CC} relative to V_{SS}	-1.0 to 4.6	V
I_{OS}	Short Circuit Output Current	50	MA
P_D	Power Dissipation	8	W
T_{SOLDER}	Soldering Temperature·Time	260·10	°C·sec

Note : Operation at above Absolute Maximum Ratings can adversely affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS* (T_A=0°C to 70°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Note
V_{CC}, V_{CCQ}	Power Supply Voltage	3.0	3.3	3.6	V	
Vss	Power Supply Voltage	0	0	0	V	
V_{IH}	Input High Voltage	2.0	3.0	V_{CC} + 0.4	V	1
V_{IL}	Input Low Voltage	-0.3	0	0.8	V	2

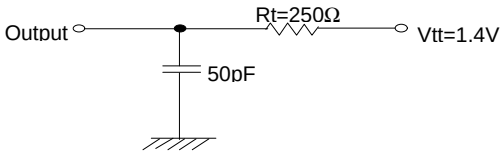
Note : 1. V_{IH}(max)=4.6V AC for pulse width ≤10ns acceptable.
2. V_{IL}(min)=-1.5V AC for pulse width ≤10ns acceptable.

RECOMMENDED AC OPERATING CONDITIONS* (T_A=0°C to 70°C, V_{CC}=3.3V±10%, V_{SS}=0V)

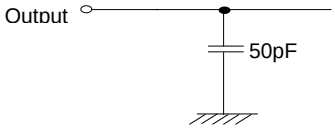
Symbol	Parameter	Value	Unit	Note
V_{IH} / V_{IL}	AC Input High/Low Level Voltage	2.4/0.4	V	
Vtrip	Input Timing Measurement Reference Level Voltage	1.4	V	
Tr / tf	Input Rise/Fall Time	1	ns	
Voutref	Output Reference Voltage	1.4	V	
C_L	Output Load Capacitance for Access Time Measurement	50	pF	

Note : Output load to measure access times is equivalent to two TTL gates and one capacitance(50pF).

Note : * DC Output Load Circuit



AC Output Load Circuit



DC CHARACTERISTICS(I)

(T_A=0°C to 70°C, V_{CC}=3.3V±10%, V_{SS}=0V)

Symbol	Parameter	Test Condition	Min.	Max.	Unit
I_{LI}	Input Leakage Current	V_I=0 to 3.6V, All other pins not undertest=0V	-8	8	μA
I_{LO}	Output Leakage Current	D_{OUT} is disabled, V_O=0 to 3.6V	-1	1	μA
V_{OL}	Output Low Voltage	I_{OL}=4.0mA	-	0.4	V
V_{OH}	Output High Voltage	I_{OH}=-4.0mA	2.4	-	V

DC CHARACTERISTICS(II)

(T_A=0°C to 70°C, V_{CC}=3.3V±10%, V_{SS}=0V)

Parameter	Symbol	Test Condition			Max.	Unit	Note
Operating current	I_{CC1}	Burst Length=1, One bank active t_{RAS}≥t_{RAS}(min), t_{RP}≥t_{RP}(min), I_O=0mA		-8	920	mA	1
				-10P	800		
				-10S	800		
Precharge Standby Current in Power Down Mode	I_{CC2P}	CKE≤V_{IL}(max), tCK=15ns			16	mA	
	I_{CC2PS}	CKE≤V_{IL}(max), tCK= ∞			16		
Precharge Standby Current in Non Power Down Mode	I_{CC2N}	CKE≥V_{IL}(min), /CS≥ V_{IL}(min), t_{CK}=15ns Input signals are chaged one time during 30ns. All other pins≥V_{DD}-0.2V or ≤0.2V			120	mA	
	I_{CC2NS}	CKE≥V_{IL}(min), t_{CK}= ∞ Input signals are stable			120		
Active Standby Current in Power Down Mode	I_{CC3P}	CKE≤V_{IL}(max), tCK=15ns			40	mA	
	I_{CC3PS}	CKE≤V_{IL}(max), tCK= ∞			40		
Active Standby Current in Non Power Down Mode	I_{CC3N}	CKE≥V_{IL}(min), /CS≥ V_{IL}(min), t_{CK}=15ns Input signals are chaged one time during 30ns. All other pins≥V_{DD}-0.2V or ≤0.2V			280	mA	
	I_{CC3NS}	CKE≥V_{IL}(min), t_{CK}= ∞ Input signals are stable			280		
Burst Mode Operating Current	I_{CC4}	t_{CK}≥ t_{CK}(min), t_{RAS}≥t_{RAS}(min), I_O=0mA All banks active	CL=3	-8	880	mA	1
				-10P	800		
				-10S	8000		
			CL=2	-8	720		
				-10P	560		
				-10S	560		
Auto Refresh Current	I_{CC5}	t_{RRC}≥t_{RRC}(min), All banks active			1600	mA	2
Self Refresh Current	I_{CC6}	CKE≤0.2V			16	mA	

Note :
1. I_{CC1} and I_{CC4} depend on output loading and cycle rates. Specified values are measured with the output open.
2. Minimum of t_{RRC}(Refresh /RAS cycle time)=96ns

AC CHARACTERISTICS I

Parameter		Symbol	-8		-10P		-10S		Unit	Note
			Min	Max	Min	Max	Min	Max		
System clock cycle time	CL=3	t_{CK3}	8	1000	10	1000	10	1000	ns	
	CL=2	t_{CK2}	10		10		10		ns	
Clock high pulse width		t_{CHW}	3	-	3	-	3	-	ns	1
Clock low pulse width		t_{CLW}	3	-	3	-	3	-	ns	1
Access time from clock	CL=3	t_{AC3}	-	6	-	6	-	6	ns	2
	CL=2	t_{AC2}	-	6	-	6	-	6	ns	2
Data-Out hold time		t_{OH}	3	-	3	-	3	-	ns	2
Data-Input setup time		t_{DS}	2	-	2	-	2	-	ns	1
Data-Input hold time		t_{DH}	1	-	1	-	1	-	ns	1
Address setup time		t_{AS}	2	-	2	-	2	-	ns	1
Address hold time		t_{AH}	1	-	1	-	1	-	ns	1
CKE setup time		t_{CKS}	2	-	2	-	2	-	ns	1
CKE hold time		t_{CKH}	1	-	1	-	1	-	ns	1
Command setup time		t_{CS}	2	-	2	-	2	-	ns	1
Command hold time		t_{CH}	1	-	1	-	1	-	ns	1
CLK to data output in low Z-time		t_{OLZ}	1	-	1	-	1	-	ns	2
CLK to data output in high Z-time	CL=3	t_{OHZ3}	3	9	3	9	3	9	ns	
	CL=2	t_{OHZ2}	3	9	3	9	3	9	ns	

Note : 1. Assumed input rise and fall time (t_R / t_F) is 1ns. If t_R & t_F is longer than 1ns, transient time compensation should be considered. i.e., [(t_R+t_F)/2-1]ns should be added to the parameter.
2. If clock rising time is longer than 1ns, (t_R/2-0.5)ns should be added to the parameter.

AC CHARACTERISTICS II

Parameter		Symbol	-8		-10P		-10S		Unit	Note
			Min	Max	Min	Max	Min	Max		
/RAS cycle time	Operation	t_{RC}	70	-	70	-	70	-	ns	
	Auto Refresh	t_{RRC}	70	-	70	-	70	-	ns	
/RAS to /CAS delay		t_{RCD}	20	-	20	-	20	-	ns	
/RAS active time		t_{RAS}	48	100K	50	100K	50	100K	ns	
/RAS precharge time		t_{RP}	20	-	20	-	20	-	ns	
/RAS to /RAS bank active delay		t_{RRD}	16	-	20	-	20	-	ns	
/CAS to /CAS delay		t_{CCD}	1	-	1	-	1	-	CLK	
Write command to data-in delay		t_{WTL}	0	-	0	-	0	-	CLK	
Data-in to precharge command		t_{DPL}	1	-	1	-	1	-	CLK	
Data-in to active command		t_{DAL}	4	-	4	-	4	-	CLK	
DQM to data-out Hi-Z		t_{DQZ}	2	-	2	-	2	-	CLK	
DQM to data-in mask		t_{DQM}	0	-	0	-	0	-	CLK	
MRS to new command		t_{MRD}	2	-	2	-	2	-	CLK	
Precharge to data output Hi-Z	CL=3	t_{PROZ3}	3	-	3	-	3	-	CLK	
	CL=2	t_{PROZ2}	2	-	2	-	2	-	CLK	
Power down exit time		t_{PDE}	1	-	1	-	1	-	CLK	
Self refresh exit time		t_{SRE}	1	-	1	-	1	-	CLK	1
Refresh time	4K	t_{REF}	64	-	64	-	64	-	ms	
	8K		128	-	128	-	128	-		

Note : 1. A new command can be given t_{RRC} after self refresh exit.

CAPACITANCE

(T_A=25°C, f=1MHz)

Symbol	Parameter	Pin	Typ.	Max.	Unit
C_{IN1}	Input Capacitance	A0-A11/12, BA0/BA1	-	60	pF
C_{IN2}	Input Capacitance	/RAS, /CAS, /WE	-	60	pF
C_{IN3}	Input Capacitance	/S0, /S2	-	35	pF
C_{IN4}	Input Capacitance	CK0, CK2	-	40	pF
C_{IN5}	Input Capacitance	CKE0		55	pF
C_{IN6}	Input Capacitance	DQM0-DQM7	-	20	pF
C_{OUT}	Output Capacitance	DQ0-DQ63	-	15	pF

MODULE OPERATING OPTION TABLE

HYM7V65800/801/830/831ATFG-8

	/CAS Latency	t_{RCD}	t_{RAS}	t_{RC}	t_{RP}	t_{AC}	t_{OH}
125MHz	3CLKs	3CLKs	6CLKs	9CLKs	3CLKs	6ns	3ns
100MHz	2CLKs	2CLKs	5CLKs	7CLKs	2CLKs	6ns	3ns
83MHz	2CLKs	2CLKs	4CLKs	6CLKs	2CLKs	6ns	3ns
66MHz	2CLKs	2CLKs	4CLKs	5CLKs	2CLKs	6ns	3ns

HYM7V65800/801/830/831ATFG-10P

	/CAS Latency	t_{RCD}	t_{RAS}	t_{RC}	t_{RP}	t_{AC}	t_{OH}
100MHz	2CLKs	2CLKs	5CLKs	7CLKs	2CLKs	6ns	3ns
83MHz	2CLKs	2CLKs	5CLKs	6CLKs	2CLKs	6ns	3ns
66MHz	2CLKs	2CLKs	4CLKs	5CLKs	2CLKs	6ns	3ns
50MHz	2CLKs	1CLKs	3CLKs	4CLKs	1CLKs	6ns	3ns

HYM7V65800/801/830/831ATFG-10S

	/CAS Latency	t_{RCD}	t_{RAS}	t_{RC}	t_{RP}	t_{AC}	t_{OH}
100MHz	3CLKs	2CLKs	5CLKs	7CLKs	2CLKs	6ns	3ns
83MHz	2CLKs	2CLKs	5CLKs	6CLKs	2CLKs	6ns	3ns
66MHz	2CLKs	2CLKs	4CLKs	5CLKs	2CLKs	6ns	3ns
50MHz	2CLKs	1CLKs	3CLKs	4CLKs	1CLKs	6ns	3ns

COMMAND TRUTH TABLE

Command		CKEn-1	CKEn	/CS	/RAS	/CAS	/WE	DQM	ADDR	A10/ AP	BA	Note
Mode Register set		H	X	L	L	L	L	X	OP code			1, 2
No Operation		H	X	H	X	X	X	X	X			
				L	H	H	H					
Bank Active		H	X	L	L	H	H	X	RA		V	
Read		H	X	L	H	L	H	X	CA	L	V	4
Read with Autoprecharge										H		4, 5
Write		H	X	L	H	L	L	X	CA	L	V	4
Write with Autoprecharge										H		4, 5
Precharge All baknks		H	X	L	L	H	L	X	X	L	X	
Precharge selected bank										H	V	
Burst Stop		H	X	L	H	H	L	X	X			6
DQM		H	X					V	X			7
Auto Refresh		H	H	L	L	L	H	X	X			3
Self Refresh	Entry	H	L	L	L	L	H	X	X			3
	Exit	L	H	H	X	X	X	X				3
				L	H	H	H					
Precharge Power down	Entry	H	L	H	X	X	X	X	X			
				L	H	H	H					
	Exit	L	H	H	X	X	X	X				
				L	H	H	H					
Clock Suspend	Entry	H	L	H	X	X	X	X	X			
	Exit	L	H	X				X				

(V=Valid, X=Don't care, H=Logic High, L=Logic Low)

Note: 1. OP code : Operand Code. ADDR, A10/AP, BA : Program keys (@MRS)
2.MRS can be issued only at both banks precharge state.
A new command can be issued after 2CLK cycles of MRS.
3. Auto refresh functions are as same as CBR refresh of DRAM
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at both banks precharge state.
4. BA : Bank select address.
If "Low" at read, write, row active and precharge, Bank A is selected.
If "High" at read, write, row active and precharge, Bank B is selected.
If A10/AP is "High" at row precharge, BA is ignored and both banks are selected.
5. During burst read or write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the associated bank can be issued at t_{RP} after the end of burst.
6. Burst stop command is valid at every burst length.
7. DQM sampled at positive going edge of a CLK masks the data-in at the very CLK (write DQM
Latency is 0), but makes Hi-Z state the data-out of 2CLK cycles after. (Read DQM latency is 2)

PACKAGE DIMENSION