SED1606D0A/D0B

CMOS LCD SEGMENT DRIVER

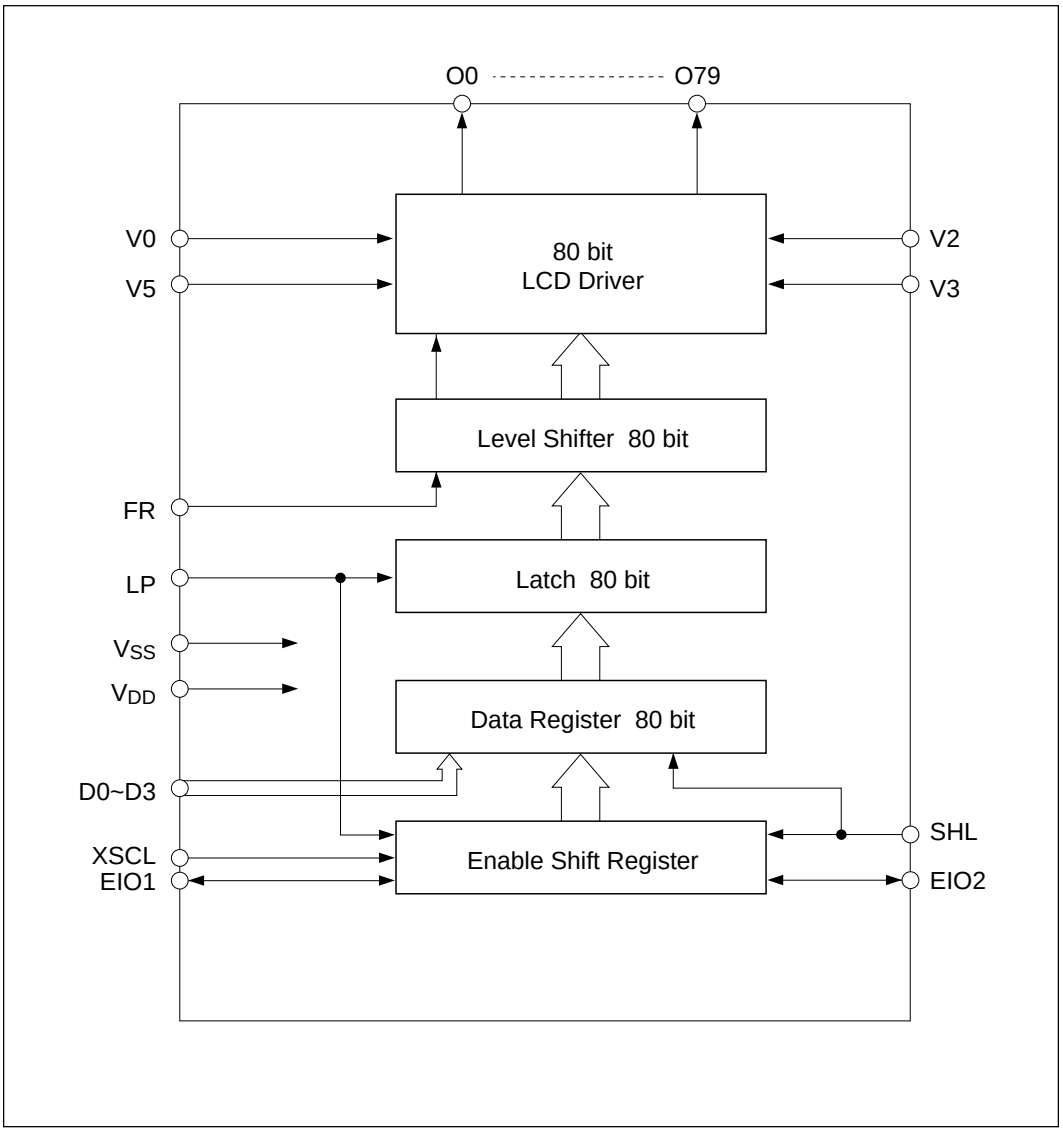
■ DESCRIPTION

The SED1606 is an 80-output segment (column) driver for use in combination with an SED1635. It is provided with high-vision measure of the LCD display and adopts high speed inable chain system for low power operation and slim chip shape suitable for minimizing of the LCD panel. Also, low voltage operation of the logic power source suits a wide range of applications.

■ FEATURES

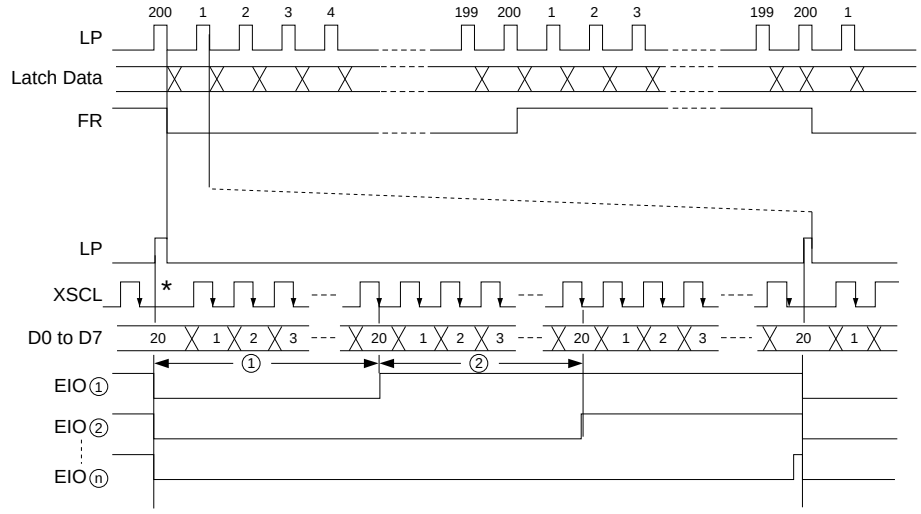
- LCD driver output number 80
- Ultra-slim chip
- Low current consumption
- Low voltage operation ..... –2.7V max.
- Wide range of liquid crystal drive voltage ..... –8 to –28V
- High speed and low power data transfer is possible by adoption of the 4-bit bus inable chain system.
  Shift clock frequency:
  6.5MHz (at –2.7V)
  10.0MHz (at –4.5V)
- Non-bias display off function
- Pin selection of the output shift direction is available
- Offset bias regulation of the liquid crystal power is possible depending on the V_{DD} level
- Logic system power source ..... –2.7 to –5.5V
- Product shapes

■ **BLOCK DIAGRAM**



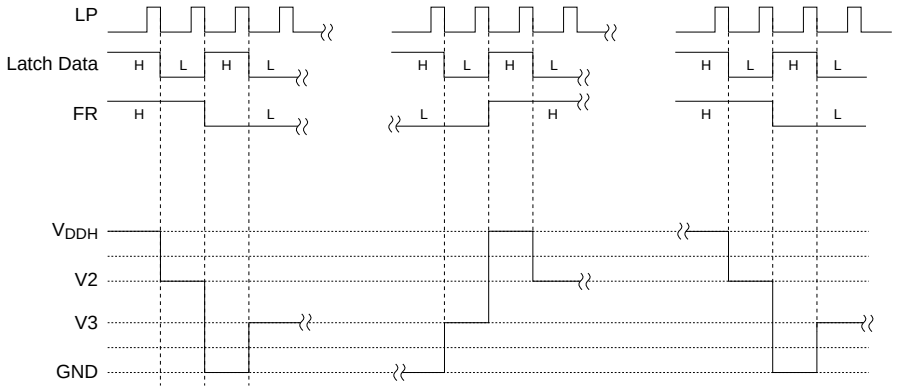
■ TIMING DIAGRAM

In case of 1/200 duty (an example)



◯ to ◯ indicate the cascade numbers of drivers.

*In case of high speed data transfer, it is necessary to secure a longer XSCL cycle in the timing of the LP pulse insertion in order to maintain the specified value of LP → XSCL (t_{LH}).



■ FUNCTIONS

● Inable Shift Register

The inable shift register is a bi-directional shift register wherewith the shift direction is determined by the SHL inputs and outputs of such shift register are used to store data bus signals to the data register. When inable signals are in the disable state, the internal clock signal and data bus are fixed to “L” to become the power save mode.

When using multiple units of the segment driver, EIO terminals of each driver should be connected by the cascade connection and the EIO terminals of the top end driver should be connected to “V_{DD}”. (Refer to the connection example). Since the inable control circuit automatically detects when all the 80-bit data are taken in and automatically transfers the inable signal, control signals from a controlling LSI are not needed.

● Data Register

This is a register for serial and parallel conversion of data bus signals by means of the inable shift register output. Consequently, the relations between the serial display data and segment outputs are determined independently from the shift clock input number.

● Latch

It takes in the contents of the data register by means of the trailing edge trigger of the LP to transmit the output to the level shifter.

● Level Shifter

This is a level interface circuit to convert the voltage level of signals from logic level to LCD driving level.

● LCD Driver

It outputs the LCD drive voltage.

Relations among data bus signals, alternating signals FR and the segment output voltage are given below.

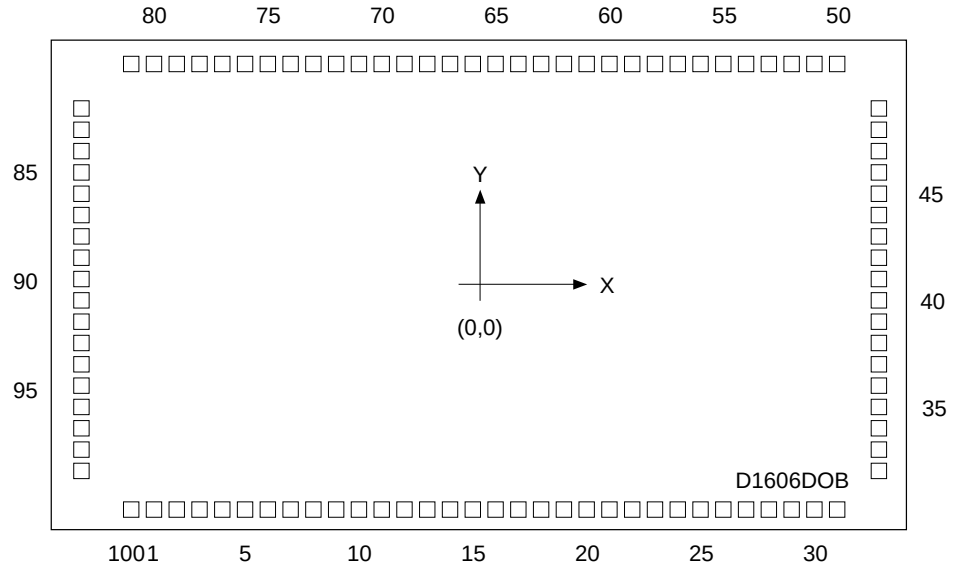
Data Bus Signals	FR	O Output Voltage
H	H	V_0
	L	V_5
L	H	V_2
	L	V_3

■ FUNCTIONS OF THE TERMINALS

<table>
<tr><th>Terminal Name</th><th>I/O</th><th>Description</th><th>Numbers of Pins</th></tr>
<tr><td>O 0 ~
O79</td><td>O</td><td>LCD driving segment (column) output
The output level varies at the trailing edge of the LP.</td><td>80</td></tr>
<tr><td>D0 ~ D3</td><td>I</td><td>Display data input</td><td>4</td></tr>
<tr><td>XSCL</td><td>I</td><td>Shift clock input of display data (trailing edge trigger)</td><td>1</td></tr>
<tr><td>LP</td><td>I</td><td>Latch pulse input of display data (trailing edge trigger)</td><td>1</td></tr>
<tr><td>EIO1
EIO2</td><td>I/O</td><td>Enable input and output
Set to input or output depending on the SHL input level.
The output is reset by the LP input and, after recieving
80 bit data, it automatically rises to “H”</td><td>2</td></tr>
<tr><td>SHL</td><td>I</td><td>Shifting direction choice, and input/output controling input to the EIO terminal
When data is input to (D3, D2, ...D0)
terminals in the order of (a3, a2, a1, a0) (b3,b2,b1,b0).....
(t2, t2, t1, t0), relations between data and
segment outputs are as follows.
<table>
<tr><th rowspan="2">SHL</th><th colspan="8">O Output</th><th colspan="2">EIO</th></tr>
<tr><th>79</th><th>78</th><th>77</th><th></th><th>2</th><th>1</th><th>0</th><th>EIO1</th><th>EIO2</th></tr>
<tr><td>H</td><td>a3</td><td>a2</td><td>a1</td><td>....</td><td>t2</td><td>t1</td><td>t0</td><td>Output</td><td>Input</td></tr>
<tr><td>L</td><td>t0</td><td>t1</td><td>t2</td><td>....</td><td>a1</td><td>a2</td><td>a3</td><td>Input</td><td>Output</td></tr>
</table>
Note: Relations between the data and segment outputs are determined independent from the shift clock number.</td><td>1</td></tr>
<tr><td>FR</td><td>I</td><td>Input of the alternating signal of the LCD drive output</td><td>1</td></tr>
<tr><td>V_{DD}, V_{SS}</td><td>Power source</td><td>Power supply for the logics V_{DD}: 0V
V_{SS}: –2.7 ~ –5.5V</td><td>2</td></tr>
<tr><td>V_0, V_2,
V_3, V_5</td><td>Power source</td><td>Power supply for the LCD driver circuit
V_{DD}: 0V V5: –8 ~ –28V
$V_{DD} \geq V_0 \geq V_2$ 6/9 V_5
*1 3/9 $V_5 \leq V_3 \leq V_5$</td><td>4</td></tr>
<tr><td></td><td></td><td>Total</td><td>100
(including NC4)</td></tr>
</table>

*1. Be sure to connect pairs of V0 – V5 to respective LCD power sources.

■ **PAD LAYOUT**



Chip Size:	5.59mm × 3.50 mm
Pad Pitch:	0.153mm (min)
Chip Thickness:	0.400mm (Al pad) 0.525mm (Au bump)

Au bump (for reference)

Bump size:	117μm × 109μm ± 20μm
Bump height:	17~28μm

■ PAD COORDINATES

Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y
1	$\overline{O}$ 0	–2227	–1578	35	$\overline{O}$ 34	2622	–871	69	$\overline{O}$ 68	–537	1578
2	$\overline{O}$ 1	–2073	↓	36	$\overline{O}$ 35	↓	–713	70	$\overline{O}$ 69	–691	↓
3	$\overline{O}$ 2	–1920		37	$\overline{O}$ 36		–554	71	$\overline{O}$ 70	–846	
4	$\overline{O}$ 3	–1766		38	$\overline{O}$ 37		–396	72	$\overline{O}$ 71	–998	
5	$\overline{O}$ 4	–1612		39	$\overline{O}$ 38		–238	73	$\overline{O}$ 72	–1152	
6	$\overline{O}$ 5	–1459		40	$\overline{O}$ 39		–79	74	$\overline{O}$ 73	–1305	
7	$\overline{O}$ 6	–1305		41	$\overline{O}$ 40		79	75	$\overline{O}$ 74	–1459	
8	$\overline{O}$ 7	–1152		42	$\overline{O}$ 41		238	76	$\overline{O}$ 75	–1613	
9	$\overline{O}$ 8	–998		43	$\overline{O}$ 42		396	77	$\overline{O}$ 76	–1766	
10	$\overline{O}$ 9	–845		44	$\overline{O}$ 43		554	78	$\overline{O}$ 77	–1920	
11	$\overline{O}$ 10	–891		45	$\overline{O}$ 44		713	79	$\overline{O}$ 78	–2073	
12	$\overline{O}$ 11	–537		46	$\overline{O}$ 45		871	80	$\overline{O}$ 79	–2227	
13	$\overline{O}$ 12	–384		47	$\overline{O}$ 46		1029	81	EIO2	–2381	↓
14	$\overline{O}$ 13	–230		48	$\overline{O}$ 47		1188	82	D0	–2622	1346
15	$\overline{O}$ 14	–76		49	$\overline{O}$ 48	↓	1346	83	D1	↓	1192
16	$\overline{O}$ 15	77		50	$\overline{O}$ 49	2381	1578	84	D2		1039
17	$\overline{O}$ 16	231		51	$\overline{O}$ 50	2228	↓	85	D3		885
18	$\overline{O}$ 17	384		52	$\overline{O}$ 51	2074		86			732
19	$\overline{O}$ 18	538		53	$\overline{O}$ 52	1921		87			578
20	$\overline{O}$ 19	692		54	$\overline{O}$ 53	1767		88			424
21	$\overline{O}$ 20	845		55	$\overline{O}$ 54	1613		89			271
22	$\overline{O}$ 21	999		56	$\overline{O}$ 55	1460		90	VDD		106
23	$\overline{O}$ 22	1152		57	$\overline{O}$ 56	1306		91	VSS		–58
24	$\overline{O}$ 23	1306		58	$\overline{O}$ 57	1152		92	V0		–224
25	$\overline{O}$ 24	1460		59	$\overline{O}$ 58	999		93	V2		–389
26	$\overline{O}$ 25	1613		60	$\overline{O}$ 59	845		94	V3		–553
27	$\overline{O}$ 26	1767		61	$\overline{O}$ 60	692		95	V5	↓	–718
28	$\overline{O}$ 27	1921		62	$\overline{O}$ 61	538		96	SHL	–2611	–885
29	$\overline{O}$ 28	2074		63	$\overline{O}$ 62	384		97	XSCL	↓	–1039
30	$\overline{O}$ 29	2228		64	$\overline{O}$ 63	231		98	LP		–1192
31	$\overline{O}$ 30	2381	↓	65	$\overline{O}$ 64	77		99	FR	↓	–1346
32	$\overline{O}$ 31	2622	–1346	66	$\overline{O}$ 65	–76		100	EIO1	–2381	–1578
33	$\overline{O}$ 32	2622	–1188	67	$\overline{O}$ 66	–230					
34	$\overline{O}$ 33	2622	–1029	68	$\overline{O}$ 67	–384	↓				

■ ELECTRICAL CHARACTERISTICS

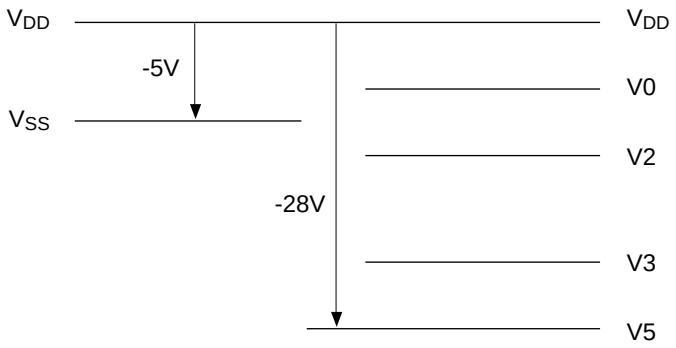
● Absolute Maximum Rating

Parameters	Codes	Ratings	Units
Power voltage (1)	V_{SS}	–7.0 ~ +0.3	V
Power voltage (1)	V_5	–30.0 ~ +0.3	V
Power voltage (3)	V_0, V_2, V_3	V_5 – 0.3 ~ V_{DD} +0.3	V
Input voltage	V_I	V_{SS} – 0.3 ~ V_{DD} +0.3	V
Output voltage	V_O	V_{SS} – 0.3 ~ V_{DD} +0.3	V
EIO output current	I_{O1}	20	mA
Working temperature	Topr	–40 ~ +85	°C
Storage temperature 1	Tstg1	–65 ~ +150	°C

Note 1. All the above voltages are based on V_{DD} = 0V.

Note 2. The storing temperature 1 specifies that of chips proper.

Note 3. Voltage of V0, V2 and V3 should always be maintained under a condition of $V_{DD} \geq V0 \geq V2 \geq V3 \geq V5$.



Note 4. When logic power becomes floating state or if V_{SS} = –2.6 or beyond while the LCD driver power source is being applied, the LSI may be permanently damaged and avoid such circumstances.

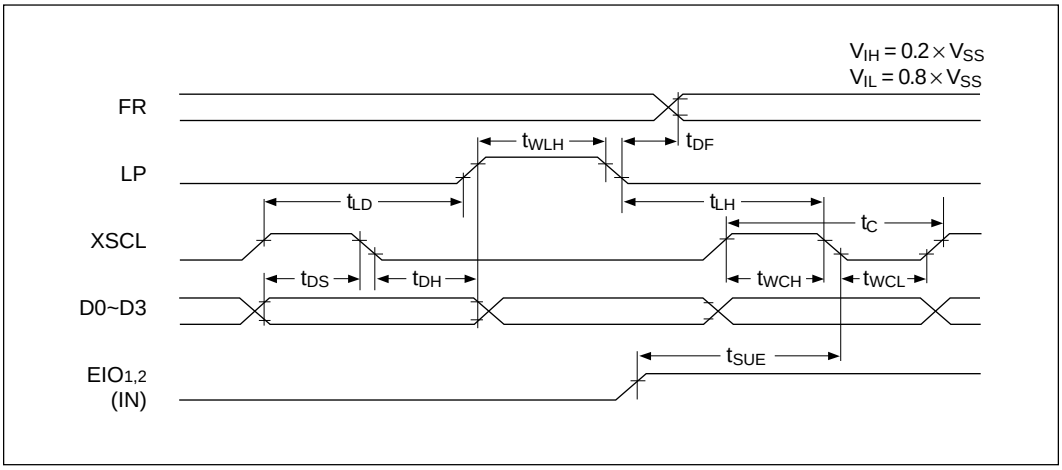
Pay extra attention to the power sequence at times of turning on and turning off the power supply.

- **DC Characteristics**

Unless otherwise designated, V_{DD} = V0 = 0V, V_{SS} = –5.0 ±10% and T_a = –40 to 85°C

Parameter	Symbol	Condition		Applicable Pin	Min	Typ	Max	Unit
Power voltage (1)	V_{SS}	—		V_{SS}	–5.5	–5.0	–2.7	V
Recommended working voltage	V_5	—		V_5	–28.0	—	–12.0	V
Operable voltage	V_5	Function		V_5	—	—	–8.0	V
Power voltage (2)	V_0	Recommended value		V_0	V_{DD} –2.5	—	V_{DD}	V
Power voltage (3)	V_2	Recommended value		V_2	V_2	3/9 V_5	—	V
Power voltage (4)	V_2	Recommended value		V_3	V_3	—	6/9 V_5	V
High level input voltage	V_{IH}	V_{SS}= 2.7~ 5.5V		EIO1, EIO2, FR D0–D3, XSCL SHL, LP,	0.2V_{CC}	—	—	V
Low level input voltage	V_{IL}						0.8V_{SS}	V
High level output voltage	V_{OH}	V_{SS} = 2.7 – 5.5V	I_{OH} = –0.6mA	EIO1, EIO2	V_{DD} – 0.4	—	—	V
Low level output voltage	V_{OL}		I_{OL} = 0.6mA		—	—	0.4	V
Input leak current	I_{LI}	$V_{SS} \le V_{IN} \le V_{DD}$		D0–D3, LP, FR XSCL, SHL	—	—	2.0	µA
Input Output leak current	$I_{LI/O}$	$V_{SS} \le V_{IN} \le V_{DD}$		EIO1, EIO2	—	—	5.0	µA
Rest current	I_{SS}	V_5 = 28.0 ~ – 14.0V V_{IH} = GND, V_{IL} = GND		V_{SS}	—	—	25	µA
Output resistance	R_{SEG}	ΔV_{ON} = 0.5V , Ta = 25°C V_5 = –20.0V V_3 = 13/15 V_5 V_2 = 2/15 V_5 V0 = V_{DD}		O 0 ~ O 79		1.2	1.6	KΩ
Average operating current consumption (1)	I_{SS}	V_{SS} = +5.0V, V_{IH} = V_{DD} V_{IL} = V_{SS}, f_{XSCL} = 2.69MHz f_{LP} = 16.8KHz, f_{FR} = 70Hz input data: Diced display no-load		V_{SS}	—	0.10	0.2	mA
		V_{SS} = +3.0V Other conditons are the same as with V_{SS} = –5V			—	0.7	0.15	
Average operating current consumption (2)	I_5	V_{SS} + 5.0V, V_O = 0.0V V_2 = +9.30V, V_3 = –18.6V, V_5 = +28.0V Other conditions are the same as with the item I_{SS}.		V_5	—	0.05	0.04	mA
Input terminal capacity	CI	Freq. = 1 Mhz Ta = 25°C XSCL,SHL chips proper		D0–D3, LP, FR	—	—	8	pF
I/O terminal capacity	$C_{I/O}$			EIO1, EIO2	—	—	15	pF

- **AC Characteristics**
  - **Input Timing Characteristics**



V_{SS} = –5.0V ± 0.5V, T_a = –40 to 85°C

Parameter	Symbol	Conditions	Min.	Max.	Units
XSCL cycle	t_C		100	—	ns
XSCL high level pulse duration	t_{WCH}		30	—	ns
XSCL low level pulse duration	t_{WCL}		30	—	ns
Data setup time	t_{DS}		20	—	ns
Data hold time	t_{DH}		10	—	ns
XSCL → LP rise time	t_{LD}		0	—	ns
LP → XSCL fall time	t_{LH}		40	—	ns
LP high level pulse duration	t_{WLH}	*3	40	—	ns
FR delay allowance	t_{DF}		–900	+900	ns
EIO setup time	t_{SUE}		35	—	ns

V_{SS} = –4.5V to 2.7V, T_a = –40 to 85°C

Parameter	Symbol	Conditions	Min.	Max.	Units
XSCL cycle	t_C	V_{SS} = –2.7V *1	153	—	ns
		V_{SS} = –3.0V *2	133		
XSCL high level pulse duration	t_{WCH}		50	—	ns
XSCL low level pulse duration	t_{WCL}		50	—	ns
Data setup time	t_{DS}		30	—	ns
Data hold time	t_{DH}		15	—	ns
XSCL → LP rise time	t_{LD}		0	—	ns
LP → XSCL fall time	t_{LH}	V_{SS} = –2.7V	75	—	ns
		V_{SS} = –3.0V	65		
LP high level pulse duration	t_{WLH}	V_{SS} = –2.7V *3	75	—	ns
		V_{SS} = –3.0V *3	65		
FR delay allowance	t_{DF}		–900	+900	ns
EIO setup time	t_{SUE}	V_{SS} = –2.7V	60	—	ns
		V_{SS} = –3.0V	51		

Notes: *1. 6.5MHz equivalence

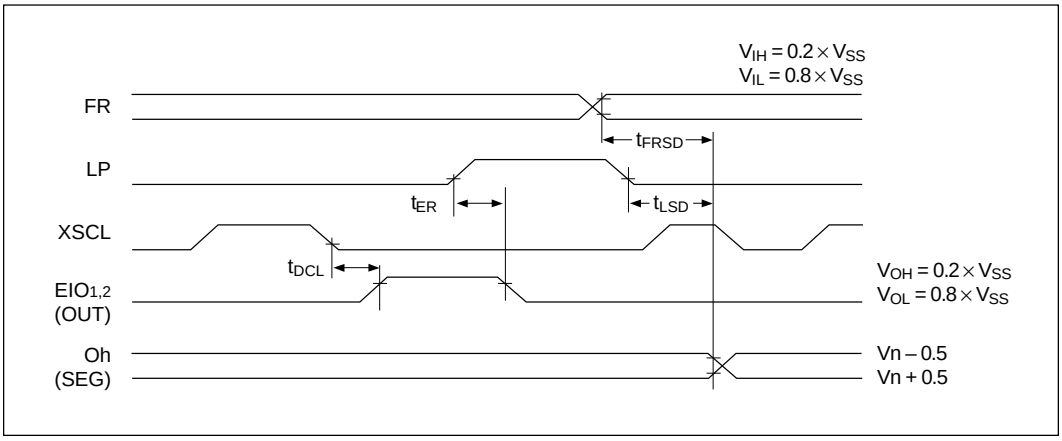
*2. 7.5MHz equivalence

*3. t_{wLH} specifies the time when LP is “H” and, at the same time, XSCL is “L”.

*4. The input signal t_r, t_f is fixed to 20ns.

*5. High-speed operation of the shift clocks (XSCL) should only be made under a condition of tr or $t_f \leq \{t_c - (t_{DCL} + t_{SUE})\}/2$

○ **Output Timing Characteristics**



V_{DD} = –5.0 ± 5%V, V5 = –12.0 to –28.0V

Parameter	Symbol	Conditions	Min.	Max.	Units
EIO reset time	t_{ER}	C_L = 15 pf (EIO)	—	90	ns
EIO output delay time	t_{DCL}		—	55	ns
LP → SEG output delay time	t_{LSD}	C_L = 100 pf (0 n)	—	200	ns
FR → SEG output delay time	t_{FRSD}		—	400	ns

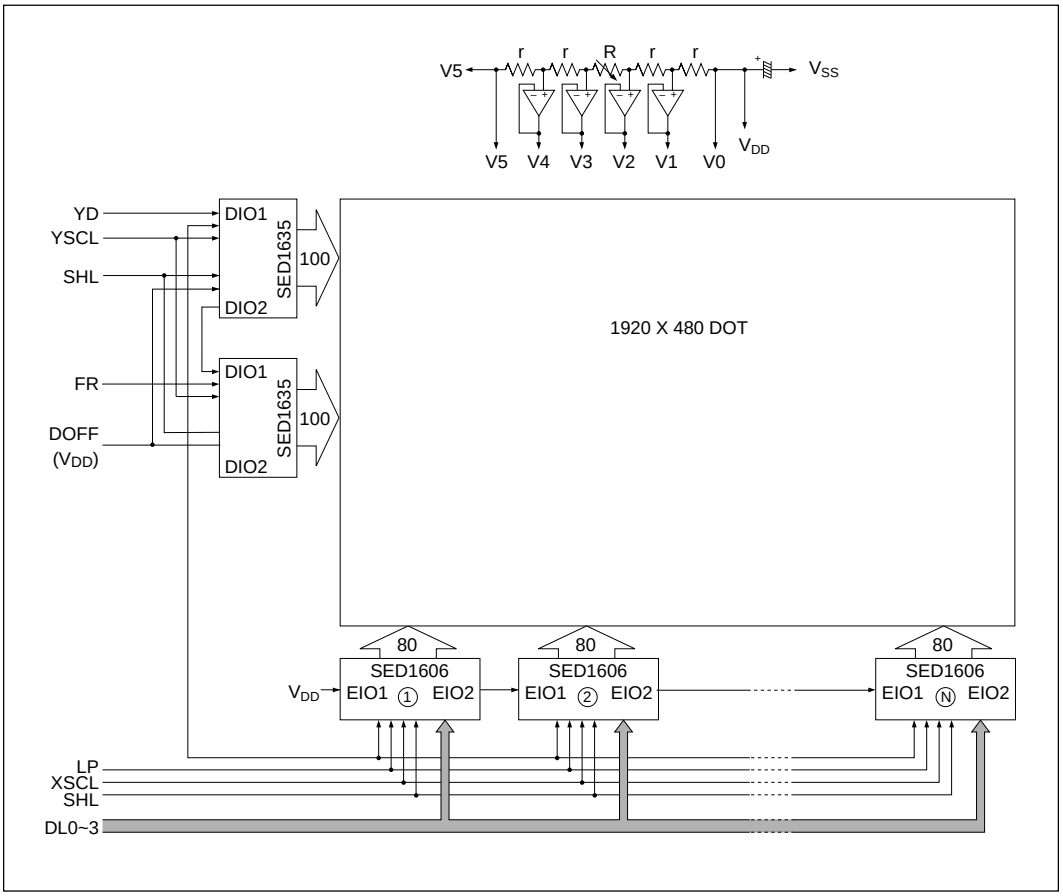
V_{DD} = –4.5 to –2.7V, V5 = –12.0 to –28.0V

Parameter	Symbol	Conditions		Min.	Max.	Units
EIO reset time	t_{ER}	C_L = 15 pf (EIO)		—	150	ns
EIO output delay time	t_{DCL}		V_{SS} = –2.7V	—	88	ns
			V_{SS} = –3.0V		77	ns
LP → SEG output delay time	t_{LSD}	C_L = 100 pf (0 n)		—	400	ns
FR → SEG output delay time	t_{FRSD}			—	800	ns

Notes: *1. The input signal t_r, t_f is fixed to 20ns.

*2. High speed operation of the shift clocks (XSCL) should be made only under a condition of t_f or $t_f \leq \{t_C - (t_{DCL} + t_{SUE})\}/2$.

■ **CONNECTION EXAMPLE**



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